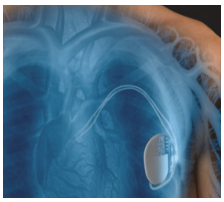

# Silicon PICS technology in portable and implantable medical applications

Rev 1.5

Application Note

## Outline

Medical portable or implantable applications are very sensitive to volume constraints and require higher and higher integration performance as well as significant performance improvements for the devices.

Some specific assembly conditions (temperature, etc.) provide additional constraints that generally limit the number of solutions supporting these conditions.

Two types of application are detailed at the end of the document.

## Problem in portable/implantable medical devices

- Significant volume constraints
- High reliability
- Battery lifetime, requiring low leakage current on capacitors
- Efficient decoupling with minimum embedded capacitors
- Oversizing of capacitor value (often a factor of 2) for sensitive capacitive circuitry to secure the amount of energy stored in the capacitors, whatever the operating voltage
- High temperature cycling during manufacturing operations

## Solutions and benefits with PICS technology

- Capacitor integration capability up to **2000 nF/mm$^3$**
- High integration capability reducing the number of passive components in the application and eliminating cracking. **TDDB$^{(*)}$ > 12 years @37°C** (lifetime)
- Very low leakage current (**< 500 pA** for a 200 nF capacitor @3.6 V)
- Very stable capacitor value over the full operating voltage & temperature ranges (**-55 to +200°C**)
- Silicon based process compatible with high temperature cycling (**exceeding 300°C**)

(*)TDDB: Time Dependent Dielectric Breakdown

## Decoupling efficiency and charge pump analysis

### Power supply decoupling aspects

Power supply decoupling can often be optimized with even better performance compared with standard decoupling with SMD capacitors, but certain rules need to be verified.

A decoupling capacitor offers two domains where the decoupling is effective:

- the capacitive area directly related to the capacitor value
- the inductive area driven by the parasitic ESL

The following figure represents the comparison in terms of insertion loss between a 100 nF SMD MLCC capacitor (for example X7R, NPO, etc.) and a 100 nF PICS capacitor.

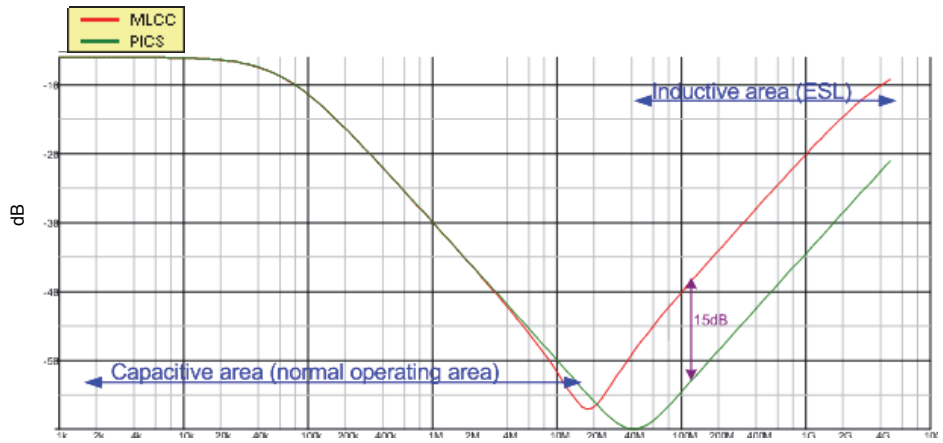


Fig.1 MLCC and PICS capacitor insertion loss (100 nF)

The insertion loss at the resonance frequency is directly driven by the ESR capacitor (lower with PICS technology). The decoupling efficiency can be improved by 15 dB in the inductive area.

Two decoupling situations are described below as examples.

*Situation 1: Multiple resonances for high band efficiency (RF decoupling)*

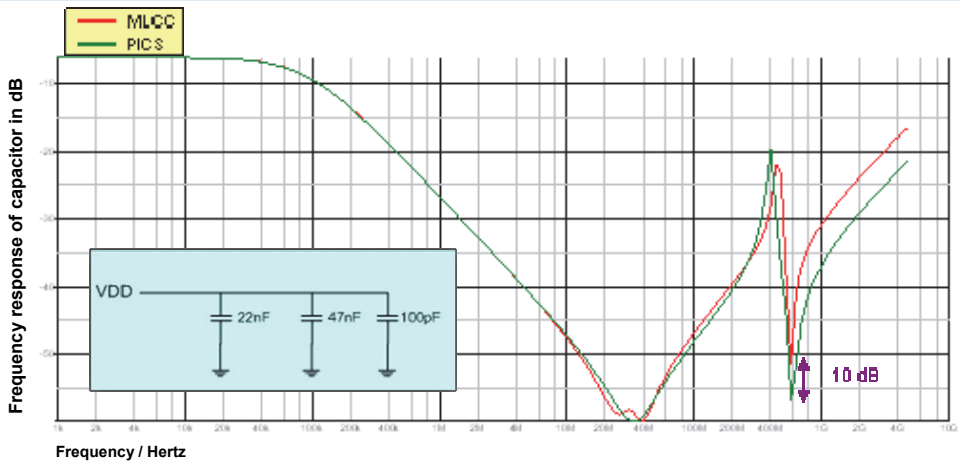


Fig.2 Analog decoupling situation with MLCC & PICS capacitors

For this type of situation, the decoupling capacitor value needs firstly to stay at the same value (no optimization). The advantage with PICS is **better efficiency at the resonance frequencies (lower ESR)**.

To save area (value capacitance reduction), it is recommended to replace MLCC and Tantalum capacitors by PICS capacitors. Depending on the operating frequency, the PICS capacitor is equivalent to 1/2 to 1/10 capacitance value of MLCC & Tantalum cap. since the impedance @ resonance frequency (ESR) of PICS is lower than MLCC & Tantalum cap. Refer to the impedance curve graph Fig 4.

For example:

| MLCC & Tantalum Cap. | | PICS recommended Cap. |
|---|---|---|
| 100 pF | | 10 pF to 50 pF |
| 4.7 nF | | 470 pF to 2.35 nF |
| 100 nF | ⇒ | 10 nF to 50 nF |
| 1 µF | | 100 nF to 0.5 µF |
| 4.7 µF | | 470 nF to 2.37 µF |
| 10 µF | | 1 µF to 5 µF |

Note that the PICS technology allows fine tuning of the ESL to place the notch at the required frequency.

*Situation 2: digital devices (digital power supply decoupling)*

This situation is met with decoupling of digital devices. As an example, we assume a 100 nF capacitor is used for the decoupling and generally, the capacitor is used in the inductive area as we need to suppress frequencies above a certain value. The PICS capacitor is placed very close to the power supply pins/pads to be decoupled (extreme reduction of the parasitic inductance between the capacitor and the pads). It is very common to divide the SMD capacitor value **by a factor 4 to 5.**

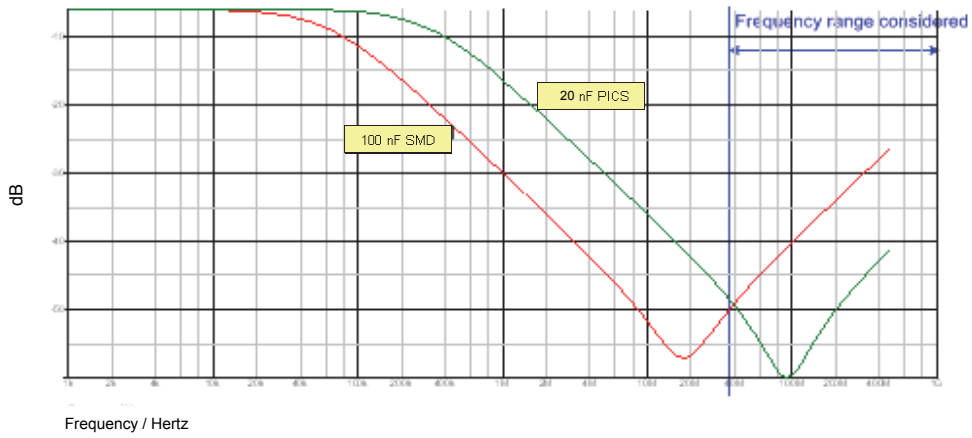


Fig.3 Digital power supply decoupling situation with PICS capacitors

For example, the following figure represents an 8.7 nF PICS2 capacitor impedance. The resonance frequency is measured @7.2 GHz with an **ESR of 27 mΩ** –> **ESL=56 fH**

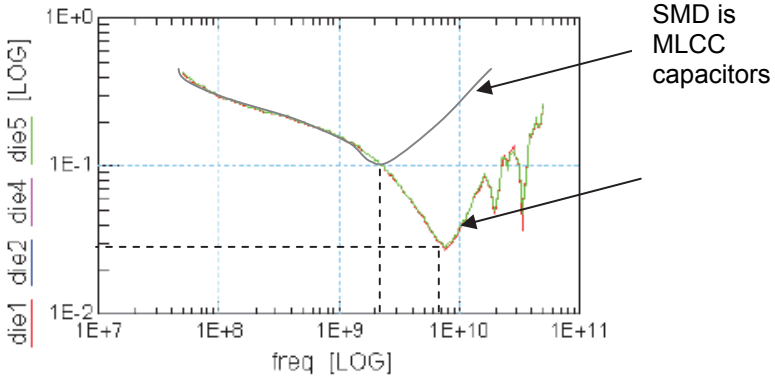


Fig.4 Impedance of 8.7 nF PICS2 capacitor (Ω)

## Charge pump aspects

In charge pump applications, two parameters are critical:

- the capacitor value stability over the voltage applied (see Fig.5 & 6)
- the leakage current which must be as small as possible to ensure the capacitors remain charged. This is important for battery powered applications (see Fig. 7 & 8).

The next figure shows the stability of the capacitor value (C) compared with the value when no voltage is applied ($C_0$) for various supply voltages and temperatures.

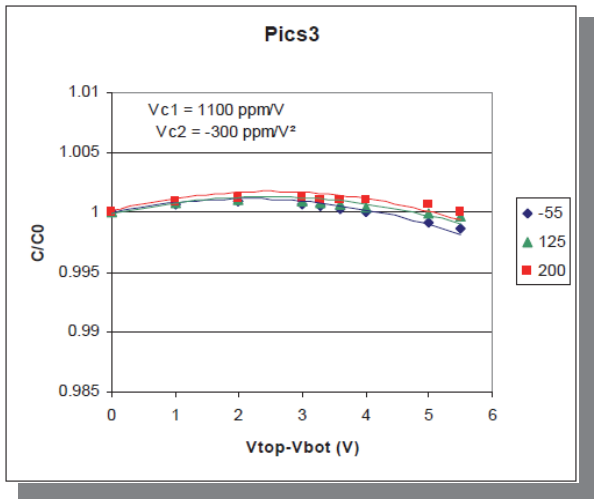


Fig.5 Capacitance stability vs. applied voltage at different temperatures

The capacitance 'C' can be expressed as:

$$C = C_0.(1 + VC_1.V + VC_2.V^2).(1 + Tcl.(T - T_0))$$

For PICS3: $VC_1$= 1100 ppm/V $VC_2$= -300 ppm/V² Tcl= 62 ppm/K

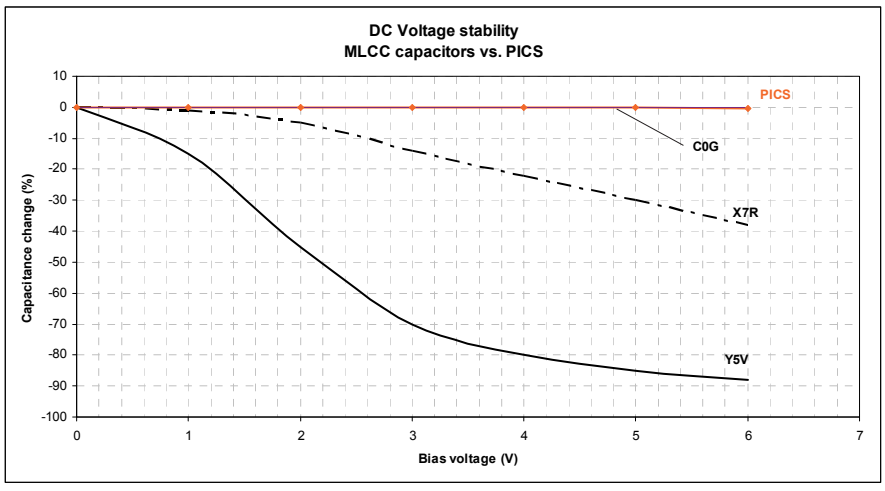


Fig.6 Voltage stability performance comparisons with various type of MLCC capacitor

The next figure provides some indications in terms of leakage current performances for three capacitor values processed in PICS3.

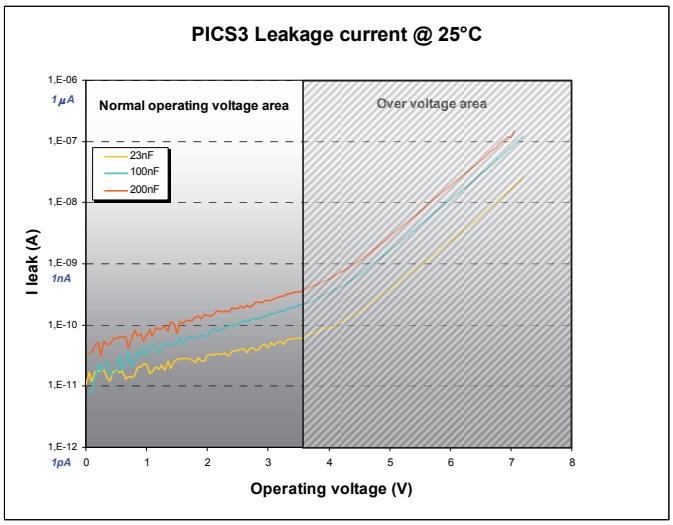


Fig.7 Leakage current in PICS capacitors (PICS3)

For nominal supply voltages (< 3.6 V), the leakage current remains below 0.5 nA.

The next figure provides the leakage current variation for a 100 nF capacitor vs. the operating voltage for different temperatures.

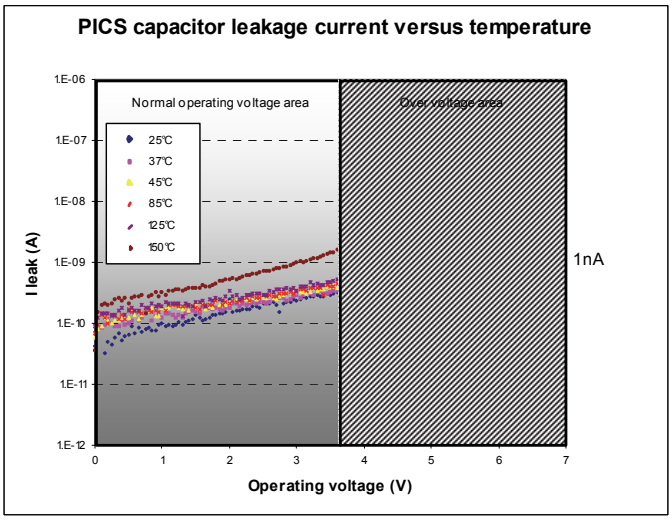


Fig.8 Leakage current in a 100nF PICS capacitor vs. temperature (PICS3)

Key values:

- leakage current <30 nA/µF whatever the process, temperature and voltage conditions
- leakage current variation < 12 pA [per 100 nF] /°C (1 nA @85°C @3.6 V for 100 nF)

## Cardiac defibrillator applications

Implantable medical units such as cardiac defibrillators are devices for which volume and weight savings are key issues.

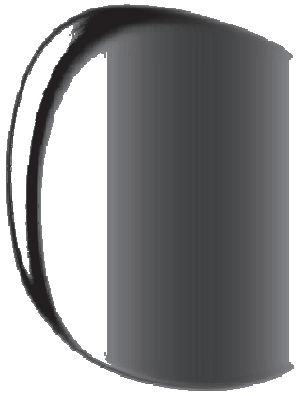

Fig.9 Defibrillator device

The electronic section integrates various SMD capacitors for decoupling purposes and charge pump applications. Some active dies can be wire bonded or flip chipped directly on the PCB due to space constraints.

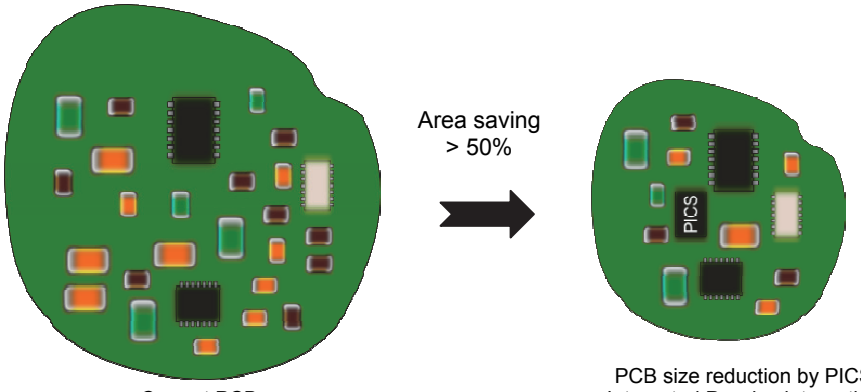


Fig.10 PCB size reduction with PICS technology

Main PICS technology advantages:

- higher decoupling efficiency,
- integration of high value capacitors in a reduced volume,
- battery lifetime: up to 30 % more.

## Hearing aid applications

This type of device requires advanced integration technologies because of high volume constraints.

The electronic section integrates a few passive components either for decoupling or various analog functions (oscillators, wireless sections [FM-Bluetooth], etc.).

PICS capacitors are highly recommended for decoupling of power supplies, especially on digital devices such as DSP's (refer to 'situation 2' in power supply decoupling in the previous section).

The low ESR performance of PICS capacitors allows lower value capacitors to be embedded compared with standard SMD, offering advantages in terms of volume.

IPD technology also offers capabilities for RF/wireless sections. High Q coils can be designed as well as derived functions, such as baluns, filters, etc.

## Integration capabilities with PICS

PICS IPD technology is a silicon based process, allowing various assembly architectures:

- Wire bonding
- Wafer level chip scale packaging (WLCSP)
- Die stacking

Dies can be molded (plastic compound, glass), used as Chip On Board (COB), flip-chipped on PCB or flex substrate.

## Quality

The IPDiA manufacturing center is certified:

- ISO-9001
- ISO-14001
- ISO-TS16949
- OHSAS-18001

IPDiA is RoHS compliant.