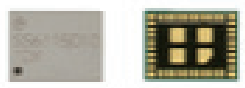
Hardware Application Note

Wi-Fi® + Bluetooth® Combo Module

Infineon CYW4343W Chipset for 802.11b/g/n + Bluetooth 5.1

Hardware Application Note - Rev. 7.0

- Design Name: Type 1DX
- Module P/N: LBEE5KL1DX



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About This Document

This application note provides the hardware development guidelines for Type 1DX (CYW4343W) and guidelines for the design of schematic, layout, and reference RF performance. For detailed module specification, refer to Type 1DX Datasheet for module specification.

Audience & Purpose

This document is targeted towards system integrators for Wi-Fi/Bluetooth solutions using Murata Type 1DX module, based on Infineon CYW4343W chipset.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	**Warning Note** Indicates very important note. Users are strongly recommended to review.
	**Info Note** Intended for informational purposes. Users should review.
	**Menu Reference** Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	**External Hyperlink** This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	**Internal Hyperlink** This symbol indicates a hyperlink within the document. **Example**: Module Introduction Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Module Introduction

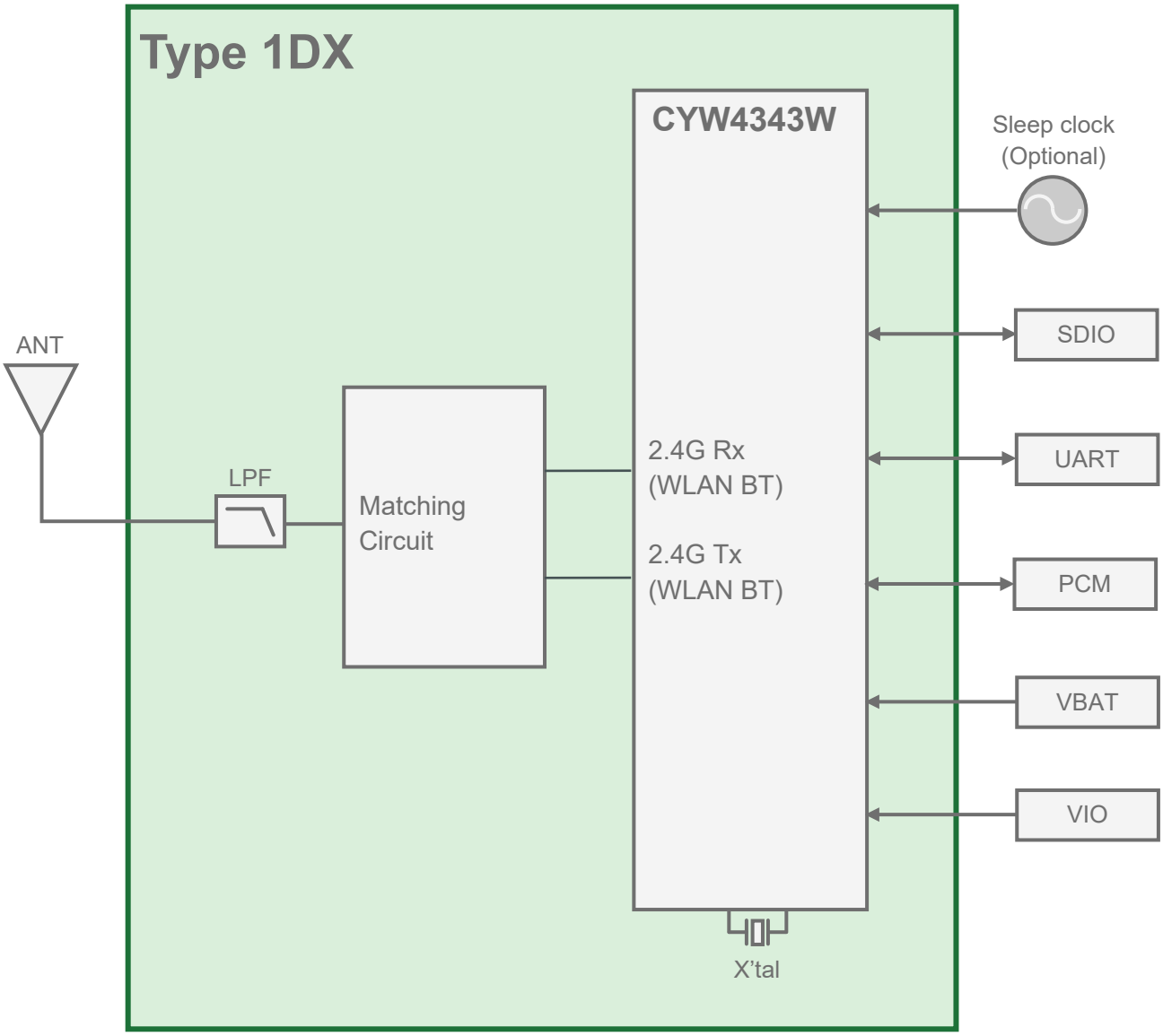
Type 1DX (1x1) is Wi-Fi + BT/BLE combo SIP module with Infineon CYW4343W, which is single-chip 2.4GHz WLAN IEEE 802.11 b/g/n MAC/Baseband/Radio, Bluetooth 5.1 support chip. (See Type 1DX Datasheet).

There are LPF and matching circuit in front of CYW4343W chipset. Ant port is tuned as 50 ohms output. Fast clock (X'tal) is also embedded. Some external components will be required to complete Wi-Fi/BT/BLE circuit. This module is covered with resin molding and fully shielded with metal. The package type is LGA (SMD type).

2 Hardware Block Diagram

The type 1DX module's internal block diagram is shown in **Figure 1**.

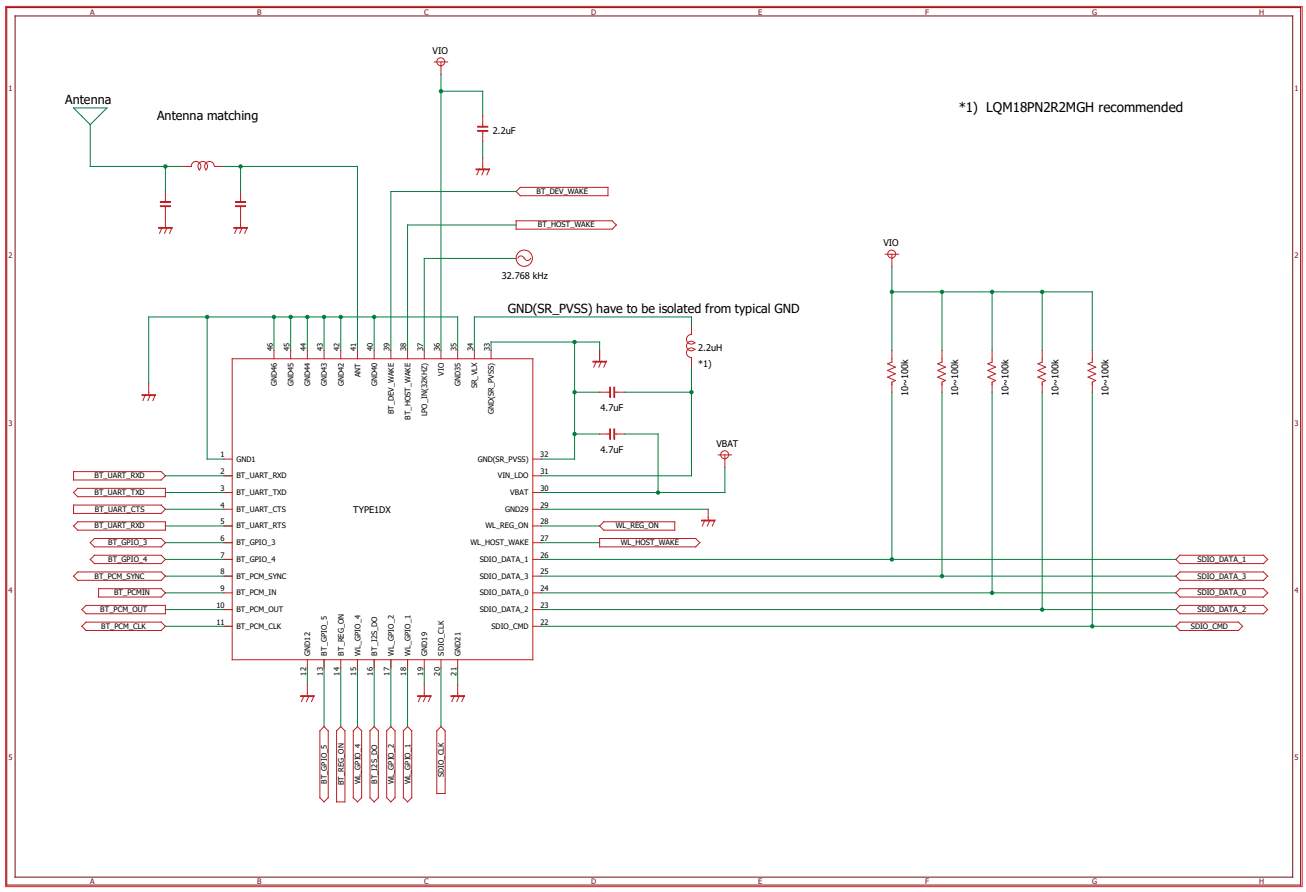
Figure 1: Block Diagram



3 Reference Circuit

Figure 2 shows the reference circuit design for Type 1DX module.

Figure 2: Reference Circuit Design



4 External BOM List (Reference)

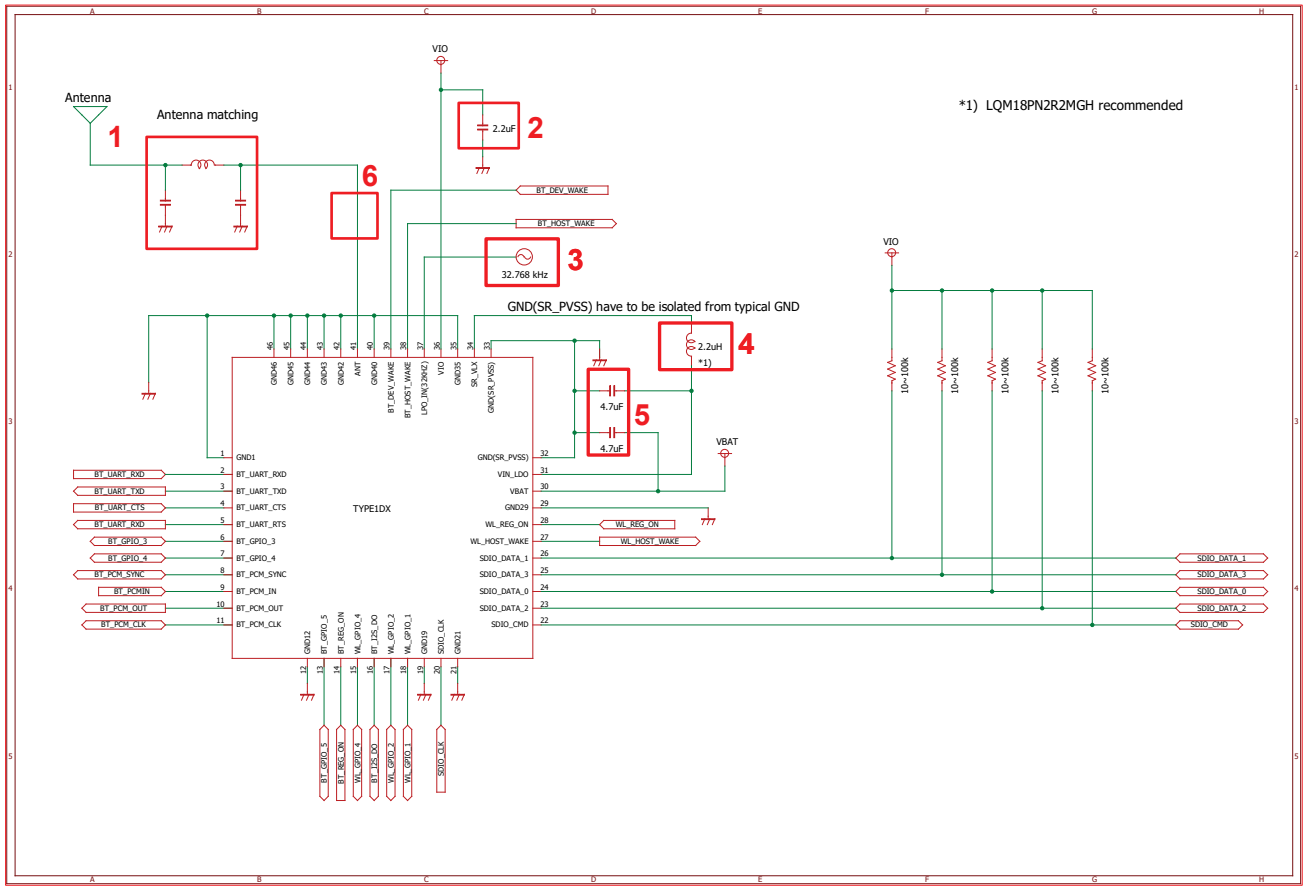
Table 2 describes the list of external components.

Table 2: External BOM List (Reference)

Block	Components	Value	pcs	Note
1	L or C	TBD	3	Depend on PCB structure / design (for Antenna matching)
2	C	2.2 uF	1	
3	LPO	32.768kHz	1	Pls see the required spec on the module datasheet
4	L	2.2uH	1	LQM18PN2R2MGH recommended. (1.05 A, DCR = 0.25 ohm)
5	C	4.7uF	2	4.7uF
6	Connector		1	In case of testing RF conductive performance. (Right next to the module)

Figure 3 shows the external BOM list reference circuit design.

Figure 3: External BOM List Reference Circuit Design



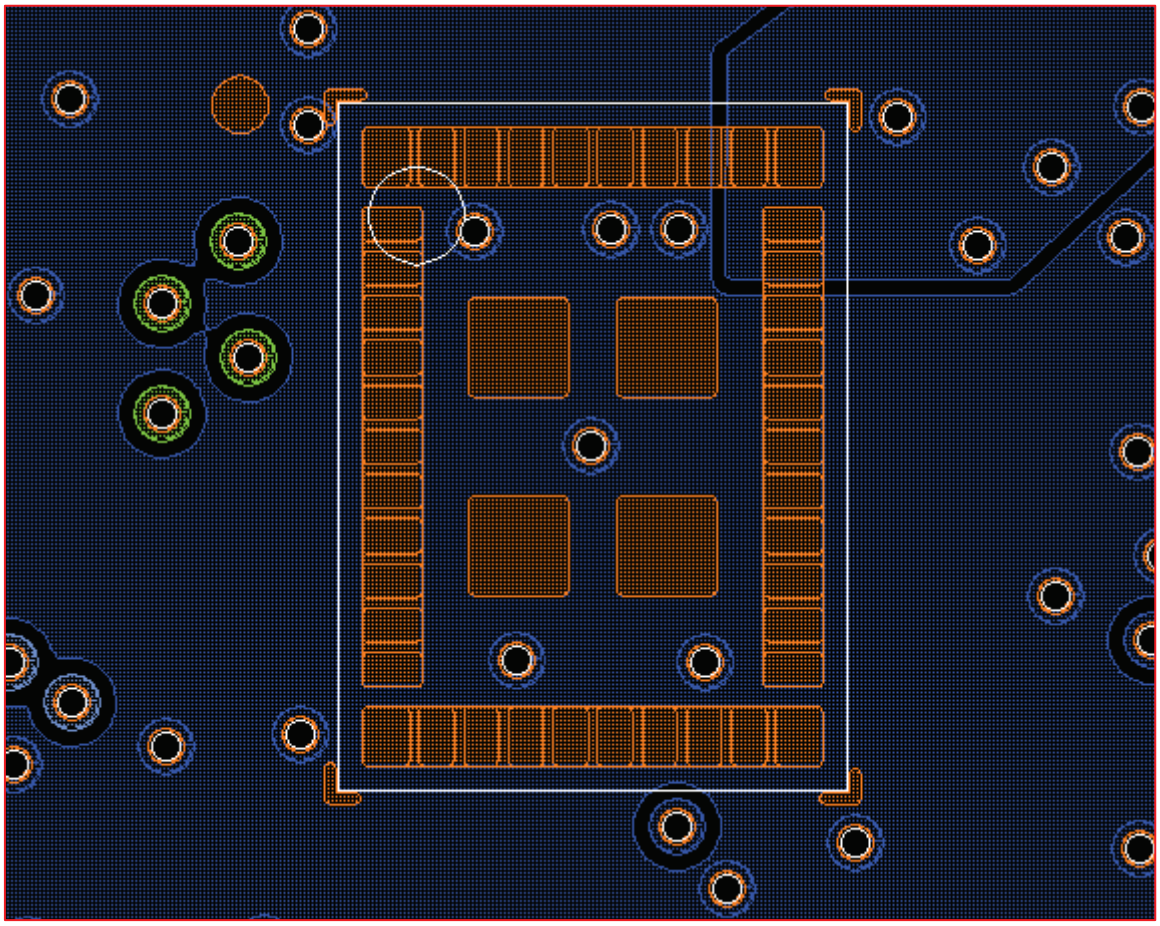
5 Hardware Design Guideline

This section describes the hardware design procedure.

5.1 Underneath of Module

Figure 4 shows the structure of the module from underneath.

Figure 4: Underneath of Module



Do not arrange any lines under the module to avoid deteriorations of RF performance. (All GND plane)

5.2 Antenna Design

Antenna line should be 50 ohms (*). There should be enough GND via along with Antenna line. Make sure that pi matching circuit is located right before the Wi-Fi antenna on the main board.

Users must perform the antenna design that followed the specifications of the antenna.

The following three points must be ensured while testing the antenna design:

1. It is the same type as the antenna type of antenna specifications.
   - Confirm the same size as the Gerber file.

2. An antenna gain is lower than a gain given in antenna specifications.
   - Measure the gain, and confirm the peak gain is less than the application value (1.4 dBi)
3. The emission level is not getting worse.
   - Measure the spurious and confirm degradation of less than 3 dB than spurious value of worst of report used for the application. However, it is spurious defined below.

Please send these reports to Murata.

Figure 5 shows the antenna line of Type 1DX.

Figure 5: Antenna Line

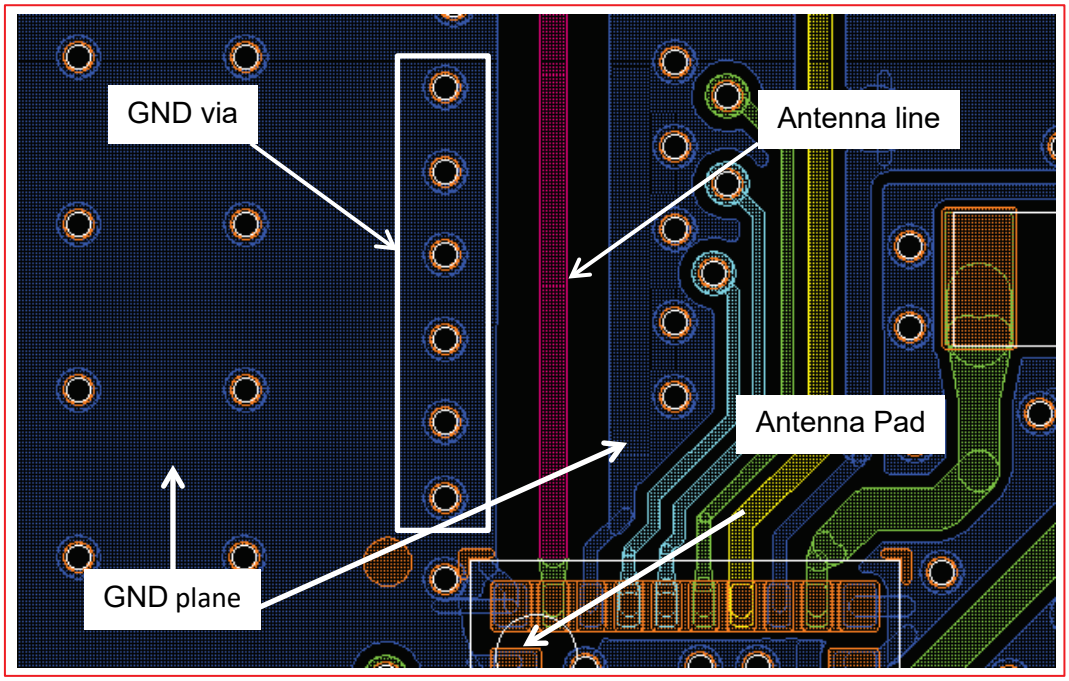
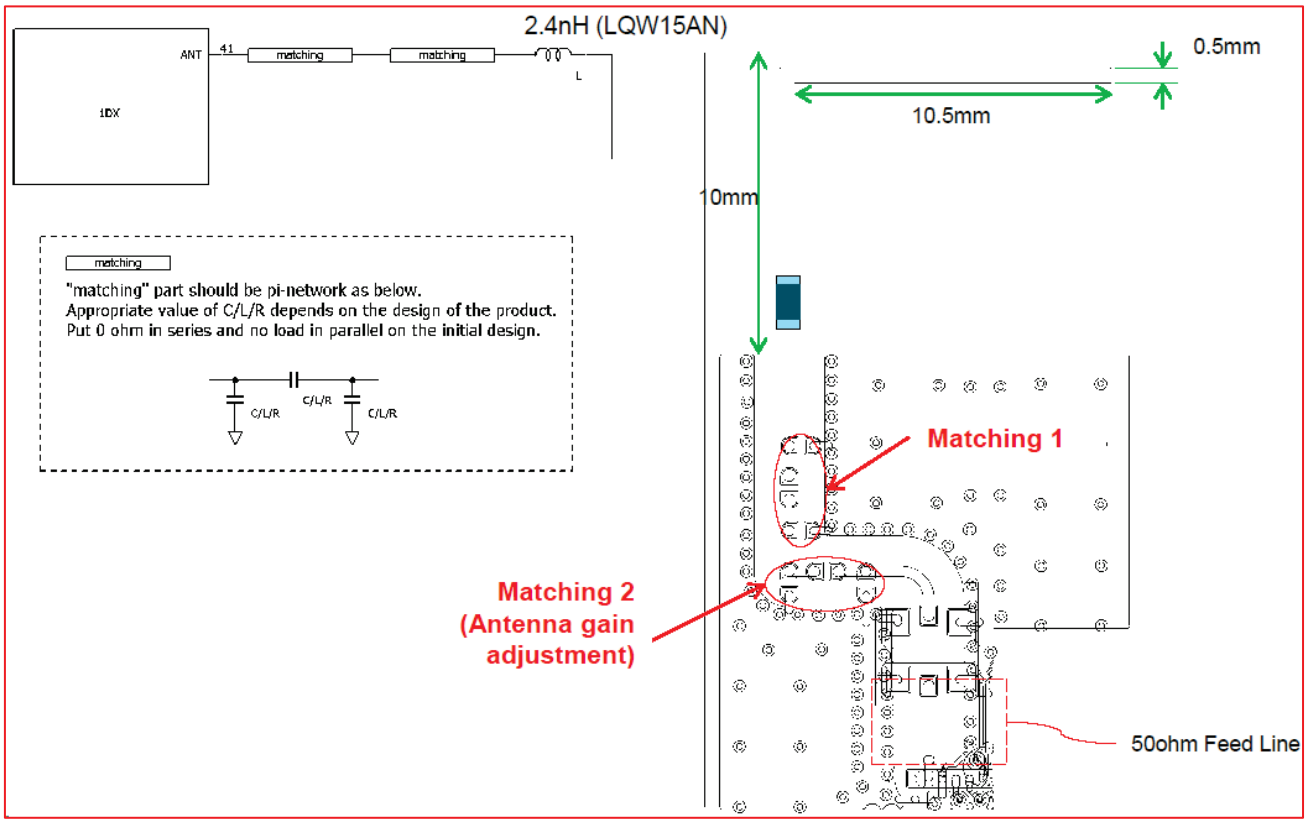


Figure 6 shows the antenna design of Type 1DX module.

Figure 6: Antenna Design



Please follow type1dx_antenna_p2ml4452-1.dxf.

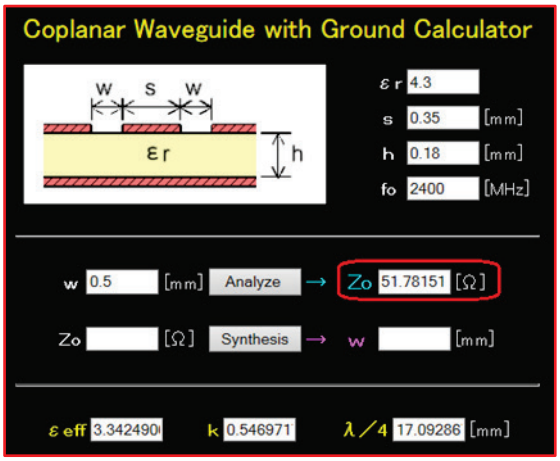
To know how to make 50-ohms line, refer to: I-Laboratory

An example of the conditions of 50-ohm lines of evaluation board is as below:

- Epsilon: 4.3
- RF trace width(s): 0.35 mm
- GND gap(h): 0.18 mm
- GND gap(w): 0.5 mm
- The line impedance is Z0 = 51.8 ohms.

The evaluation board is shown in **Figure 7**.

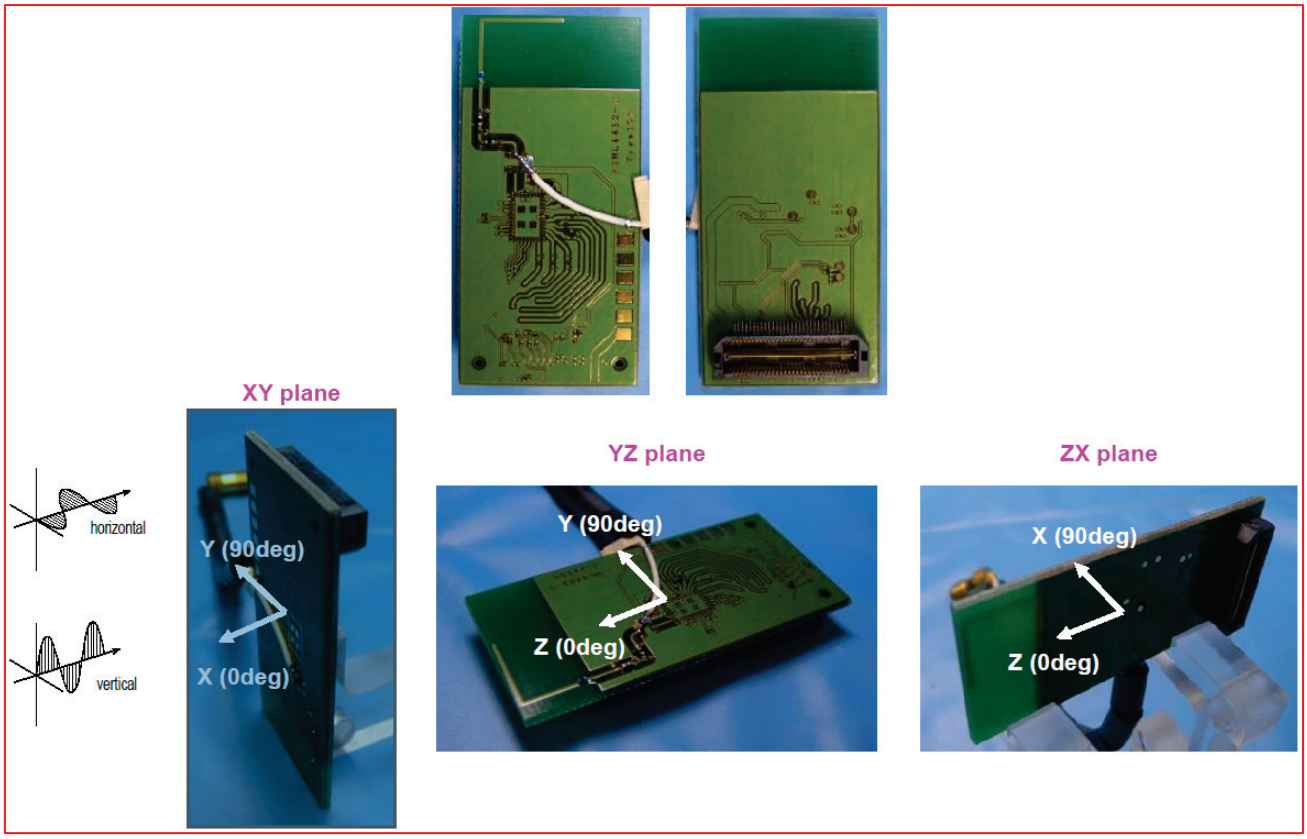
Figure 7: Coplanar Waveguide



5.3 Measurement Board

Figure 8 shows the measurement board.

Figure 8: Measurement Board



5.4 Antenna Performance

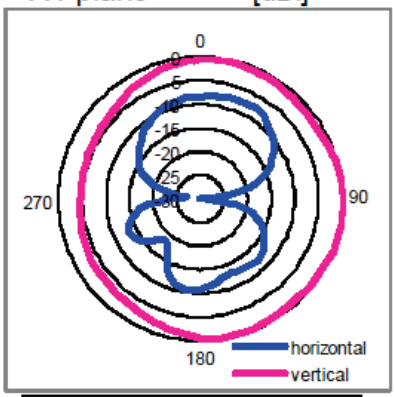
Figure 9 shows the antenna performance of 1DX module.

Figure 9: Antenna Performance

[dBi] [dB]

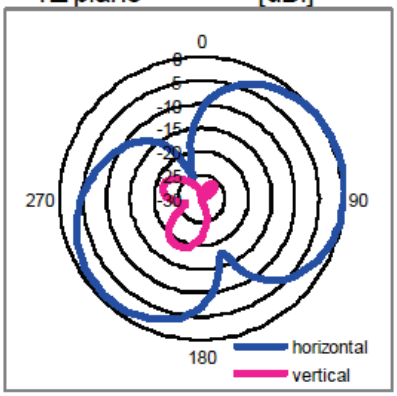
LINEAR POLARIZATION		XY-plane hor.	XY-plane ver.	YZ-plane hor.	YZ-plane ver.	ZX-plane hor.	ZX-plane ver.	Total Efficiency
2400 MHz	MAX.	-7.9	0.0	0.3	-21.4	-0.4	-7.1	
	AVE.	-12.3	-1.5	-3.6	-26.0	-4.5	-9.1	-2.4
2442 MHz	**MAX.**	**-7.5**	**0.3**	**0.6**	**-18.8**	**-0.4**	**-6.8**	
	AVE.	**-12.0**	**-1.4**	**-3.4**	**-24.5**	**-4.3**	**-8.9**	**-2.3**
2484 MHz	MAX.	-7.1	0.4	0.5	-18.3	0.1	-6.4	
	AVE.	-11.5	-1.3	-3.6	-23.5	-4.1	-8.7	-2.2

XY plane [dBi]



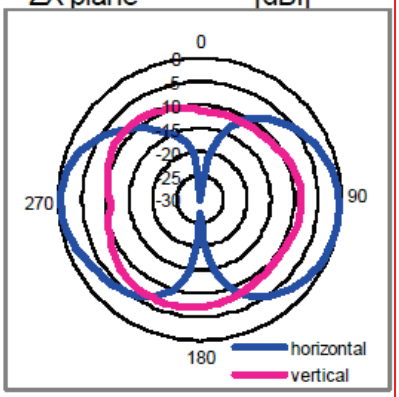
	HOR.	VER.
MAX	-7.5	0.3
AVE	-12.0	-1.4

YZ plane [dBi]



	HOR.	VER.
MAX	0.6	-18.8
AVE	-3.4	-24.5

ZX plane [dBi]



	HOR.	VER.
MAX	-0.4	-6.8
AVE	-4.3	-8.9

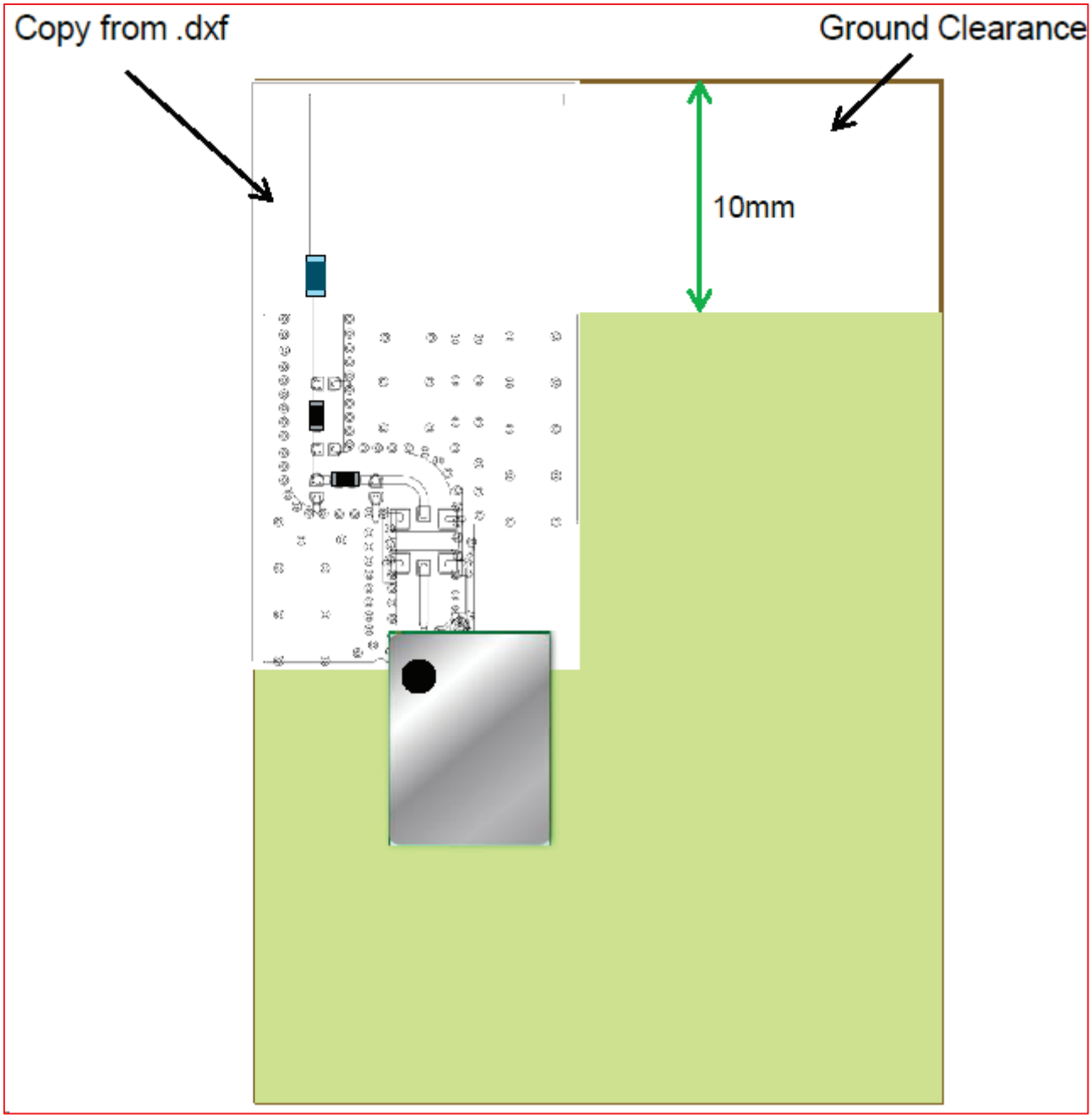
Antenna Type: Monopole (pattern antenna)
Antenna Gain: 0.6 dBi (peak)

5.5 Layout Guide for Good Antenna Performance

Please follow the layout guide for good antenna performance as listed below and in **Figure 10.**

- Place the antenna on top-left corner.
- Keep GND clearance all long the top edge.
- Place metal stuff as far as possible.
- Place two pi-network for matching and attenuating.
- Put 0ohm in series and no load in parallel on the initial design.
- Put appropriate value of C/L/R depends on actual performance.

Figure 10: Antenna Layout Guide



5.6 VBAT/CBUCK line

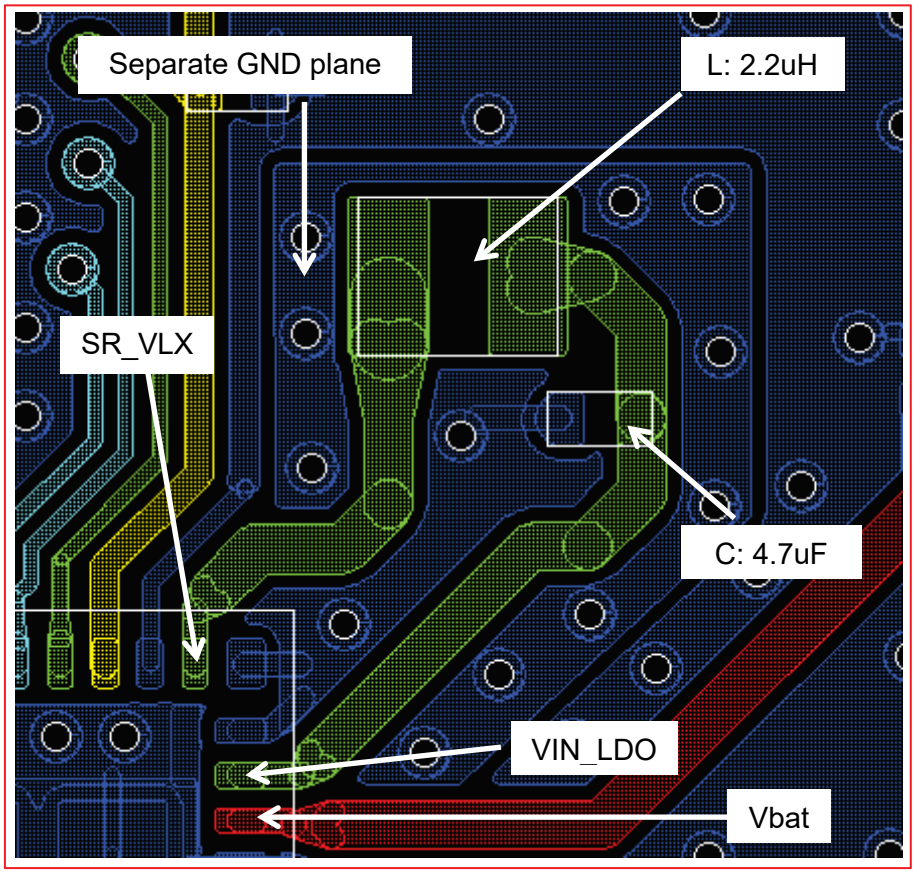
Make the line from SR_VLX to VIN_LDO as short as possible. 4.7uF capacitor should be as close to VIN_LDO as possible.

If the main board is multilayer PCB type, it's better to separate the GND place for this area on the top later, then connect it to the main GND thru the via hole on the lower layer.

On VBAT line, 4.7uF bypass capacitor should be located as close to the module as possible.

The VBAT/BUCK line is shown in **Figure 11**.

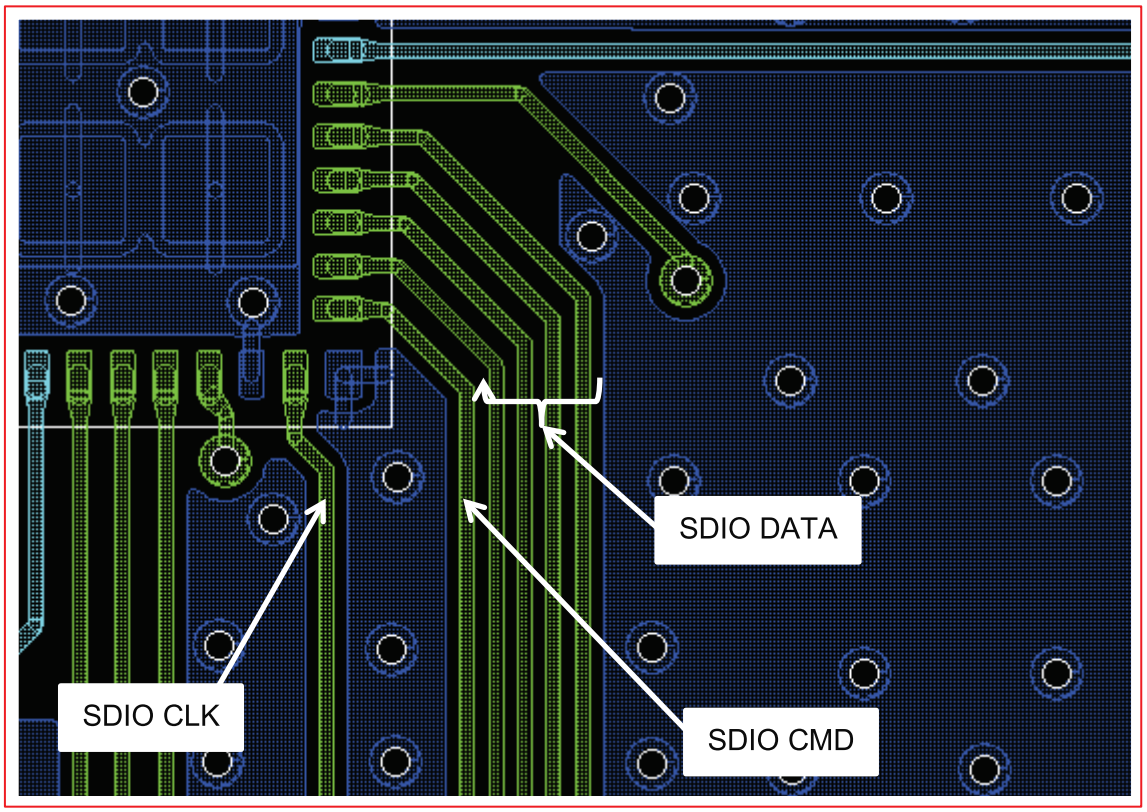
Figure 11: VBAT/CBUCK Line



5.7 SDIO - Line1

Keep the space between SDIO_CMD line and SDIO_CLK line as much as possible to avoid coupling as shown in **Figure 12**.

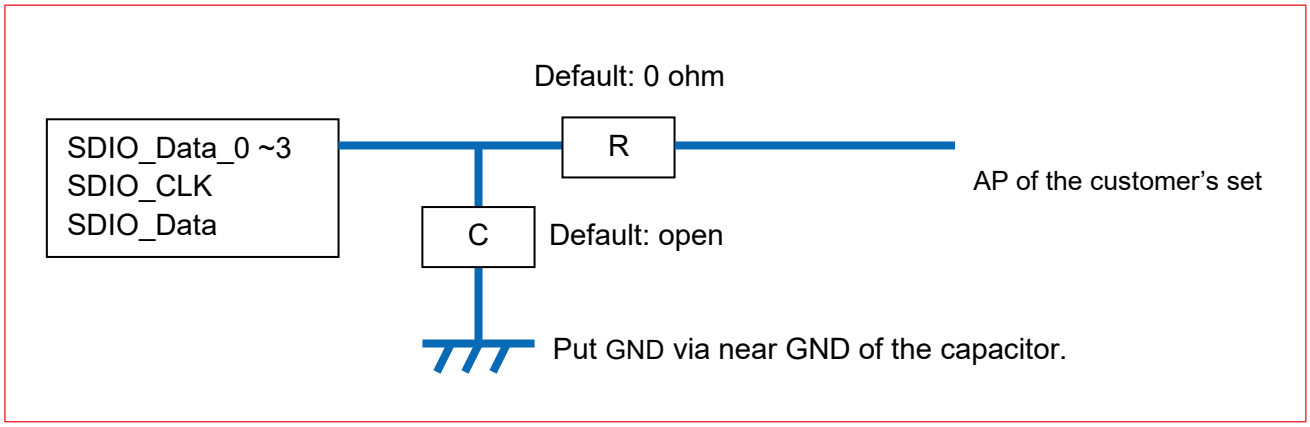
Figure 12: SDIO - Line 1



5.8 SDIO - Line 2

Arrange SDIO lines with 50 ohm and put R, C parts, just in case, to reject the noise as follows if the space is allowed (**Figure 13**). These lands can be used as test pad for the debug purpose as well.

Figure 13: SDIO - Line 2

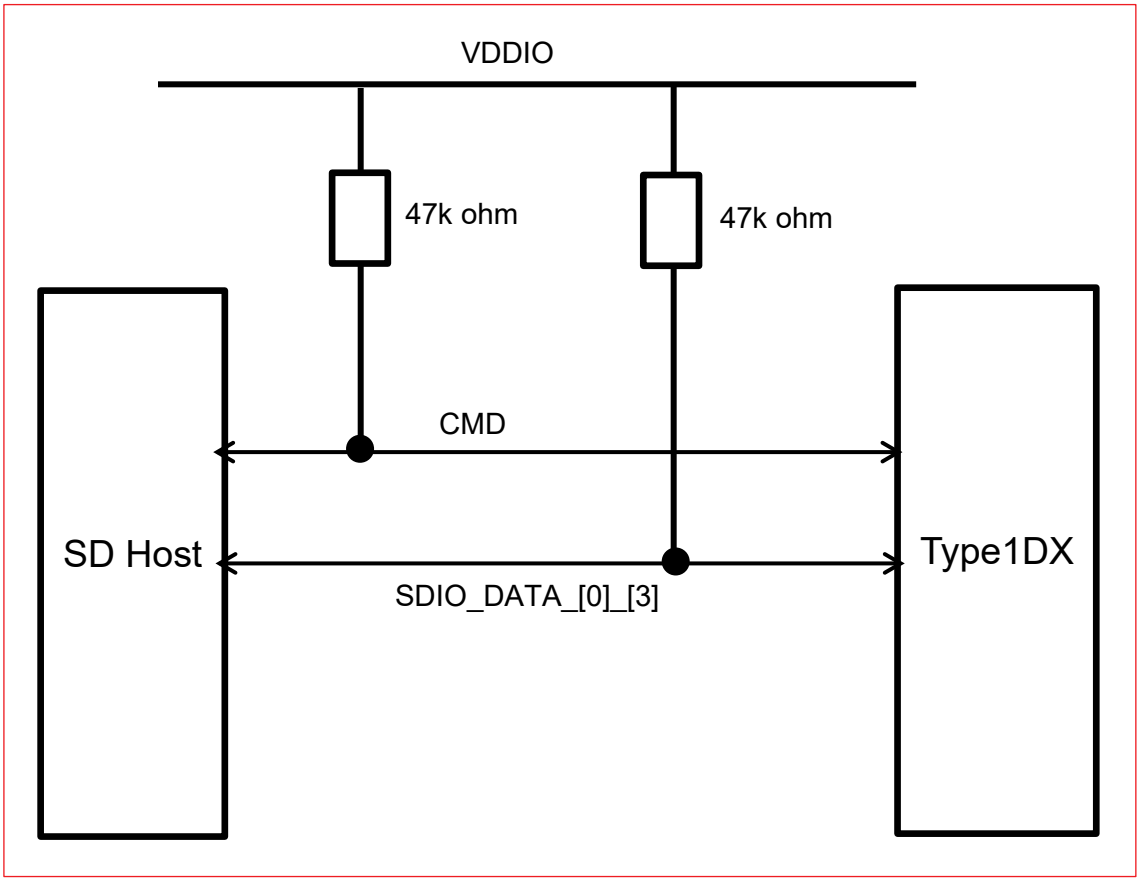


5.9 SDIO - Line 3

10 to 100k ohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resisters or properly programming internal SDIO Host pull-ups. This module (Type 1DX) does not have internal pull-ups on these lines inside module.

The SDIO Line 3 configurations are shown in **Figure 14**.

Figure 14: SDIO - Line 3



6 RF Characteristics - Conducted Tests

This section describes:

- Tx output power level (at module antenna port)
- Rx minimum sensitivity level (at module antenna port)

6.1 Tx Output Power Level (at Module Antenna Port)

- Wi-Fi 2.4GHz - 11b: 17 dBm, 11g: 13 dBm, 11n: 12 dBm
- BT - 8 dBm (typical),
- BLE - 8 dBm (typical)

6.2 Rx Minimum Sensitivity Level (at Module Antenna Port)

- Wi-Fi 2.4GHz - 11b -11 Mbps: -89 dBm (typical), 11g - 54 Mbps: -75 dBm (typical), 11n - MCS7 HT20: -73 dBm (typical)
- BT - BDR DH5: -91 dBm (typical), EDR 2DH5: -94 dBm (typical), EDR 3DH5: -87 dBm (typical)
- BLE: -95 dBm (typical)

7 Power Consumption

This section describes the current consumption conditions and parameters for Wi-Fi and Bluetooth.

7.1 Wi-Fi Current Consumption (VBAT = 3.6V, VDDIO = 3.3V)

Condition: WL_REG_ON: High, BT_REG_ON: Low

Table 3: Current Consumption - Wi-Fi

Mode	Rate	Typical: Vbat: 3.6V, VIO: 3.3V, 25^{0}C	
		Vbat (mA)	VIO (uA)
Sleep Mode			
Leakage (off)	N/A	0.005	1
Sleep (Idle)	N/A	0.008	251
IEEE PS DTIM3	N/A	0.7	
Active Mode			
Rx active (1024byte, 20usec interval)	11b 11Mbps	47	
	11g 54Mbps	47	
	11n MCS7	47	
Tx (1024byte, 20usec interval)	11b@ 17 dBm	320	
	11g@ 13 dBm	270	
	11n@ 12 dBm	260	

7.2 Bluetooth Current Consumption (VBAT = 3.6V, VDDIO = 3.3V)

Condition: WL_REG_ON: Low, BT_REG_ON: High

Table 4: Current Consumption - Bluetooth

Operation **Mode**	**Typical: Vbat: 3.6V, VIO: 3.3V, 25^{0}C**		
	Vbat	**VIO**	**Unit**
Bluetooth 2.1 + EDR			
BDR DH5	28		mA
EDR 2DH5	25		mA
EDR 3DH5	25		mA
Bluetooth 4.0			
Sleep (Idle)	20	107	uA
Inquiry Scan (1.28s)	275	180	uA
Tx @ 7.5 dBm	34		mA
Rx	13.4		mA

8 Throughput Performance

This section describes the throughput performance as listed below:

- Measurement conditions
- Measurement Results

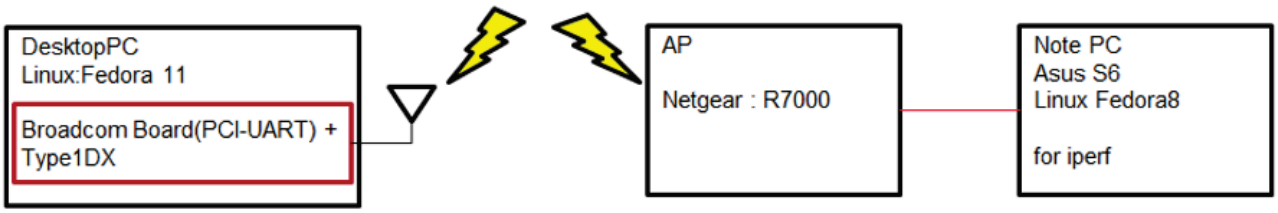
8.1 Measurement Conditions

Measurement Conditions are listed below:

- Kernel**:** 2.6.29.4-167
- Driver version**:** 1.141.64.8
- FW version**:** 7.10.48.1
- Nvram: nvram_4343s_4343w_37M4_normal_power_1030.txt

The measurement conditions are shown in **Figure 15**.

Figure 15: Test Environment



8.2 Measurement Results

The measurement results are shown in **Table 5**.

Table 5: Measurement Results

2.4GHz 11n (MCS7 HT20)		Tx [Mbps]	Rx [Mbps]	CH
	HT20	46.4	51.2	7

9 References

Table 6 reviews all the key reference documents that the user may like to refer to.

Table 6: Reference Table

Support Site	Notes
Murata Type 1DX Module Datasheet	Murata Type 1DX module datasheet (type1dx.pdf)
Murata Type 1DX Module Footprint	Murata Type 1DX module footprint (type1dx-module-footprint-topview.dxf)
Murata Type 1DX Antenna	Murata Type 1DX module trace antenna (type1dx_antenna_p2ml4452-1.dxf)
Linux WLAN Configuration	Murata GitHub link for Linux NVRAM file for 1DX
Linux WLAN Regulatory Configuration	Murata GitHub link for Linux CLM_BLOB file for 1DX
Linux User Guide	Murata Linux User Guide for Infineon modules (Murata Wi-Fi & BT (IFX) Solution for i.MX Linux User Guide.pdf).
I-Laboratory	Link for I-Laboratory

10 Technical Support Contacts

Table 7 lists all the support resources available for the Murata Wi-Fi/BT solution.

Table 7: List of Support Resources

Support Site	Notes
Murata Community Forum	**Primary support point for technical queries.** This is an open forum for all customers. Registration is required.
Murata i.MX Landing Page	No login credentials required. Murata documentation covering hardware, software, testing, etc. is provided here.
Murata uSD-M.2 Adapter Landing Page	Landing page for uSD-M.2 Adapter. In conjunction with Murata i.MX Landing Page, this should provide the user with comprehensive getting started documentation.
Murata Module Landing Page	No login credentials required. Murata documentation covering all Infineon-based Wi-Fi/BT modules is provided here.

Revision History

Revision	Date	Section	Change Description
1.0	July 21, 2015		First Issue
2.0	August 06, 2015	Header/Footer	Revised the description
3.0	Jan 10, 2017	4.0 Reference BOM	Revised Inductor P/N (4)
4.0	Jan 04, 2018		Changed IC PN from BCM4343W to CYW4343W
5.0	Apr 05, 2019	4.0 Reference BOM	Revised Inductor P/N (4) LQM18PN2R2MGH L->LQM18PN2R2MGH
6.0	Jun 06, 2022		Revision of silicon vendor name BT version is revised.
7.0	Nov 02, 2023		Converted to new format.