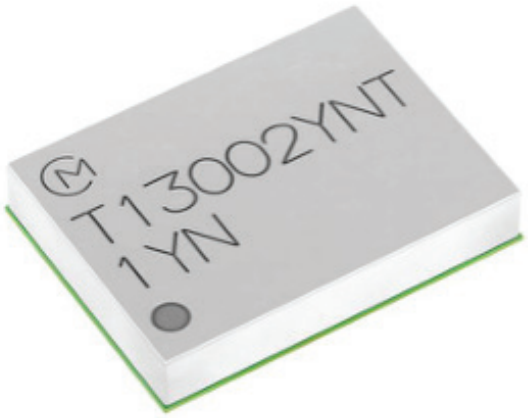
Hardware Application Note

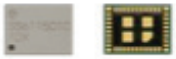
Wi+Fi® + Bluetooth® Combo Module

Infineon CYW43439 Chipset v5.2 for 802.11b/g/n + Bluetooth 5.2

Hardware Application Note - Rev. 3.0

- Design Name: Type 1YN
- Module P/N: LBEE5KL1YN





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About This Document

This application note covers HW development and provides how to design the schematic and layout, and reference RF performance. Refer to Type 1YN Datasheet for Module specification.

Audience & Purpose

This document is targeted towards system integrators for Wi-Fi/Bluetooth solutions using Murata Type 1YN (CYW43439) module, based on IFX CYW43439 chipset.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Module Introduction Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Module Introduction

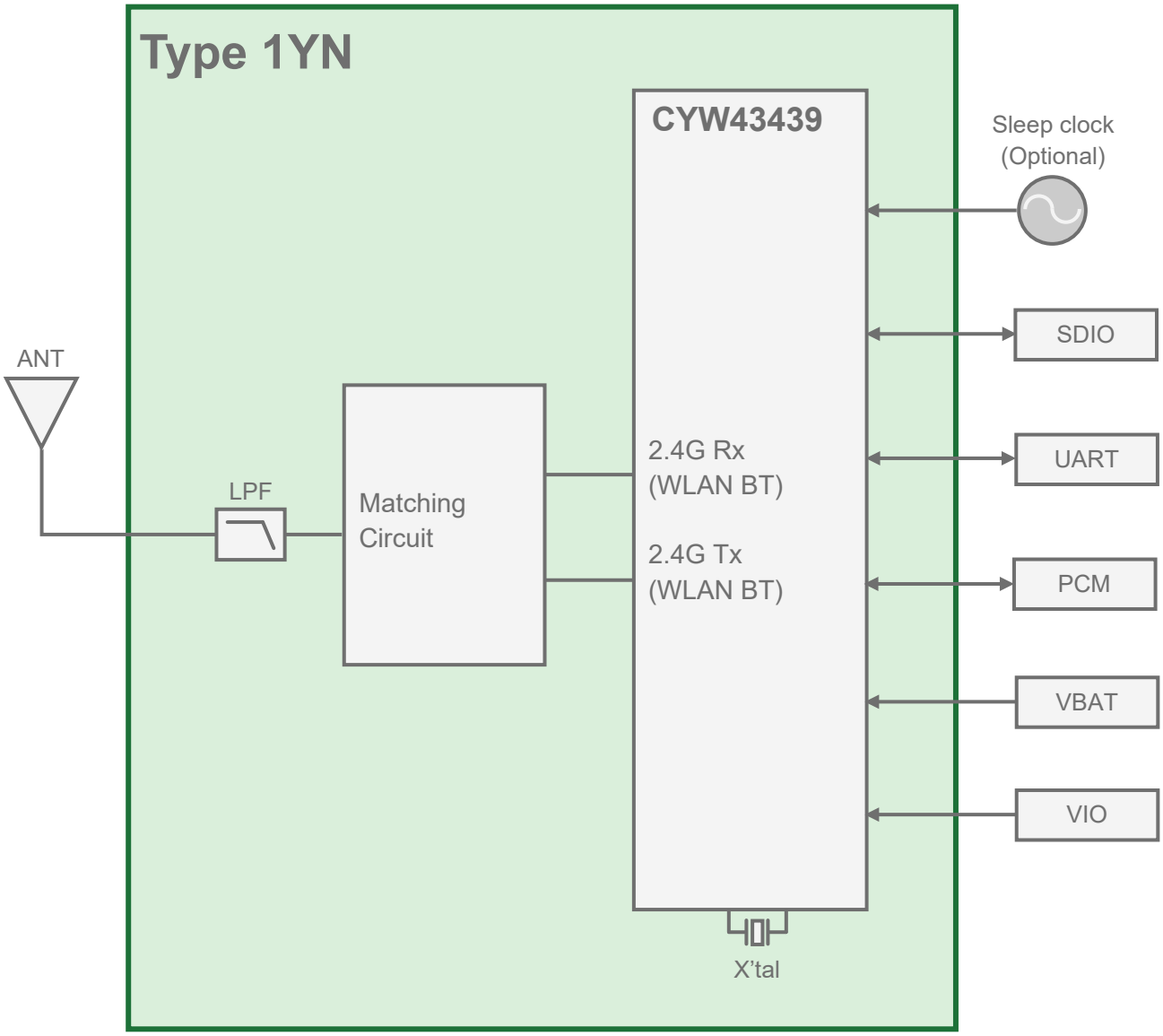
Type 1YN (1x1) is Wi-Fi + BT/BLE combo SIP module with Broadcom CYW43439, which is single-chip 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/Baseband/Radio, Bluetooth 5.2 support chip. (See Type 1YN Datasheet).

There are LPF and matching circuit in front of CYW43439 chipset. Ant port is tuned as 50 ohms output. Fast clock (X'tal) is also embedded. Some external components will be required to complete Wi-Fi/BT/BLE circuit. This module is covered with resin molding and fully shielded with metal. The package type is LGA (SMD type).

2 Hardware Block Diagram

The module internal block diagram is shown in **Figure 1**.

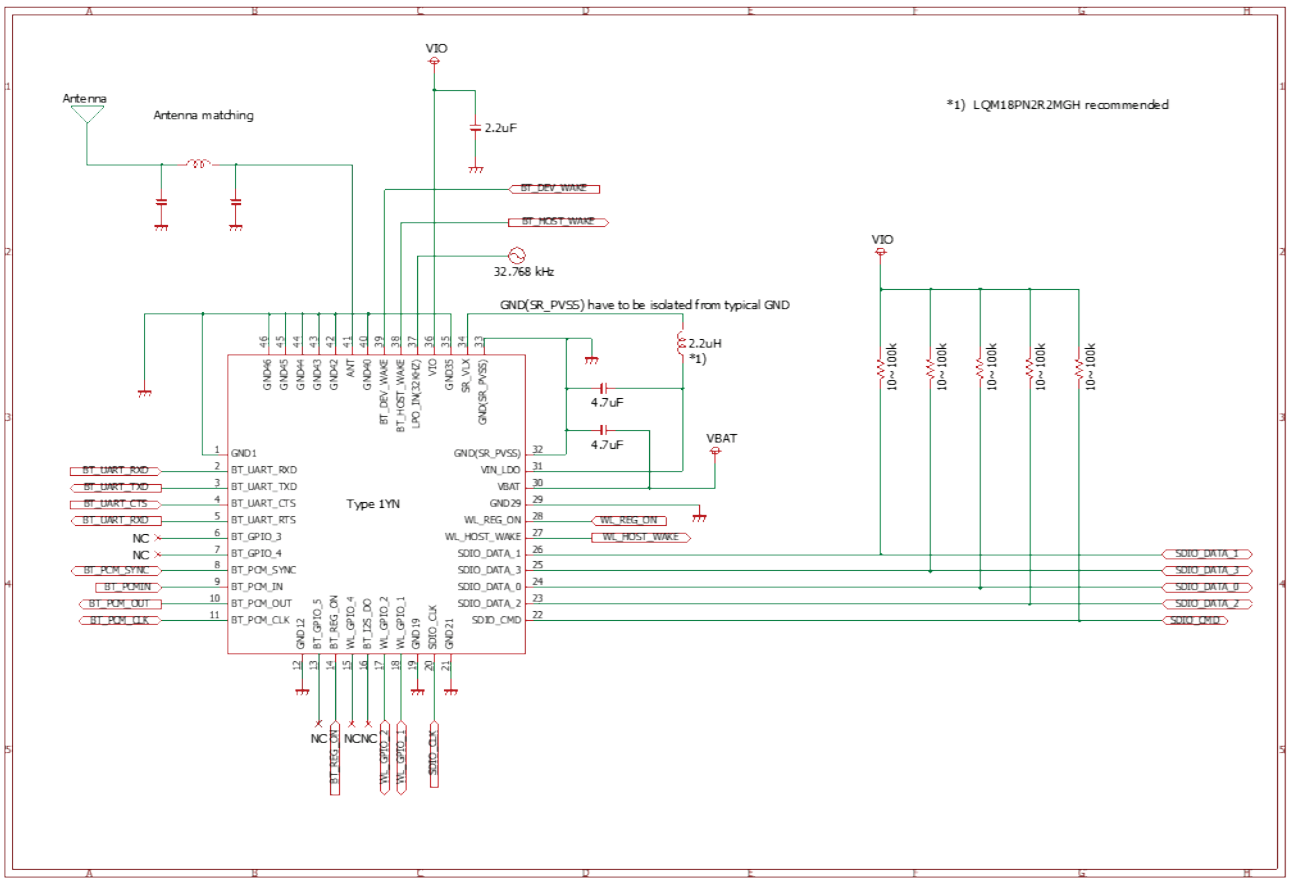
Figure 1: Block Diagram



3 Reference Circuit

Figure 2 shows the reference circuit design for Type 1YN module.

Figure 2: Reference Circuit



4 External BOM List (Reference)

Figure 3 shows the external BOM list diagram and **Table 2** describes the list of external components.

Figure 3: External BOM List (Reference)

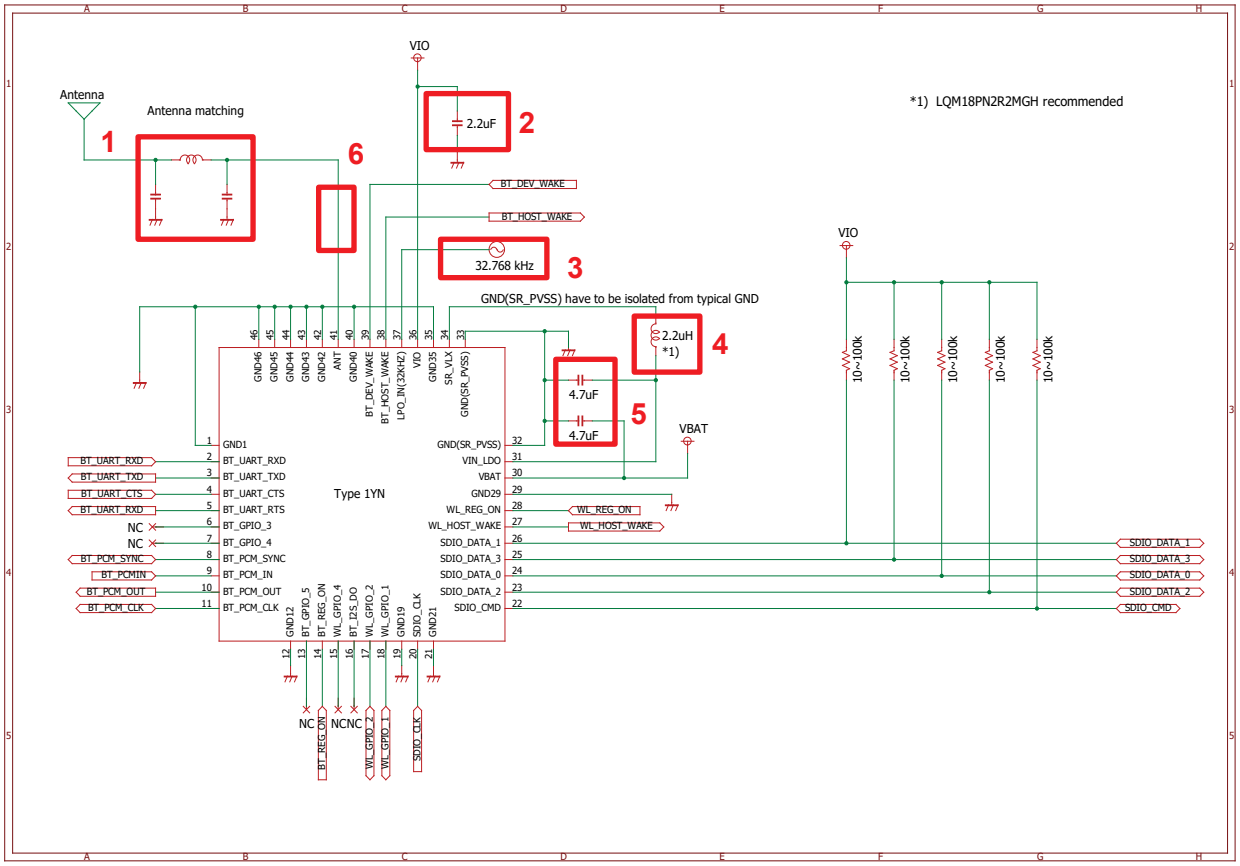


Table 2: External BOM list Description

Block	Components	Value	Pieces	Note
1	L or C	TBD	3	Depend on PCB structure / design (for Antenna matching)
2	C	2.2 uF	1	
3	LPO	32.768 kHz	1	Pls see the required spec on the module datasheet
4	L	2.2uH	1	LQM18PN2R2MGH recommended. (1.05 A, DCR = 0.25 ohm)
5	C	4.7uF	2	4.7uF
6	Connector	-	1	In case of testing RF conductive performance. (Right next to the module)

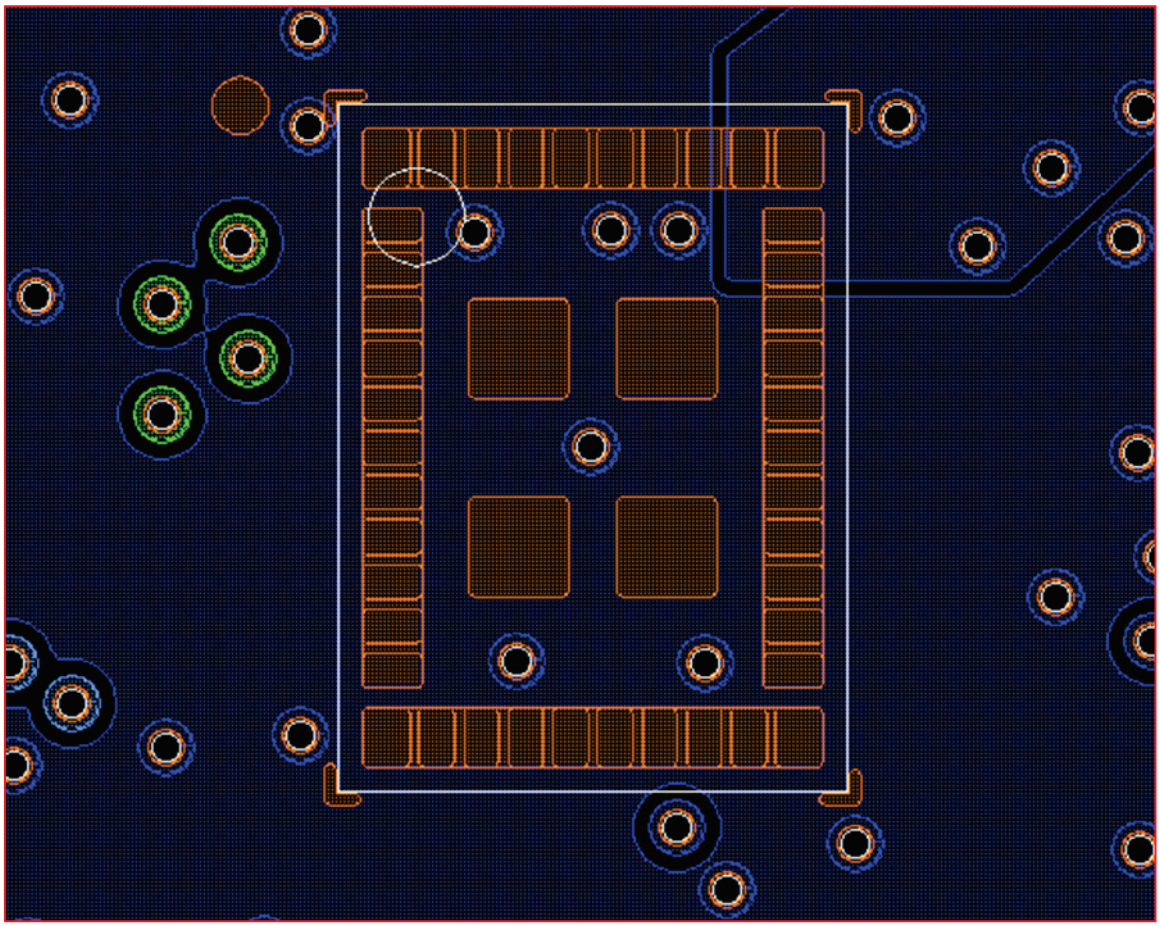
5 Hardware Design Guidelines

The hardware design guidelines include guidelines on underneath of module design, antenna line, VBAT/CBUCK line, SDIO line 1, 2, and 3.

5.1 Underneath of Module

Do not arrange any lines under the module to avoid deteriorations of RF performance. (All GND plane). **Figure 4** shows the design for underneath of the module.

Figure 4: Underneath of Module Design

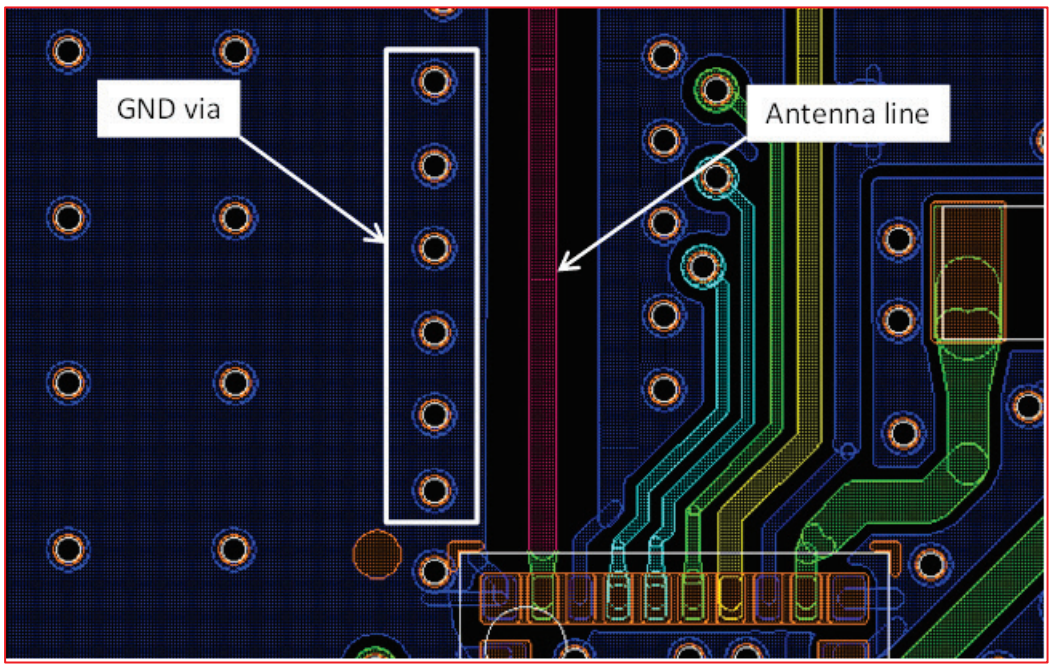


5.2 Antenna Line

The guidelines for antenna line are:

1. The antenna line should be of 50ohm (*) and there should be enough GND via along with Antenna line.
2. Make sure that the pi matching circuit is located right before the Wi-Fi antenna on the main board. The antenna line design is shown in **Figure 5**.

Figure 5: Antenna Line

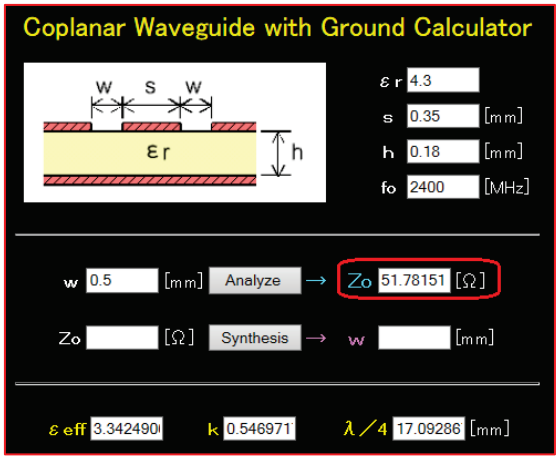


To know how to make 50ohm line see I-Laboratory.

Here is one example of the conditions of 50ohm lines of evaluation board:

- Epsilon: 4.3
- RF trace width(s): 0.35mm
- GND gap(h): 0.18mm
- GND gap(w): 0.5mm
- The line impedance is Z0 = 51.8ohm.

Figure 6: Coplanar Waveguide with Ground Calculator



Please perform the antenna design that followed the specifications of the antenna. The concrete contents of a check are the following three points:

1. It is the same type as the antenna type of antenna specifications. Confirm the same size as the Gerber file.
2. An antenna gain is lower than a gain given in antenna specifications. Measure the gain, and confirm the peak gain is less than the application value (1.4 dBi)
3. The emission level is not getting worse. Measure the spurious and confirm degradation of less than 3 dB than spurious value of worst of report used for the application.

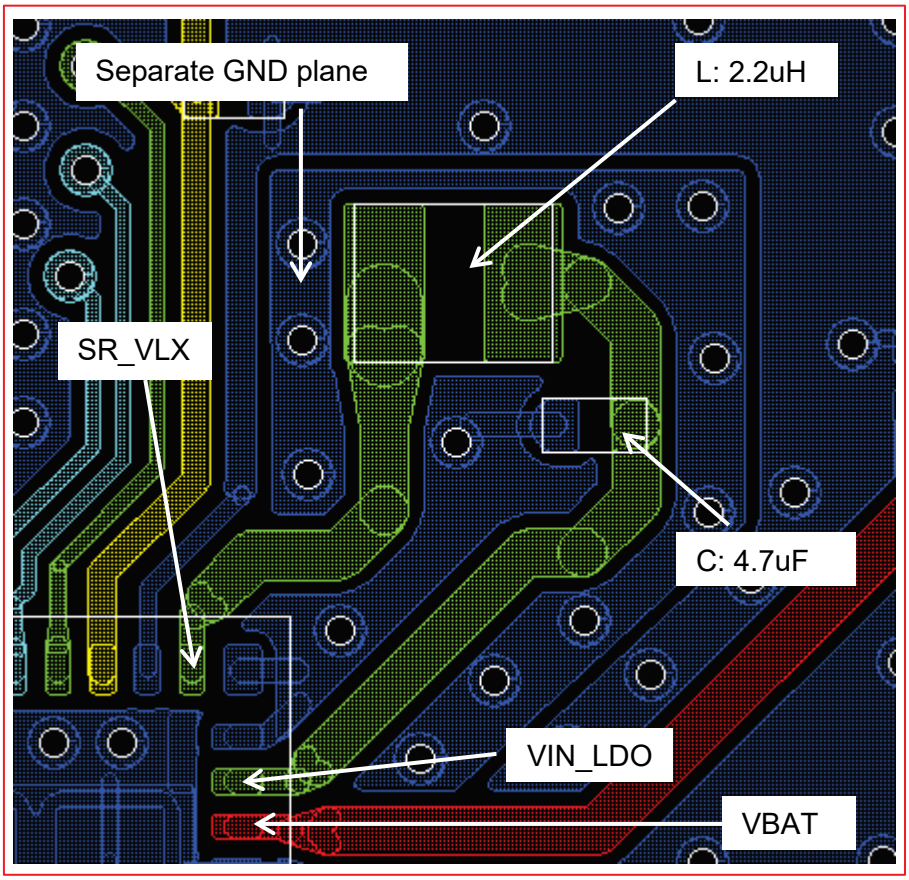
Please send those reports to Murata.

5.3 VBAT/CBUCK Line

The guidelines are:

- Make the line from SR_VLX to VIN_LDO as short as possible. The 4.7uF capacitor should be as close to VIN_LDO as possible.
- If the main board is multilayer PCB type, it's better to separate the GND place for this area on the top later, then connect it to the main GND thru the via hole on the lower layer.
- On VBAT line, 4.7uF bypass capacitor should be located as close to the module as possible.

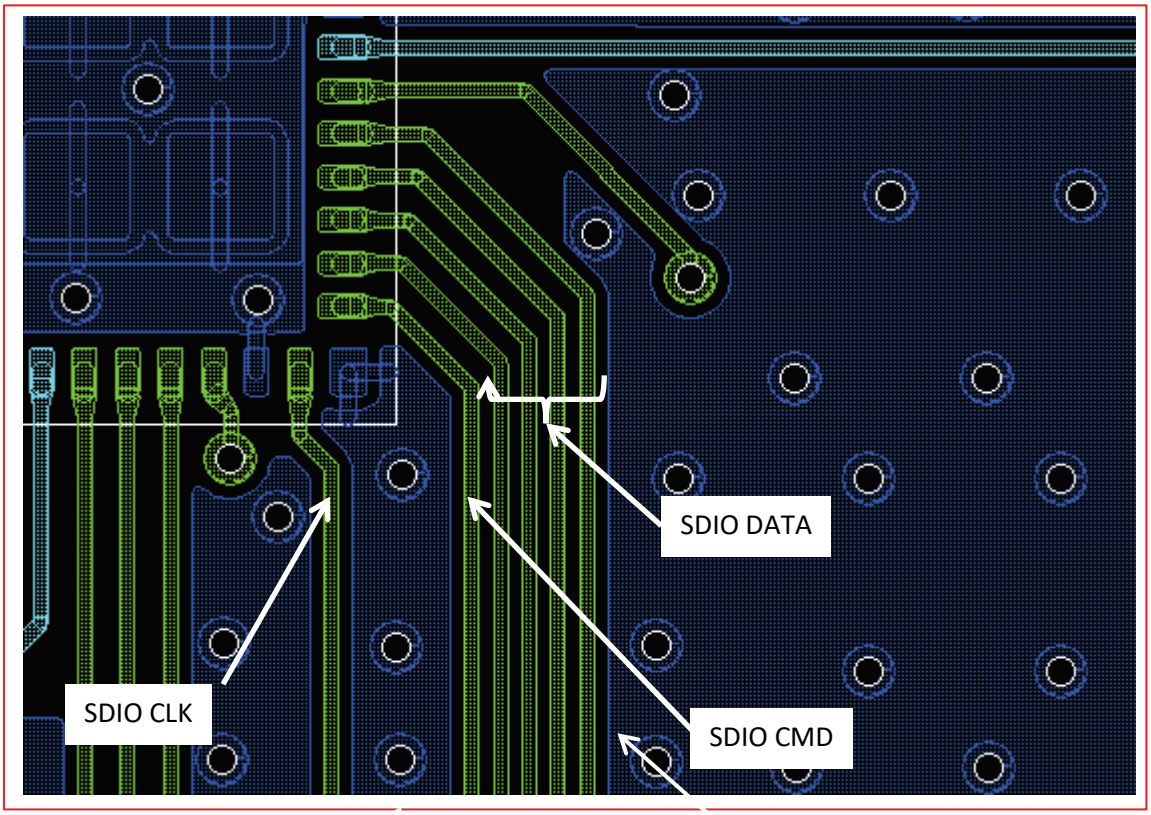
Figure 7: VBAT/CBUCK Line



5.4 SDIO Line -1

Keep the space between SDIO_CMD line and SDIO_CLK line as much as possible to avoid coupling. Refer to **Figure 8** for SDIO Line 1 design.

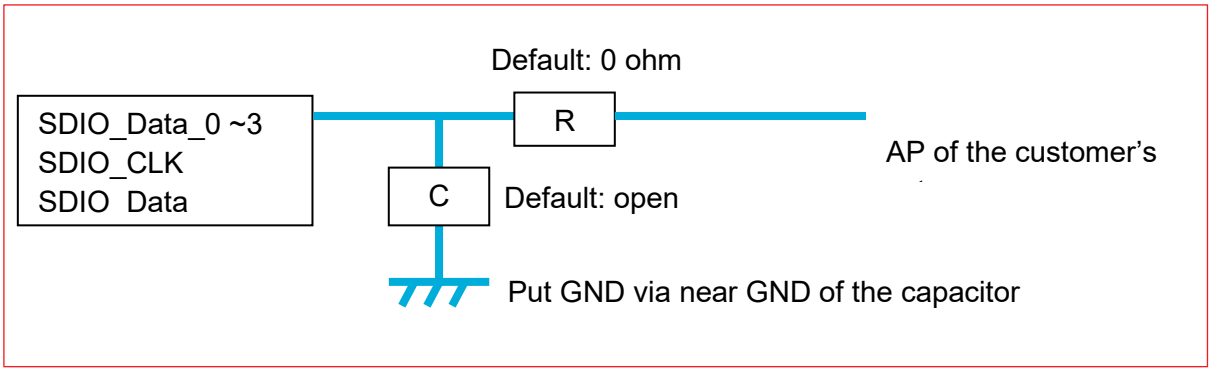
Figure 8: SDIO Line - 1 Design



5.5 SDIO Line 2

Arrange SDIO lines with 50 ohm and put R, C parts, just in case, to reject the noise as follows if the space is allowed. These lands can be used as test pad for the debug purpose as well. Refer to **Figure 9** for SDIO Line 2 design.

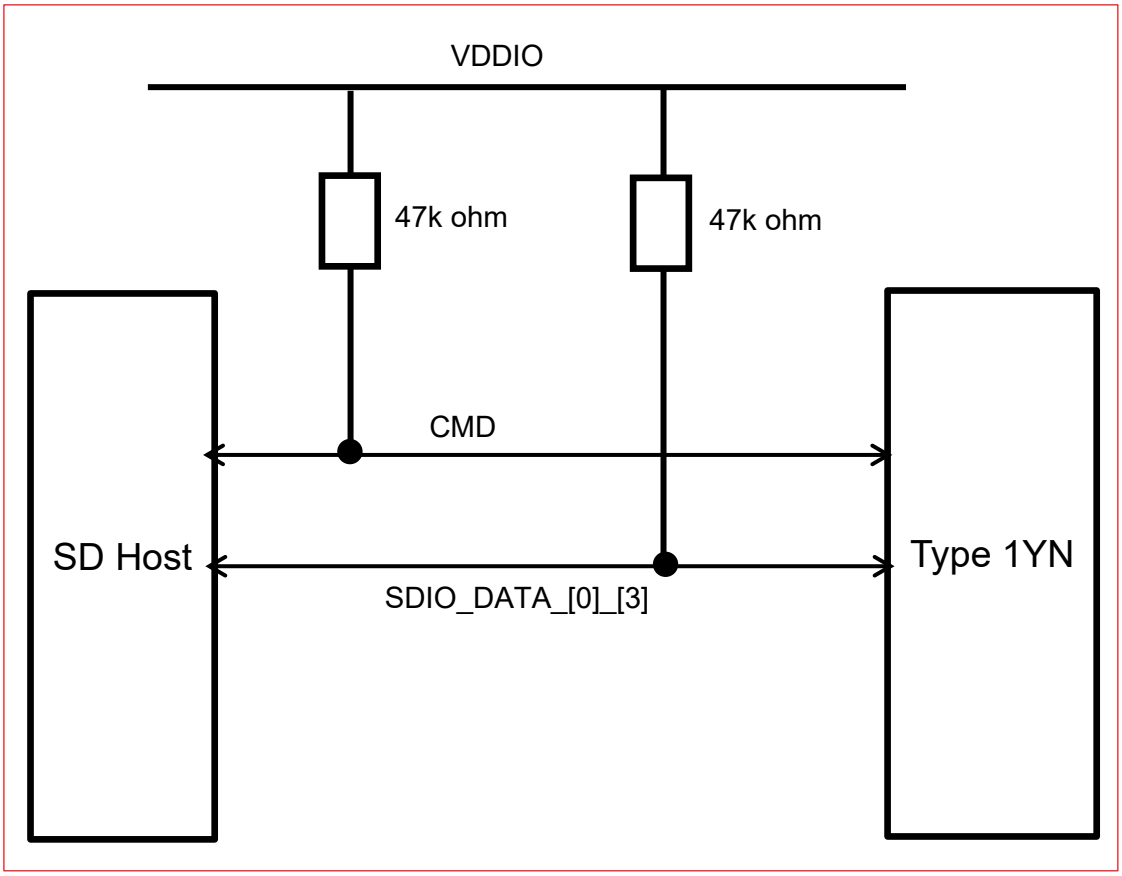
Figure 9: SDIO Line 2 Design



5.6 SDIO Line 3

10 to 100k ohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resisters or properly programming internal SDIO Host pull-ups. This module (Type 1YN) does not have internal pull-ups on these lines inside module. Refer to **Figure 10** for SDIO Line 3 design.

Figure 10: SDIO Line 3 Design



6 RF Characteristics – Conducted Test

This section described the RF characteristics, i.e., Tx output power level and Rx minimum sensitivity level at antenna port.

6.1 Tx Output Power Level (at Module Antenna Port)

Conditions:

- Wi-Fi 2.4 GHz - 11b: 17 dBm, 11g: 13 dBm, 11n: 12 dBm
- BT - 8 dBm (typical),
- BLE - 8 dBm (typical)

6.2 Rx Minimum Sensitivity level (at Module Antenna Port)

Conditions:

- Wi-Fi 2.4 GHz - 11b -11 Mbps: -89 dBm (typical), 11g - 54 Mbps: -75 dBm (typical), 11n - MCS7 HT20: -73 dBm (typical)
- BT - BDR DH5: -91dBm (typical), EDR 2DH5: -94dBm (typical), EDR 3DH5: -87dBm (typical)
- BLE - -95dBm (typical)

7 Power Consumption

This section describes the Wi-Fi and Bluetooth power consumptions.

7.1 Wi-Fi Current consumption (VBAT = 3.6V, VDDIO = 3.3V)

Conditions: WL_REG_ON: High, BT_REG_ON: Low

Table 3: Current Consumption - Wi-Fi

Mode	Rate	Vbat: 3.6V, VIO: 3.3V, 25^{0}C (Typical)	
		VBAT (mA)	VIO (uA)
Sleep Mode			
Leakage (off)	N/A	0.005	1
Sleep (Idle)	N/A	0.008	251
IEEE PS DTIM3	N/A	0.7	
Active Mode			
Rx active (1024 byte, 20 µs interval)	11b 11 Mbps	47	
	11g 54 Mbps	47	
	11n MCS7	47	
Tx (1024 byte, 20 µs interval)	11b@ 17 dBm	320	
	11g@ 13 dBm	270	
	11n@ 12 dBm	260	

7.2 Bluetooth Current Consumption (VBAT = 3.6V, VDDIO = 3.3V)

Conditions: WL_REG_ON: Low, BT_REG_ON: High

Table 4: Current Consumption - Bluetooth

Operation Mode	VBAT: 3.6V, VIO: 3.3V, 25^0.C (Typical)		
	VBAT	VIO	Unit
Bluetooth 2.1 + EDR			
BDR DH5	28		mA
EDR 2DH5	25		mA
EDR 3DH5	25		mA
Bluetooth 4.0			
Sleep (Idle)	20	107	µA
Inquiry scan (1.28s)	275	180	µA
Tx @ 7.5 dBm	34		mA
Rx	13.4		mA

8 References

Table 5 reviews all the key reference documents that the user may like to refer to.

Table 5: Reference Table

Support Site	Notes
Murata Type 1YN Module Datasheet	Murata Type 1YN module datasheet (type1yn.pdf)
Murata Type 1YN Module Footprint	Murata Type 1YN module footprint (type1yn-module-footprint-topview.dxf)
Murata Type 1YN Antenna	Murata Type 1YN module trace antenna (type1YN-antenna-p2ml4452-1.dxf)
Linux WLAN Configuration	Murata GitHub link for Linux NVRAM file for 1YN
Linux WLAN Regulatory Configuration	Murata GitHub link for Linux CLM_BLOB file for 1YN
Linux User Guide	Murata Linux User Guide for Infineon modules (Murata Wi-Fi & BT (IFX) Solution for i.MX Linux User Guide.pdf).
I-Laboratory	Link For I-Laboratory

9 Technical Support Contacts

Table 6 lists all the support resources available for the Murata Wi-Fi/BT solution.

Table 6: List of Support Resources

Support Site	Notes
Murata Community Forum	**Primary support point for technical queries.** This is an open forum for all customers. Registration is required.
Murata i.MX Landing Page	No login credentials required. Murata documentation covering hardware, software, testing, etc. is provided here.
Murata uSD-M.2 Adapter Landing Page	Landing page for uSD-M.2 Adapter. In conjunction with Murata i.MX Landing Page, this should provide the user with comprehensive getting started documentation.
Murata Module Landing Page	No login credentials required. Murata documentation covering all Infineon-based Wi-Fi/BT modules is provided here.

Revision History

Revision	Date	Section	Change Description
1.0	Nov 3, 2021		First Issue
2.0	Feb 21, 2022	Table of Contents	The table and contents corrected.
3.0	Nov 28, 2023		Converted to new format.

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