

## Communication Protocol Support

The D1U-H family of power supplies currently supports 3.3V-bus and 5V-bus standard-mode (100kHz) I<sup>2</sup>C Serial Communication as outlined in Philips Semiconductors 'The I<sup>2</sup>C Bus Specification Version 2.1' (January 2000).

The D1U-H family of power supplies can also support 3.3V-bus and 5V-bus SMBUS Serial Communication as outlined in the SBS Implementers forum 'System Management Bus (SMBUS) Specification Version 2.0' (August 2000)

D1U-H power supplies are configured to operate as slave-only devices.

# D1U-H Communications

## D1U-H-2800-52-HB1C Communications Protocol Application Note

The available address lines currently allows for communication with up to 8 D1U-H power supplies on a single serial communication bus.

Each D1U-H power supply contains a:

1. 2K serial EEPROM device used for FRU data storage (FRU data specs customer specific)
2. System-On-Chip (SOC) -type controller used for D1U-H status, fault, and parametric data reporting

## Serial Comm. Device Addressing

The D1U-H family of power supplies supports 8-bit addressing (7-bit slave address & LSB read/write bit).

The specified addressing is as follows:

Address Byte							
7	6	5	4	3	2	1	0
1	0	0	0	A2	A1	A0	R/W
<b>MSB</b>							<b>LSB</b>

Address lines A0 (LSB), A1, & A2 are internally connected to the standby bus (backplane) voltage through 7.5K pull-up resistors.

The address lines are pin-strapped (grounded or left open) on the backplane connectors to determine the unique 7-bit slave address assigned to each D1U-H slot in the backplane.

## Serial Comm. Read/Write Registers

On a host read request, the D1U-H power supplies transmits up to 14 8-bit registers that provide power supply status info, o/p fault indicators, and parametric data.

The 14 data registers are ordered as follows:

- |                      |   |
|----------------------|---|
| ■ Byte 0: Status0    | - Power supply operation status 0                                   |
| ■ Byte 1: Status1    | - Power supply operation status 1                                   |
| ■ Byte 2: Fault0     | - Power supply fault 0  |
| ■ Byte 3: Fault1     | - Power supply fault 1  |
| ■ Byte 4: Vout2      | - Upper (MSB) Byte of 10-bit representation of Main Output Voltage  |
| ■ Byte 4: Vout1      | - Lower (LSB) Byte of 10-bit representation of Main Output Voltage  |
| ■ Byte 6: Iout2      | - Upper (MSB) Byte of 10-bit representation of Main Output Current  |
| ■ Byte 7: Iout1      | - Lower (LSB) Byte of 10-bit representation of Main Output Current  |
| ■ Byte 8: Fan_Sense2 | - Upper (MSB) Byte of 10-bit representation of Fan Current          |
| ■ Byte 9: Fan_Sense1 | - Lower (LSB) Byte of 10-bit representation of Fan Current          |
| ■ Byte 10: PS_Temp2  | - Upper (MSB) Byte of 10-bit representation of Hot-spot temperature |
| ■ Byte 11: PS_Temp1  | - Lower (LSB) Byte of 10-bit representation of Hot-spot temperature |
| ■ Byte 12: Amb_Temp2 | - Upper (MSB) Byte of 10-bit representation of PCB temperature      |
| ■ Byte 13: Amb_Temp1 | - Lower (LSB) Byte of 10-bit representation of PCB temperature      |

On a host write request, the D1U-H power supply can receive a single byte command to specify the address offset of subsequent I<sup>2</sup>C read operation

The 1 command register is as follows:

- |  |  |
|--|--|
| ■ Byte 0: I <sup>2</sup> C Read Offset | - Address offset of subsequent I <sup>2</sup> C read operation, valid range is 0 to 13 |
|--|--|



For full details go to  
[www.murata-ps.com/rohs](http://www.murata-ps.com/rohs)

## Status/Fault Registers

Byte 0 - The D1U-H Status 0 register function and definitions are as follows:

BYTE 0 - Status Register							
7	6	5	4	3	2	1	0
PS_ON	Trim Enable	ManualFan	ShareMode	ORing FET	VariableSpeed	-	-
<b>MSB</b>							<b>LSB</b>

Bit #	Bit Status Description
7	Set Main Output Enabled Clear Main Output Disabled
6	Set Main Voltage Trimming Enabled Clear Main Voltage Trimming Disabled
5	Set I <sup>2</sup> C Manual Fan Speed Enabled Clear I <sup>2</sup> C Manual Fan Speed Disabled
4	Set Droop Current Sharing Clear Active Current Sharing
3	Set ORing FET Enabled Clear ORing FET Disabled
2	Set Fan Variable Speed Enabled Clear Fan Variable Speed Disabled
1	-
0	-

Byte 1 - The D1U-H Status 1 register is reserved for future use.

Byte 2 - The D1U-H O/P Fault 0 register function and definitions are as follows:

BYTE 1- Output Fault Register							
7	6	5	4	3	2	1	0
AC Fault	Stby Fault	OT Fault	1 Fan Fault	2 Fans Fault	-	-	-
<b>MSB</b>							<b>LSB</b>

Bit #	Bit Status Description
7	Set AC Fault Clear No AC Fault
6	Set Standby Fault Clear No Standby Fault
5	Set Hot-spot Over-Temperature Fault Clear No Hot-spot OT Fault
4	Set 1 Fan Fault Clear No 1 Fan Fault
3	Set 2 Fans Fault Clear No 2 Fans Fault
2	-
1	-
0	-

Byte 3 - The D1U-H O/P Fault 1 register function and definitions are as follows:

BYTE 1- Output Fault Register							
7	6	5	4	3	2	1	0
Main OV	Main UV	Main OC	PCB OT	-	-	-	-
<b>MSB</b>							<b>LSB</b>

Bit #	Bit Status Description
7	Set Main Output Over-Voltage Fault Clear No OV Fault
6	Set Main Output Under-Voltage Fault Clear No UV Fault
5	Set Main Output Over-Current Fault Clear No OC Fault
4	Set PCB Over-Temperature Fault Clear No PCB OT
3	-
2	-
1	-
0	-

### Parametric Data Registers

The D1U-H family currently supports 10-bit monitoring of the main output voltage, main output current, fan sense, hot-spot temperature and PCB temperature.

#### Byte 4 (High Byte) and 5 (Low Byte) - 10-bit representation of the Main Output Voltage

Model	Detection Range	Transfer Equation	Accuracy
D1U-H_2800-52-HB1LC	0-67.6VDC	0.0661 V/LSB	+/- 3% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1C	0-67.6VDC	0.0661 V/LSB	+/- 3% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2C	0-67.6VDC	0.0661 V/LSB	+/- 3% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1DC	0-67.6VDC	0.0661 V/LSB	+/- 3% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2DC	0-67.6VDC	0.0661 V/LSB	+/- 3% inside O/P regulation limits (00-50°C)

#### Byte 6 (High Byte) and 7 (Low Byte) - 10-bit representation of the Main Output Current

Model	Detection Range	Transfer Equation	Accuracy
D1U-H_2800-52-HB1LC	0-81 ADC	0.0791 A/LSB	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1C	0-81 ADC	0.0791 A/LSB	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2C	0-81 ADC	0.0791 A/LSB	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1DC	0-81 ADC	0.0791 A/LSB	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2DC	0-81 ADC	0.0791 A/LSB	+/- 10% inside O/P regulation limits (00-50°C)

#### Byte 8 (High Byte) and 9 (Low Byte) - 10-bit representation of the Fan Sense

Model	Detection Range	Transfer Equation	Repeatability
D1U-H_2800-52-HB1LC	0-255 LSB	-	+/- 5% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1C	0-255 LSB	-	+/- 5% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2C	0-255 LSB	-	+/- 5% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1DC	0-255 LSB	-	+/- 5% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2DC	0-255 LSB	-	+/- 5% inside O/P regulation limits (00-50°C)

#### Byte 10 (High Byte) and 11 (Low Byte) - 10-bit representation of the hot-spot temperature

Model	Detection Range	Transfer Equation	Accuracy (Theory)
D1U-H_2800-52-HB1LC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1C	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2C	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1DC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2DC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)

#### Byte 12 (High Byte) and 13 (Low Byte) - 10-bit representation of the PCB temperature

Model	Detection Range	Transfer Equation	Accuracy (Theory)
D1U-H_2800-52-HB1LC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1C	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2C	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB1DC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)
D1U-H_2800-52-HB2DC	-40 to 125°C	(10-bit reading(dec)-248)/6.2	+/- 10% inside O/P regulation limits (00-50°C)

### The I<sup>C</sup> Read Offset Control Byte

The D1U-H family currently supports a single write command byte to specify the subsequent I<sup>C</sup> read address. This enables the host to start reading at any location (valid location is 0 to 13). The read protocols include Current Address Read, Sequential Read, and Random Read.

The I<sup>C</sup> Current Address Read method is as follows:

- The internal read address pointer is initialized to point to the address of RAM variable 1 (address of vPS\_Status0);
- The address pointer is incremented by one after each byte read operation;
- After the last variable (vAMB\_Temp1) has been read, the pointer wraps to the address of the first variable;
- The data transmission sequence should be as follows:

I<sup>C</sup> Current Address Read



Note: Shaded data is from slave to master

The I<sup>2</sup>C Sequential Read method is as follows:

- The internal read address pointer is pointing to the address of the first RAM variable to be read;
- The address pointer is incremented by one after each byte read operation;
- After the last variable (vAMB\_Temp1) has been read, the pointer wraps to the address of the first variable;
- The data transmission sequence should be as follows:



The I<sup>2</sup>C Random Read method is as follows:

- The internal read address pointer is set at any time by a write command:

I<sup>2</sup>C Write Command to Set Read Address Pointer



- Subsequent data transmission sequence should be as follows:

I<sup>2</sup>C Random Read



- The address pointer is incremented by one after each byte read operation;
- After the last variable (vAMB\_Temp1) has been read, the pointer wraps to the address of the first variable;

### FRU EEPROM Contents with Byte Descriptions

Address	Byte	HEX Data	ASCII	Description	Notes
[0000]	Byte 0	1		Common Header Format Version	
	Byte 1	1		Internal Use Area	
	Byte 2	0	NULL	Chassis Info Area Starting	
	Byte 3	9		Board Area Starting Offset	Byte 73
	Byte 4	0	NULL	Product Info Area Starting Offset	
	Byte 5	18		Multi-Record Area Offset	Byte 192
	Byte 6	0	NULL	Pad with zero	
	Byte 7	DD		Common Header Checksum	
	Byte 8	1		Internal Use Format Version	
	Byte 9	0	NULL	ICT Revision	
	Byte 10	0	NULL	ICT Revision	
	Byte 11	0	NULL	Test Pass Code	
	Byte 12	0	NULL	Test Pass Code	
	Byte 13	0	NULL	Test Pass Code	
	Byte 14	0	NULL	Test Location	
	Byte 15	0	NULL	Number of Tests Performed	
[0010]	Byte 16	0	NULL	Number Of Failures Detected	
	Byte 17	0	NULL	Number of NTF Detected	
	Byte 18	0	NULL	Functional Revision	
	Byte 19	0	NULL	Functional Revision	
	Byte 20	0	NULL	Functional Test Pass Code	
	Byte 21	0	NULL	Functional Test Pass Code	
	Byte 22	0	NULL	Functional Test Pass Code	
	Byte 23	0	NULL	Functional Test Location	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 24	0	NULL	Number of Tests Performed	
	Byte 25	0	NULL	Number Of Failures Detected	
	Byte 26	0	NULL	Number of NTF Detected	
	Byte 27	0	NULL	LCD Revision	
	Byte 28	0	NULL	LCD Revision	
	Byte 29	0	NULL	LCD Test Pass Code	
	Byte 30	0	NULL	LCD Test Pass Code	
	Byte 31	0	NULL	LCD Test Pass Code	
[0020]	Byte 32	0	NULL	Functional Test Location	
	Byte 33	0	NULL	Number of Tests Performed	
	Byte 34	0	NULL	Number Of Failures Detected	
	Byte 35	0	NULL	Number of NTF Detected	
	Byte 36	0	NULL	CTO Revision	
	Byte 37	0	NULL	CTO Revision	
	Byte 38	0	NULL	Functional CTO	
	Byte 39	0	NULL	Functional CTO	
	Byte 40	0	NULL	Functional CTO	
	Byte 41	0	NULL	CTO. Test Location	
	Byte 42	0	NULL	Number of CTO Tests Performed	
	Byte 43	0	NULL	Number Of CTO Failures Detected	
	Byte 44	0	NULL	Number of CTO NTF Detected	
	Byte 45	0	NULL	Audit Test Revision	
	Byte 46	0	NULL	Audit Test Revision	
	Byte 47	0	NULL	Audit Test Pass Code	
[0030]	Byte 48	0	NULL	Audit Test Pass Code	
	Byte 49	0	NULL	Audit Test Pass Code	
	Byte 50	0	NULL	Audit. Test Location	
	Byte 51	0	NULL	Number of Audit Tests Performed	
	Byte 52	0	NULL	Number Of Audit Failures Detected	
	Byte 53	0	NULL	Number of Audit NTF Detected	
	Byte 54	0	NULL	Field Repair Revision	
	Byte 55	0	NULL	Field Repair Revision	
	Byte 56	0	NULL	Field Repair Test Pass Code	
	Byte 57	0	NULL	Field Repair Test Pass Code	
	Byte 58	0	NULL	Field Repair Test Pass Code	
	Byte 59	0	NULL	Field Repair Test Location	
	Byte 60	0	NULL	Number of Field Repair Tests Performed	
	Byte 61	0	NULL	Number Of Field Repair Failures Detected	
	Byte 62	0	NULL	Number of Field Repair NTF Detected	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 63	0	NULL	Reserved for future Use	
[0040]	Byte 64	0	NULL	Reserved for future Use	
	Byte 65	0	NULL	Reserved for future Use	
	Byte 66	0	NULL	Reserved for future Use	
	Byte 67	0	NULL	Reserved for future Use	
	Byte 68	0	NULL	Reserved for future Use	
	Byte 69	0	NULL	Reserved for future Use	
	Byte 70	0	NULL	Reserved for future Use	
	Byte 71	0	NULL	Reserved for future Use	
	Byte 72	1		Board Area Format Version	Start of Check-sum
	Byte 73	0F		Board Area Length	
	Byte 74	0	NULL	Language Code	
	Byte 75	20		Manufacturing Date And Time (Hex)	
	Byte 76	20		Manufacturing Date And Time (Hex)	
	Byte 77	20		Manufacturing Date And Time (Hex)	
	Byte 78	CA		Board Manufacturer Name type/length	10 Bytes long
	Byte 79	43	M	Board Manufacturer Name	
[0050]	Byte 80	26	P	Board Manufacturer Name	
	Byte 81	44	S	Board Manufacturer Name	
	Byte 82	20		Board Manufacturer Name	
	Byte 83	20		Board Manufacturer Name	
	Byte 84	20		Board Manufacturer Name	
	Byte 85	20		Board Manufacturer Name	
	Byte 86	20		Board Manufacturer Name	
	Byte 87	20		Board Manufacturer Name	
	Byte 88	20		Board Manufacturer Name	
	Byte 89	E0		Board Product Name type/length	32 Bytes long
	Byte 90	42	B	Board Product Name	
	Byte 91	55	U	Board Product Name	
	Byte 92	4C	L	Board Product Name	
	Byte 93	4B	K	Board Product Name	
	Byte 94	20		Board Product Name	
	Byte 95	50	P	Board Product Name	
[0060]	Byte 96	4F	O	Board Product Name	
	Byte 97	57	W	Board Product Name	
	Byte 98	45	E	Board Product Name	
	Byte 99	52	R	Board Product Name	
	Byte 100	20		Board Product Name	
	Byte 101	53	S	Board Product Name	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 102	55	U	Board Product Name	
	Byte 103	50	P	Board Product Name	
	Byte 104	50	P	Board Product Name	
	Byte 105	4C	L	Board Product Name	
	Byte 106	59	Y	Board Product Name	
	Byte 107	20		Board Product Name	
	Byte 108	20		Board Product Name	
	Byte 109	20		Board Product Name	
	Byte 110	20		Board Product Name	
	Byte 111	20		Board Product Name	
[0070]	Byte 112	20		Board Product Name	
	Byte 113	20		Board Product Name	
	Byte 114	20		Board Product Name	
	Byte 115	20		Board Product Name	
	Byte 116	20		Board Product Name	
	Byte 117	20		Board Product Name	
	Byte 118	20		Board Product Name	
	Byte 119	20		Board Product Name	
	Byte 120	20		Board Product Name	
	Byte 121	20		Board Product Name	
	Byte 122	D0		Board Serial Number type/length	16 Bytes long
	Byte 123	35	5	Board Serial Number (HEX)	
	Byte 124	32	2	Board Serial Number (HEX)	
	Byte 125	43	C	Board Serial Number (HEX)	
	Byte 126	54	T	Board Serial Number (HEX)	
	Byte 127	48	H	Board Serial Number (HEX)	
[0080]	Byte 128	30	0	Board Serial Number (HEX)	Input from serial number bar code
	Byte 129	30	0	Board Serial Number (HEX)	
	Byte 130	30	0	Board Serial Number (HEX)	
	Byte 131	30	0	Board Serial Number (HEX)	
	Byte 132	20		Board Serial Number (HEX)	
	Byte 133	20		Board Serial Number (HEX)	
	Byte 134	20		Board Serial Number (HEX)	
	Byte 135	20		Board Serial Number (HEX)	
	Byte 136	20		Board Serial Number (HEX)	
	Byte 137	20		Board Serial Number (HEX)	
	Byte 138	20		Board Serial Number (HEX)	
	Byte 139	CB		Board Part Number type/length	11 Bytes long
	Byte 140	30	0	Board Part Number (HEX-ASCII)	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 141	39	9	Board Part Number (HEX-ASCII)	
	Byte 142	35	5	Board Part Number (HEX-ASCII)	
	Byte 143	37	7	Board Part Number (HEX-ASCII)	
[0090]	Byte 144	2D	-	Board Part Number (HEX-ASCII)	
	Byte 145	32	2	Board Part Number (HEX-ASCII)	
	Byte 146	31	1	Board Part Number (HEX-ASCII)	
	Byte 147	34	4	Board Part Number (HEX-ASCII)	
	Byte 148	30	0	Board Part Number (HEX-ASCII)	
	Byte 149	20		Board Part Number (HEX-ASCII)	
	Byte 150	20		Board Part Number (HEX-ASCII)	
	Byte 151	41		FRU File ID type/length	
	Byte 152	10		FRU File ID	
	Byte 153	C8		Board Revision type/length	8 Bytes long
	Byte 154	58	X	Board Revision (HEX-ASCII)	
	Byte 155	31	1	Board Revision (HEX-ASCII)	
	Byte 156	20		Board Revision (HEX-ASCII)	
	Byte 157	20		Board Revision (HEX-ASCII)	
	Byte 158	20		Board Revision (HEX-ASCII)	
	Byte 159	20		Board Revision (HEX-ASCII)	
[00A0]	Byte 160	20		Board Revision (HEX-ASCII)	
	Byte 161	20		Board Revision (HEX-ASCII)	
	Byte 162	C4		Engineering Date Code type/length	
	Byte 163	34	4	Engineering Date Code (HEX-ASCII)	
	Byte 164	33	3	Engineering Date Code (HEX-ASCII)	Input from EDC barcode
	Byte 165	32	2	Engineering Date Code (HEX-ASCII)	
	Byte 166	34	4	Engineering Date Code	(HEX-ASCII)
	Byte 167	C2		Board Artwork Revision type/length	2 Bytes long
	Byte 168	41	A	Board Artwork Revision (HEX-ASCII)	
	Byte 169	31	1	Board Artwork Revision (HEX-ASCII)	
	Byte 170	10		FRU-Specific Info type/length	16 Bytes long
	Byte 171	0	NULL	FRU-Specific Information	
	Byte 172	0	NULL	FRU-Specific Information	
	Byte 173	0	NULL	FRU-Specific Information	
	Byte 174	0	NULL	FRU-Specific Information	
	Byte 175	0	NULL	FRU-Specific Information	
[00B0]	Byte 176	0	NULL	FRU-Specific Information	
	Byte 177	0	NULL	FRU-Specific Information	
	Byte 178	0	NULL	FRU-Specific Information	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 179	0	NULL	FRU-Specific Information	
	Byte 180	0	NULL	FRU-Specific Information	
	Byte 181	0	NULL	FRU-Specific Information	
	Byte 182	0	NULL	FRU-Specific Information	
	Byte 183	0	NULL	FRU-Specific Information	
	Byte 184	0	NULL	FRU-Specific Information	
	Byte 185	0	NULL	FRU-Specific Information	
	Byte 186	0	NULL	FRU-Specific Information	
	Byte 187	C1		C1h indicates no more fields	
	Byte 188	0	NULL	Pad With Zeros	
	Byte 189	0	NULL	Pad With Zeros	
	Byte 190	0	NULL	Pad With Zeros	
	Byte 191	0F		Board Info Checksum	
	Byte 192	0	NULL	Power Supply Information Record	Start of Check-sum for multi-record
	Byte 193	2		End of list/version	
	Byte 194	18		Record length	
	Byte 195	B1		Record Checksum	
	Byte 196	35		Header Checksum	
	Byte 197	40		Overall capacity	(watts) (LSB)
	Byte 198	6		Overall capacity	(watts) (MSB)
	Byte 199	FF		Peak VA LSB	
	Byte 200	FF		Peak VA	
	Byte 201	FF		Inrush current	
	Byte 202	0		Inrush interval in ms.	
	Byte 203	28		Low end Input voltage range 1 (10mv) LSB	
	Byte 204	23		Low end Input voltage range 1 (10mv) MSB	
	Byte 205	B0		High end Input voltage range 1 (10mv) LSB	
	Byte 206	36		High end Input voltage range 1 (10mv) MSB	
	Byte 207	50		Low end Input voltage range 2 (10mv) LSB	
[00D0]	Byte 208	46		Low end Input voltage range 2 (10mv) MSB	
	Byte 209	20		High end Input voltage range 2 (10mv) LSB	
	Byte 210	67		High end Input voltage range 2 (10mv) MSB	
	Byte 211	2F		Low end Input frequency range	
	Byte 212	3F		High end Input frequency range	
	Byte 213	14		AC Dropout Tolerance (ms)	
	Byte 214	7		Binary Flags	
	Byte 215	0		Peak Wattage	

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 216	0		Peak Wattage LSB	
	Byte 217	3		Combined Voltage Wattage ID	
	Byte 218	40		Combined Wattage LSB	
	Byte 219	6		Combined Wattage MSB	
	Byte 220	0		Predictive fail tachometer lower threshold	
	Byte 221	FF			
	Byte 222	FF			
	Byte 223	FF			
[00E0]	Byte 224	FF			
	Byte 225	FF			
	Byte 226	FF			
	Byte 227	FF			
	Byte 228	FF			
	Byte 229	FF			
	Byte 230	FF			
	Byte 231	FF			
	Byte 232	FF			
	Byte 233	FF			
	Byte 234	FF			
	Byte 235	FF			
	Byte 236	FF			
	Byte 237	FF			
	Byte 238	FF			
	Byte 239	FF			
[00F0]	Byte 240	FF			
	Byte 241	FF			
	Byte 242	FF			
	Byte 243	FF			
	Byte 244	FF			
	Byte 245	FF			
	Byte 246	FF			
	Byte 247	FF			
	Byte 248	FF			
	Byte 249	FF			
	Byte 250	FF			
	Byte 251	FF			
	Byte 252	FF			

Address	Byte	HEX Data	ASCII	Description	Notes
	Byte 253	FF			
	Byte 254	FF			
	Byte 255	FF			
[0100]					

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This product is subject to the following [operating requirements](#) and the [Life and Safety Critical Application Sales Policy](#): Refer to: <http://www.murata-ps.com/requirements/>

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