D1U54P-12-EDGE

ACAN-73 Connector Card Application Note

OVERVIEW

The D1U54P-12-EDGE interface connector card is a dual card that is intended to interconnect the output voltages and signals of one or two D1U54x-x-450-12-HxxC Series power modules for laboratory/bench level evaluation of the product.
The outputs are capable of being parallel connected and a common ISHARE bus is provided to ensure that both power modules share current within specified limits.
The Interface Card is capable of operation from standby voltages of 3.3V, 5V and 12V (provided by the D1U54x power supply under test) without any reconfiguration.
It is designed and intended to be used for the members within the following series (both AC and DC input source variants and both airflow options):

Order Number	Compatible with these Model Variants	3.3V$_{STANDBY}$	5V$_{STANDBY}$	12V$_{STANDBY}$
D1U54P-12-EDGE	D1U54P-W-450-12-HxxC-xxx	HC3C-xxx HC4C-xxx	HA3C-xxx HA4C-xxx	HB3C-xxx HB4C-xxx
	D1U54P-W-450-12-HxxC	HC3C HC4C	HA3C HA4C	HB3C HB4C
	D1U54-D-450-12-HxxC-xxx	-	HA3C-xxx HA4C-xxx	HB3C-xxx HB4C-xxx
	D1U54-D-450-12-HxxC	-	HA3C HA4C	HB3C HB4C

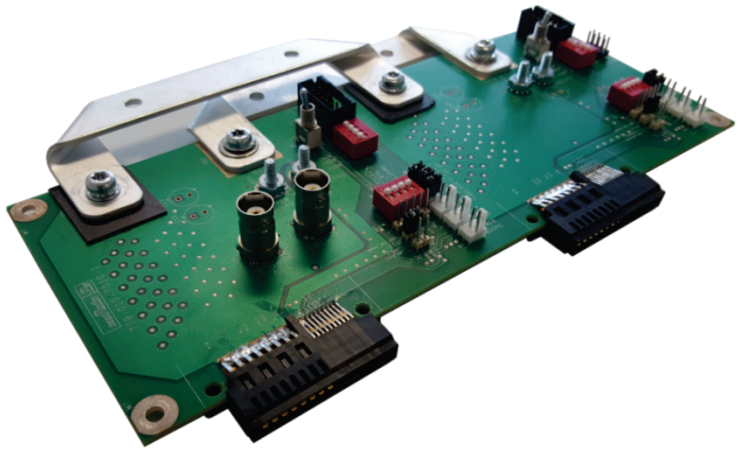
End Users can also use this card in their applications as an alternative to a host system power/mid or interposer connection plane (consult Murata Sales for details). To get the most from this application note, refer to the product PMBus™ communications protocol application note ACAN-72 as well as the series product datasheet.

SAFETY PRECAUTION

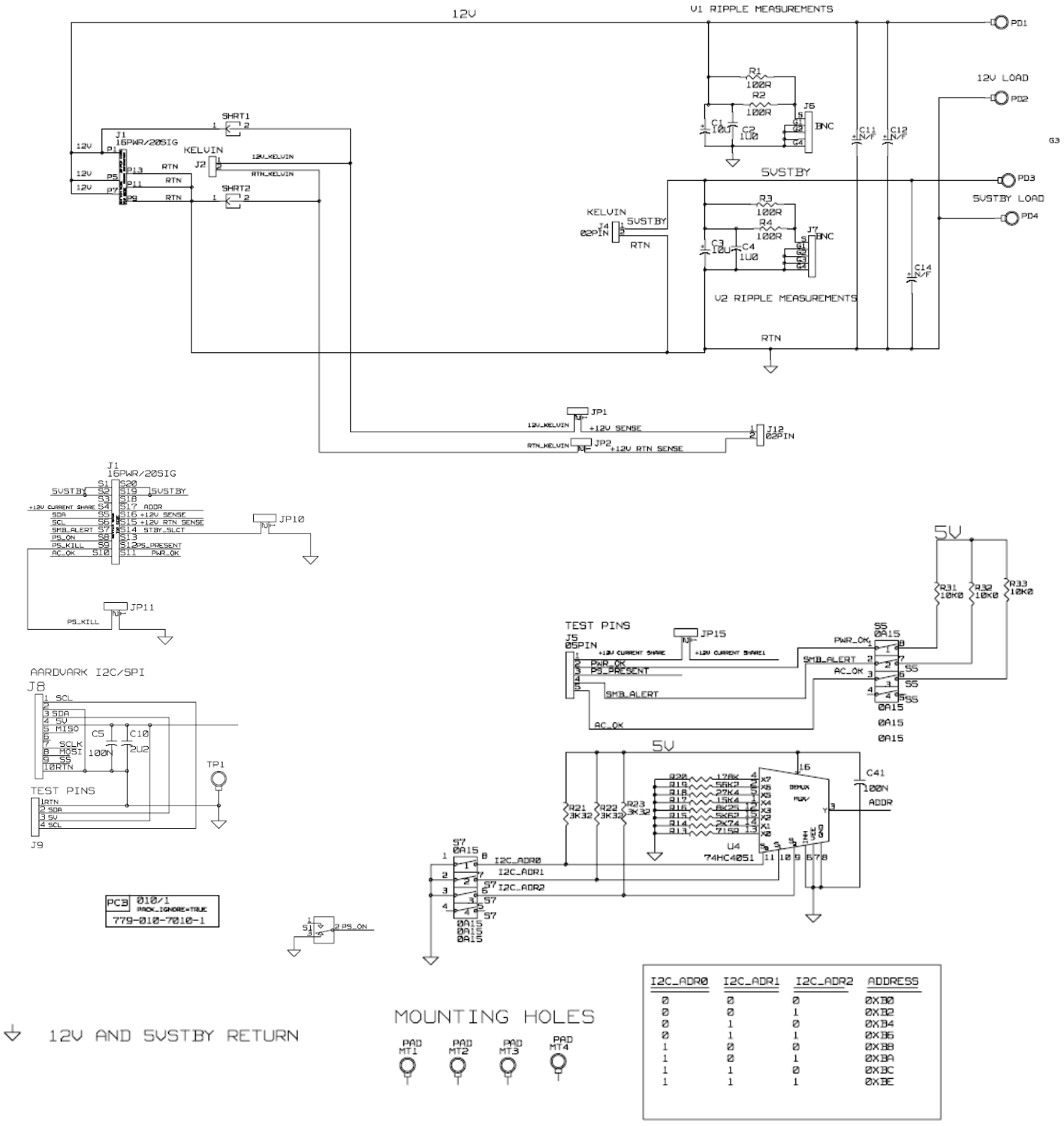
The D1U54P-12-EDGE output connector card is intended to facilitate the connection of the output supply rails of the power module. As such there a high energy source exposed on the output connector card; please take the necessary safety precautions during the use of this connector card for product evaluation.

IMAGE – D1U54P-12-EDGE

Component Side (Top) View

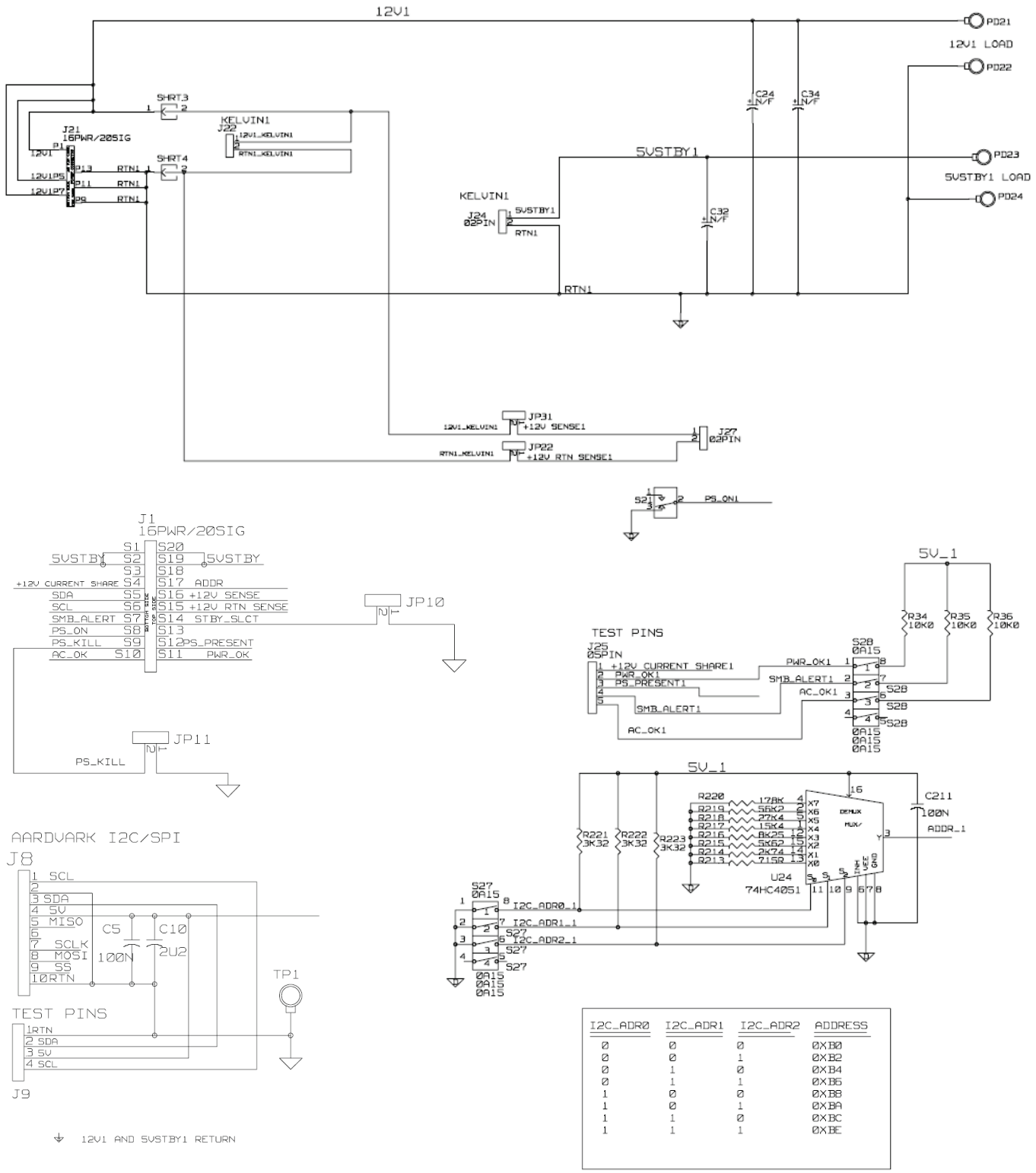


SCHEMATIC – D1U54P-12-EDGE PSU Slot 1



I2C_ADR0	I2C_ADR1	I2C_ADR2	ADDRESS
0	0	0	0XB0
0	0	1	0XB2
0	1	0	0XB4
0	1	1	0XB6
1	0	0	0XB8
1	0	1	0XBA
1	1	0	0XBC
1	1	1	0XBE

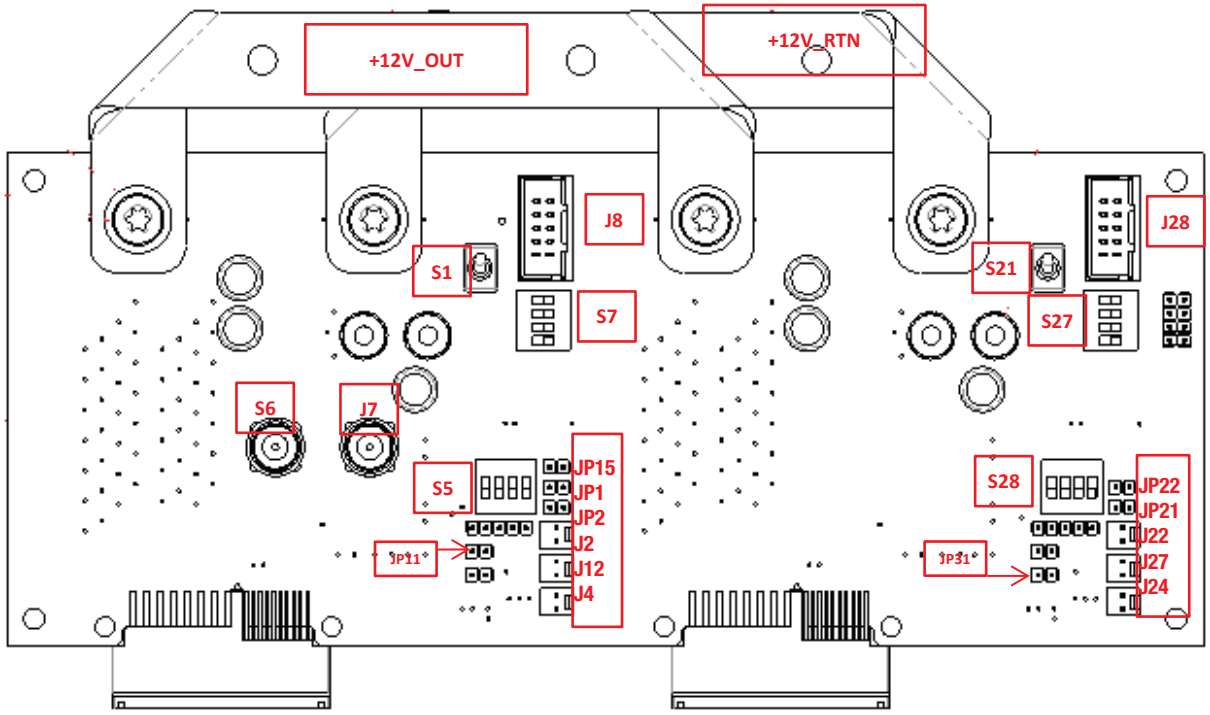
SCHEMATIC – D1U54P-12-EDGE PSU Slot 2



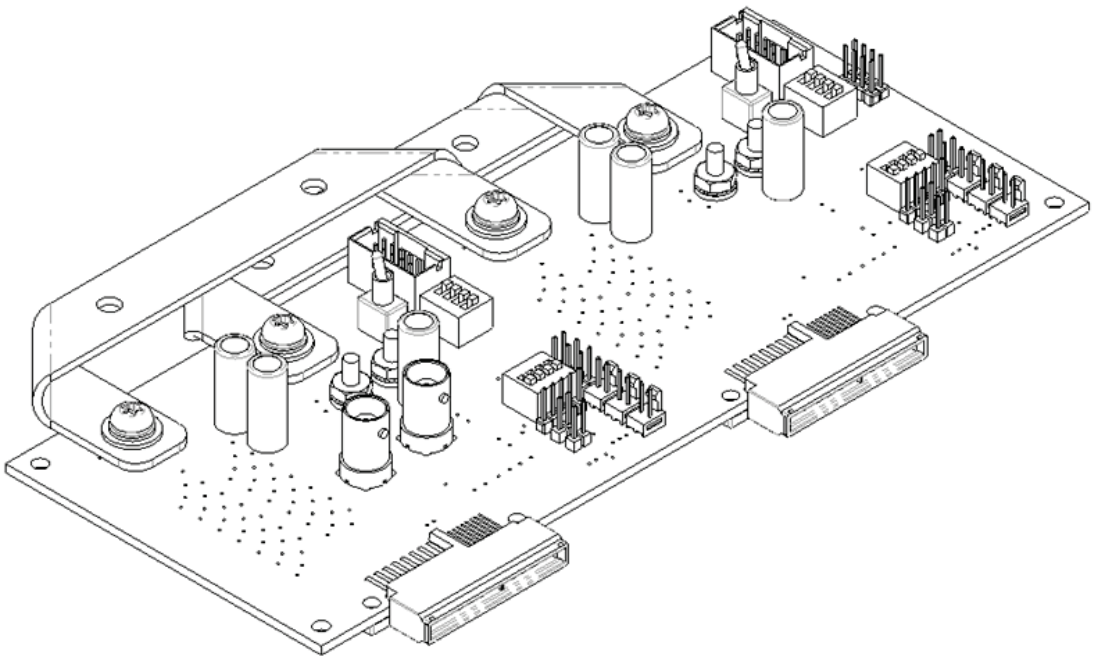
I2C_ADR0	I2C_ADR1	I2C_ADR2	ADDRESS
0	0	0	0XB0
0	0	1	0XB2
0	1	0	0XB4
0	1	1	0XB6
1	0	0	0XB8
1	0	1	0XBA
1	1	0	0XBC
1	1	1	0XBE

MECHANICAL OUTLINE

Top View



3D View



CONFIGURATION NOTES:

1. The Interface Connector card is basically two identical circuits, provided on a single card (PCB). Each "half" or "slot has all the necessary configuration links duplicated to enable each "half" to operate individually if required. Key difference being the ripple measurement BnC connectors, provided for one of the two slots.

   Common connections exist these being as follows:

   a. Power bus bars that are intended to interconnect the main 12VDC outputs of each "half"; these can be removed as required, and substituted with separate cables to the required load.
   b. ISHARE signal bus between each "half". This interconnection is provided by a single jumper JP15 and can be removed if operation as two independent (no parallel connection) is required.

   Note that no physical parallel connection is provided to interconnect the VSTANDBY output of each "half". If required cable connections can be provided by the End User (note: parallel connection of the VSTANDBY is subject to the limitations as described in the respective product datasheets).

2. To configure each "half" for independent or parallel operation, ensure that the following configurable jumpers (headers) have shorting links (shunts Dual Beam; TE Connectivity Pt# 390088-2) fitted across their respective Pins 1 & 2 (refer to schematic, photograph and Red Boxes on the preceding mechanical outline top view.
   a. JP1/JP21 ; +12VSENSE local voltage sense selection; deselect if remote sense connection is provided to the load.
   b. JP2/JP22; +12VSENSE_RTN local voltage sense selection;deselect if remote sense connection is provided to the load.
   c. JP11 & JP31 (PS_KILL connection to GNDB/GNDD return ; enables output). Can also be used to reset status registor faults and warnings.
   d. JP15; this jumper interconencts the ISHARE signals between the two power modules. Fit the shorting link across Pins 1 & 2 if the units are to be operated in parallel to share a common load.
      Remove the shorting link if the units are to be operated "independently" as separate power modules.

3. The two DC Main 12V DC outputs are interconnected with bus bars.

4. The BNC connectors for ripple & noise measurements of 12VSTBY (J7 bias/standby) and 12VOUT (J6 Main output) are intended for direct (BNC to BNC) connection (or via a 10X probe if required) to an oscilloscope. Note also that the measurement node is filtered with a parallel connected 10µF tantalum and 1µF ceramic capacitor (across tip to ground)
   A short 50ohm coaxial cable connnection shall be provided between the relevant BNC measurement connector and the input to the measuring 'scope (the 'scope bandwidth shall be limited to 20MHz).

5. Connector J8/J28 is a PMBob I^2C/SPI interface connector. The PMBob USB to I2C Interface external device allows communications via a USB port of a laptop or PC that can be used with the provided MPS software GUI.
   As such this is the recommended communication interface for use with this interface card for initial bench evaluation.
   Refer to ACAN 72 for PMBus™ Communications Protocol for this product series.

6. S1/S21 enables/disables (turns "on"/"off") the main output by connecting PS_ON_L to the respective 12VSTBY Return.
   Close S1/S21 to enable (turn "on") the respective power module 12VDC Main Output.

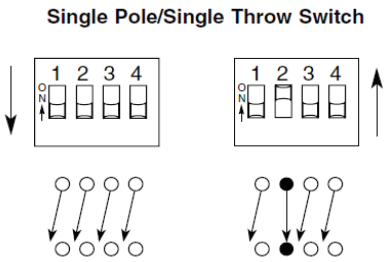
CONFIGURATION NOTES:

7. S7/S27 are a four (4) position DIL/DIP switches that is intended to select the User configurable bits that assign the variable address for I^2C communications with the power module.
   The D1U54x-x-450-12-HxxC products series' employs an analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications.
   Connection of a suitable resistor to +VSB_Return, in conjunction with a resistor divider chain (internal to the power module), will configure the required address.
   However since the purpose of this connector card is to provide a convenient means to evaluate the D1U54x-x-450-12-HxxC products, this method has been replaced by an analogue multiplexer device that allows selection of the slave address via a "pin strap" method using three address bits (configured via S7/S27).

S7/S27 Position #3 (A2) (Serial Address BIT 2)	S7/S27 Position #2 (A1) (Serial Address BIT 1)	S7/S27 Position #1 (A0) (Serial Address BIT 0)	Power Module Main Controller (Serial Comm Slave Address)	Power Module Main EEPROM (Serial Comm Slave Address)
LOW	LOW	LOW	0xB0	0xA0
LOW	LOW	HIGH	0xB2	0xA2
LOW	HIGH	LOW	0xB4	0xA4
LOW	HIGH	HIGH	0xB6	0xA6
HIGH	LOW	LOW	0xB8	0xA8
HIGH	LOW	HIGH	0xBA	0xAA
HIGH	HIGH	LOW	0xBC	0xAC
HIGH	HIGH	HIGH	0xBE	0xAE

The address convention uses 7-bit left shifted Slave Device addressing with the Read/Write bit either a "0" (Write) or a "1" (Read). The addresses above assume the Read/Write bit is a "0".

S7/S27 is shown in the diagram opposite (also refer to the schematic).
With any of the DIL switches (1, 2, & 3) set to the "off" (open) position, the corresponding address line (A0/A1/A2 respectively) shall be set to a logic level high (by action of the 3K32K ohm pull up resistor upon the Interface Connector Card.
Operating the appropriate switch to the "on" (closed) position will connect the appropriate line to a logic level low.
Note: The switch position DIL Position #4 is unused and has no connection (NC) on the interface connector card.



NB: The D1U54x-x-450-12-HxxC Series employs "left shifted" 7-Bit addressing; where Bit "0"of the device address is the Read/Write bit. The addresses, as shown above, assume that the Read/Write bit is a logic level "0".

Internal MPS P/N: M7010