

## Output Capacitive Load Considerations DCAN-58

By Larry Copeland

There are numerous factors to consider when adding external capacitors to switched-mode power supplies (SMPS). This article will discuss noise, startup, ESR, stability, pre-bias applications, Sense inputs, On/Off (remote enable) controls and other topics.

Many real-world DC/DC applications require external bypass “bulk” capacitors as part of the output load. These capacitors supply extra current during a step load change. Lower DC voltages used in newer logic devices mean that the voltage margin difference between logic ZERO and logic ONE is reduced to hundreds or even tens of millivolts. Thus, since even modest power supply noise can cause data errors by exceeding this threshold, these bypass caps are necessary to reduce this DC/DC noise.

The excellent performance of these converters is based on minimal output capacitance, typically some small filter components noted in the product specifications. Any output load is assumed to be purely resistive with no capacitive or inductive reactance. While these converters are rated to accept a maximum amount of output capacitance, that is for a single capacitor with known Equivalent Series Resistance (ESR), placed very close to the converter with adequate board etch and grounding. The specifications also assume that there is no other reactive output load, especially inductance. Be aware that external capacitors include finite amounts of internal, unwanted ESL (Equivalent Series Inductance). External wiring also includes additional series inductance.

In addition to the possibility of failed or delayed startup (see item [6] below), increasing external capacitance can cause sluggish transient response, possible ringing and instability. Excessive output capacitance combined with low ESR and higher inductance and/or poor board layout can even make some converters oscillate. The maximum output capacitive load specification is really an indication of acceptable and stable startup performance but with moderated transient response.

A further complication associated with external bypass capacitance is the ESR inside each capacitor. Acting as a small-value resistor in series with the internal capacitance, low ESR values are desirable to absorb load spikes. However, lower ESR capacitors may compromise the dynamic performance of the converter. That is why some converters can accept larger output capacitors as long as the ESR is higher.

Modern systems, with an assortment of programmable logic, CPU's, memories and distributed I/O circuits are difficult to fully characterize analytically. Thus, some empirical testing may be necessary to assure successful operation. Also be aware that all output circuit elements, including bypass capacitors, inherent load reactance and other circuit parasitics, become part of the total control loop circuit inside the converter. Increasing amounts of external capacitance reduce the phase margin of the internal control loop and therefore endangers dynamic performance.



### Application Example

In the following application, we see three bypass capacitors, all at different distances from the DC/DC converter. For now, we will ignore the three small 1  $\mu\text{F}$  ceramic caps used for high frequency suppression. At first glance, one might be tempted to simply add together the three parallel bypass caps (500, 2000 and 1000  $\mu\text{F}$  = 3500  $\mu\text{F}$ ). If the converter's rated maximum capacitive load specification is 5000  $\mu\text{F}$ , we are apparently “safely” within specification.

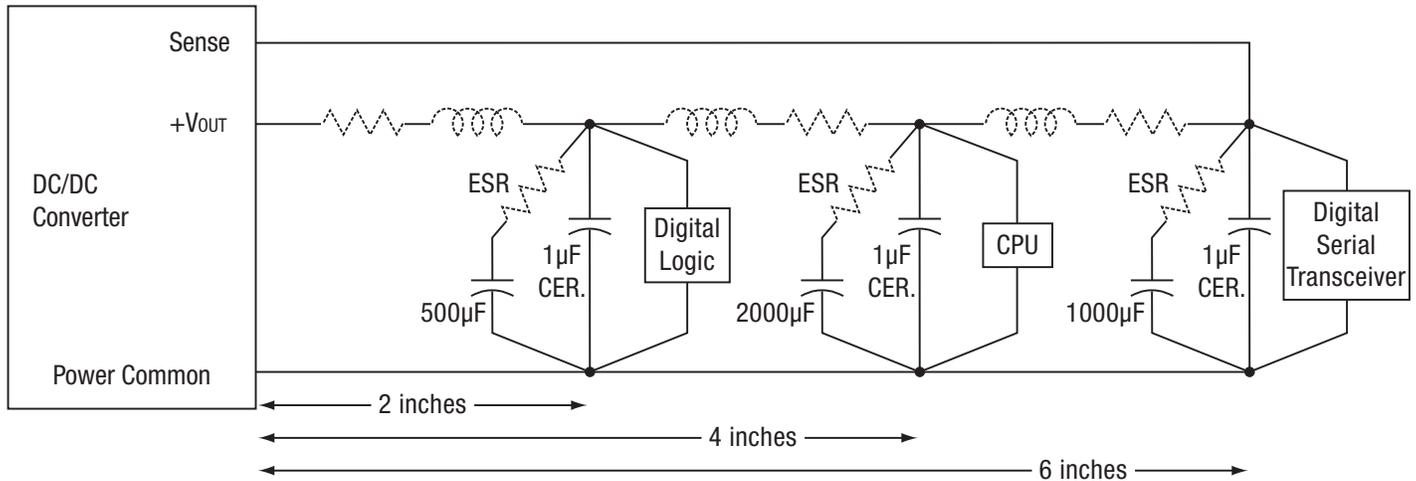
However, this analysis does not consider the “phantom” passive components in dashed lines. These phantoms consist of inductance, stray capacitive and resistive elements in the power wiring and copper etch. And it includes the ESR inside each bypass cap. Real-world caps also include tiny amounts of ESL series inductance, sometimes not specified on capacitor data sheets. The combination of all these additional “free” components plus the user's PC board layout comprise a complex **distributed constant** network. If the actual values can be measured at all, theoretical analysis of such a network can be a considerable effort.

A recommended solution is to test the system empirically, looking for noise levels, ringing and oscillation in the DC/DC's output with step load changes. If performance is marginal, consider changing the filter components or implementing some other circuit changes including additional DC/DC converters located right at their loads. Yes, like much of advanced electronics, there is a little bit of “black magic” here that is hard to model mathematically.

### Guidelines

Here are some recommendations for external capacitor usage:

- [1] All dynamic, active systems ring with step load changes. The goal is to achieve a critically damped response where the initial overshoot or undershoot under step load changes does not exceed a given tolerance and the output enters and remains within an acceptable voltage band in less than a specified time span. MPS specifications list both recovery time and the error band after a specified step load change.  
  
When doing step load testing, make sure that the simulated load change ramps up or down at the current rate of change (in Amperes per micro-second) listed in the converter specification. Too “slow” a ramp may not adequately test the system.
- [2] Newer large-value bulk capacitors, especially ceramic types, exhibit lower ESR values and may reduce the phase margin of the converter's control loop. Select and test ceramic caps carefully in your system at each point of application. Ironically, a very tiny amount of series inductance between the converter and the capacitor (sometimes only a ferrite bead) may avoid problems. Make sure that the inductor does not saturate with maximum current.
- [3] Use only enough output capacitance to achieve the energy storage and noise suppression you need **and no more**. This point is very important because the temptation is to add more capacitance. You may need to be very flexible in your board layout including the option of using several smaller parallel caps in place of one large cap. Connect the capacitors right at the load.



**Figure 1. Typical distributed bypass capacitive load system**

- [4] The manufacturer and part number of the capacitor used to establish the maximum capacitive load specification is available from MPS. Compare these specifications (especially ESR) carefully with your system. However, this may be of limited value for systems with multiple parallel bypass caps at different distances, as in the application example.
- [5] If you can fully characterize your load, determine how much power supply noise your system can tolerate. Consider all load values. Use this noise limit to evaluate the system during empirical testing.
- [6] Another significant reason to specify a maximum output capacitance is to guarantee successful converter startup. External bulk bypass capacitors require a large current pulse to charge up initially. This power-on charge-up may be the largest load step that the converter ever sees.

The converter accepts several types of load. One is the initial bulk cap charge-up. Another load type is the steady-state circuit load once the system reaches full regulated output voltage. The bulk charge-up current is directly proportional to the rate of change of the bulk cap voltage.

Excessive output capacitance and/or low ESR may interfere with the converter's soft-start function or trigger the converter's output overload protection shutdown which causes startup to fail. Converters with "hiccup" over-current protection may actually cycle several times before the bypass caps are fully charged. Even if the bypass capacitor voltage eventually stabilizes, multiple restart attempts can result in an unknown delay for system startup and possible system initialization failure because the external "system" assumes that the converter is now running.

Another suggested solution to the bypass cap charge-up problem is to use a ramp rate sequenced (tracking) DC/DC converter.

- [7] Route the Sense lines carefully. The Sense input is used primarily to compensate for voltage drop output errors due to high output currents, finite resistance and the occasional extended length of power wiring. For this purpose, do not exceed the Sense compensation specification (typically 0.5 Volts maximum difference between the voltage at the Sense point and at

the converter's output terminals). Sense also offers some stability enhancement by coupling load changes into the converter's control loop. Make sure that Sense is not routed near large fields. If necessary, consider using shielding for the Sense lines.

For converters with two Sense lines (positive and negative outputs), consider routing the Sense lines in parallel. Avoid creating large loop area since induced current is proportional to the loop area times the magnetic field strength. The Sense lines do not carry much current therefore smaller trace size is acceptable.

In the application example, depending on the user's layout, you may want to terminate the Sense input at the larger (middle) CPU load instead of at the end.

- [8] Be cautious when using the On/Off (remote enable) control in conjunction with high output capacitance. After shutoff, avoid immediately turning the converter back on if there is stray voltage stored in the external output circuits. Allow the voltage on the external capacitors to decay using external bleeder circuits. Please refer to MPS's series of converters which feature pre-bias start-up. Also refer to the pre-bias discussion below.

If the output capacitors are not allowed to bleed down their voltage sufficiently after shutdown, some converters may fail startup because of residual output voltage applying excessive reverse current flowing back into the converter's outputs. Smaller output capacitors with lower energy storage should not interfere with startup or induce reverse output current. Most converters include a warning to limit the amount of current sourced back into the converter.

- [9] **Pre-Bias** operation protects the converter against existing external voltage on the output at power start-up and ensures a monotonic start-up before the converter reaches full regulation. Such pre-existing voltage might come from larger external bulk storage capacitors or another parallel current-sharing power supply. Most newer MPS converters include Pre-Bias protection.

Please observe the following pre-bias guidelines:

- A. The external pre-bias voltage must be *lower* than the expected final set-point output voltage. If the pre-bias voltage remains higher than the set-point and is capable of back-driving excess current, failed start up may occur. If the higher voltage remains after startup (a very unlikely condition), the output overvoltage protection (available on most models) may shut down the converter as the converter detects that it cannot maintain regulation.
- B. Tracking operation must not be used during pre-bias startup. If a Tracking/Sequence input is installed, the Tracking function is not available during startup. After successful startup time to full regulation (sometimes indicated by a Power Good signal from the converter), Tracking may be resumed. This applies to both power-on startups and cycling of the On/Off control.

- C. Carefully examine any output circuits with large external output capacitors and low-ESR. If there is no bleeder circuit or other method to reduce the stored voltage AND the cap voltage is higher than the expected set-point, start up may fail.

## Conclusion

This article has discussed several issues regarding external capacitive loads connected to DC/DC converters. For further assistance, please contact Murata Power Solutions' Application Engineers.

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