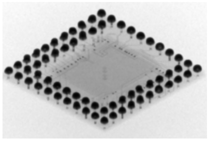
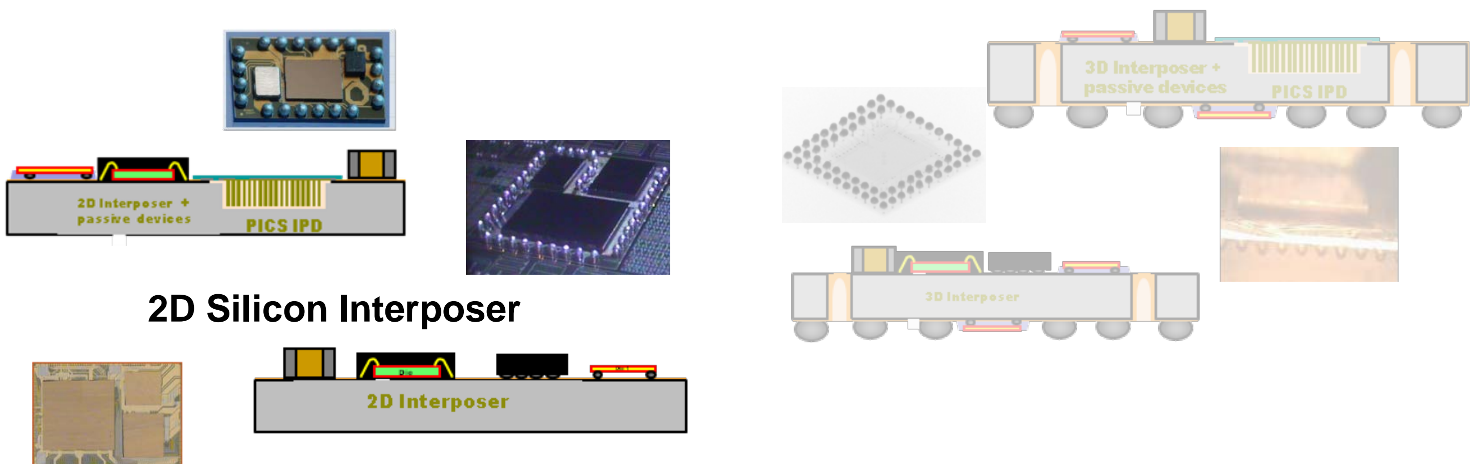


2D Silicon Interposer

Rev 1.0

Application Note

IPDiA has been a pioneering Silicon interposer platform since early 2000. With more than 100 million silicon interposers delivered in various markets, IPDiA is clearly recognized as a market leader.
The IPDiA interposer product offering includes a huge variety of solutions, from Basic 2D interposers to advanced 3D interposers with passive components built in the Silicon, in order to meet all your interposer requirements.



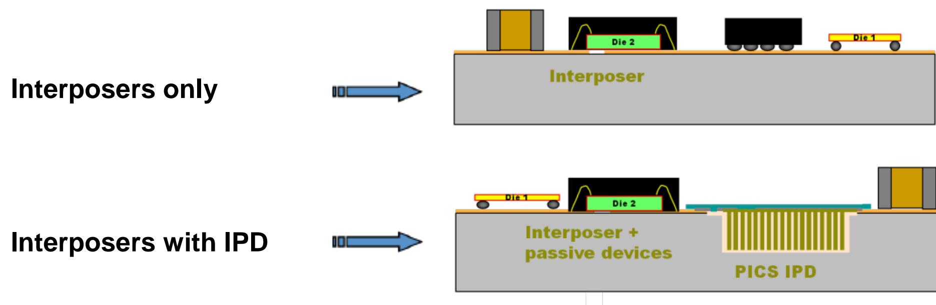
The IPDiA 2D silicon interposer is the perfect solution for applications with major size constraints. Thanks to the redistribution layer capability combined with the IPDiA Integrated Passive Device technology, most of the components required for the application can be integrated or soldered on top of the silicon interposer.

Key features

- 2 metal layers minimum
- Thickness 300 µm
- Very low leakage currents
- 2 metal line space: 5 µm minimum
- Integrated passive components
- 250 nF/mm^2 trench capacitors with high stability and low ESR
- High quality factor inductors Q > 80 at 10 GHz
- Polysilicon resistors with excellent matching

Key benefits

- Huge system size reduction
- Perfect CTE matching
- Bumping and flip-chip or die attach and wire-bonding
- Native redistribution and fanout
- Compliant with :
  - Organic platform (FR4, PCB, Flex, etc.)
  - Ceramic platform Package substrate
  - Glass platform
  - Metallic lead-frame platform



IPDiA Silicon Interposer main applications

- Space transformer, from semiconductor pitch to applicative substrate pitch with layout redistribution and space saving.
- Wafer level packaging solution.
- Interposer in Semiconductor IC Package with decoupling capacitors and redistribution layers.
- System integration platform with integrated passives, active bare dies, and Xtal, SMD.

Silicon Interposer comparison with alternative technologies

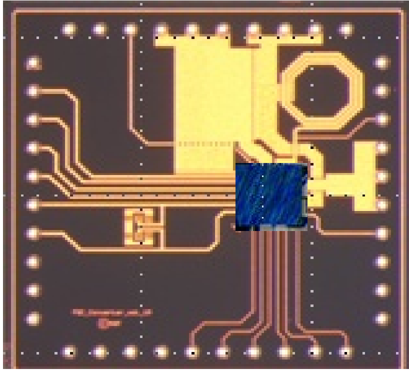
	Printed Circuit Board (PCB)	Thick/thin flex	Ceramic	Silicon Interposer
Line width / Spacing	90µm down to 65 µm for advanced PCB technologies	75µm down to 50µm for advanced thin flex technologies	75 µm to 50 µm for advanced LTCC technologies	5 µm
	Accuracy around 25µm	Accuracy around 15µm	Accuracy around 15 µm or less for LTCC	Below 1µm
Metal layers for signal and routing management	One metal layer in-between 2 thick laminated layer	Two layers for advanced flex technology	One layer	No limitation (2 to 3 layer)
Via diameter	200 µm or below for advanced PCB	150 µm for the best in class	120 µm for advanced LTCC	75 µm or below

Fig 1: Comparison on dimensions aspects

Substrate	Printed Circuit Board (PCB)	Thick flex	Ceramic	Silicon Interposer
CTE1	~ 20 ppm/K	~ 20 ppm/K	~ 10 ppm/K	~ 2 ppm/°C
	Big CTE mismatch with DSP and memories die set	Big CTE mismatch with DSP and memories die set	Slight CTE mismatch with DSP and memories die set	No CTE mismatch with DSP and memories die set
Temperature	Limited to 250 °C with warpage	Lower than 200 °C with polymer degradation	Higher than 400 °C	Higher than 400 °C
Process compatibility	Very good with SMD	Intermediate with SMD	Good with SMD	Good with SMD
	Critical with silicon die set	Intermediate with silicon die set	Good with silicon die set	Perfectly adjusted for silicon die set

Fig.2: Comparison on thermal, thermo-mechanical and material aspects

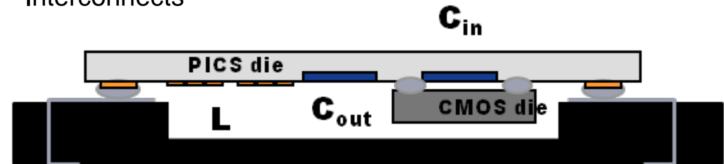
2D PICS Interposer examples



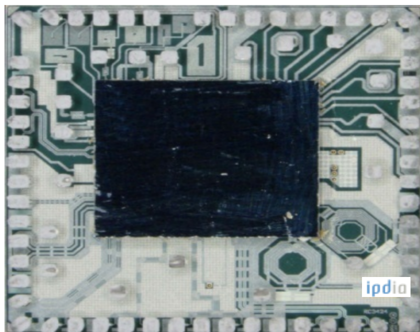
Active die flip-chipped on the IPD

Market Application: AC/DC converter in CSP package

- Frequency range: 100 MHz
- Components: Resistors, capacitors, Inductor, Interconnects



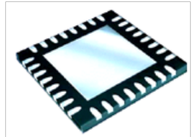
Module architecture

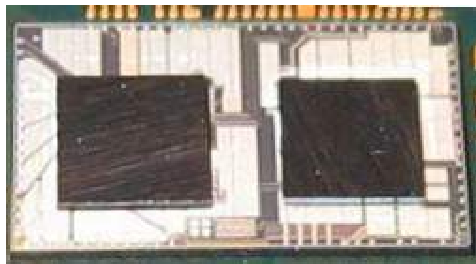


Active die flip-chipped on the IPD
5 mm x 5 mm

Market Application : Cellular in HVQFN package

- IPD RF module (with 73 SMD embedded) for W-CDMA & GSM RF transceiver
- 850-950MHz & 1.7-1.9GHz
- RF Silicon carrier flip chipped on lead frame (SIP)
- Components: RF capacitors, RF inductors, RF baluns, loop filters, decoupling capacitors and RF ESD protections





3 Active dies flip-chipped on the IPD
7.00 mm x 7.00 mm

Digital TV (Dual TV Tuner)

- 2 tuners flipped on silicon Interposer
- SnAg galvanic bumps on actives die
- Capacitors, Resistor build in
- External Aluminum pads
- Module picked and place over laminated substrate (LGA package)

3 Active dies flip-chipped on the IPD

2nd interconnect bumps on IPD

Double flip-chip on foil

Medical (In-vivo T° monitoring)

- 3 die flipped over silicon Interposer
- Gold stud bumps on actives die
- Capacitors, Resistor and PIN Diode built in the interposer
- External solder balls (WLCSP)
- Module flipped over flex substrate

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Date of release: 20th June 2012
Document identifier: