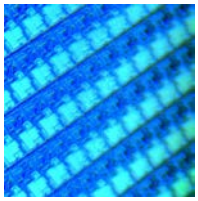

Silicon Capacitors Benefits for Phase Sensitive Broadband Applications

Rev 2.0 White Paper

Abstract

The Optical networking market demand for higher data rate is nowadays successfully covered by the use of **optical Phase Shift Keying** solutions like **DP-QPSK**. Compared with previous applications, all the components involved in the main signal line have to manage properly their **phase behavior** to minimize their **group delay** impact on final performances. In this paper, the intrinsic IPDiA Silicon capacitors group delay is compared with the multi layer ceramic capacitor (MLCC) one.

Key words: Integrated Passive Devices, Silicon Capacitors, QPSK, Broadband, Optical networking, Group delay

Introduction

IPDiA is involved in Silicon based 3D-IPD advanced technology. The 3D high-density capacitor is already at the forefront of IPDiA's roadmap with three generations already in production 25nF/mm^2, 80nF/mm^2 and 250nF/mm^2 and millions of products sold in the world in the consumer market.

IPDiA silicon components show outstanding characteristics in terms of integration, electrical behavior and reliability, and respond to the increasing demand of the optical networking domain regarding performances enhancement and miniaturization. IPDiA is indeed providing a high-capacitance platform which, combined with the low thickness of the components (400µm down to 100µm), delivers a high volumetric efficiency. Compared with the multi layer ceramic capacitor (MLCC) technology, IPDiA is able to deliver similar capacitance values in a much thinner layer.

Overview of technology & passive components

1- Description of the Integrated Passive Devices (IPD) technology

The high-density capacitors are using the third dimension to substantially increase the capacitor surface and thus its capacitance without increasing the capacitor footprint. Figure 1 shows a cross section of the first generation capacitor: the bottom electrode is formed by doped silicon, the dielectric is a thin layer and the top electrode is formed by deposition of a doped layer. Pores in the silicon are realized by dry etching with the so called "Bosch process" [6].

According to the well known formula $C = \frac{\varepsilon_0 \times \varepsilon_r \times S}{e}$, there are several ways to get higher capacitor density: increase the permittivity (ε_r) of the capacitor dielectric, minimize dielectric thickness (e) or increase the surface of the capacitor (S).

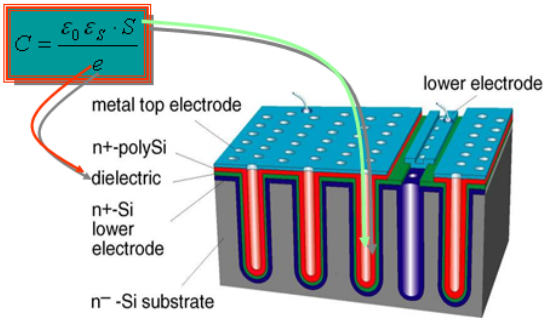

Figure 1: Cross-sectional view of a high density trench silicon capacitor

It is important to notice that the fabrication of these capacitors is requiring only standard process techniques and that the materials used are well known and appreciated for their high reliability.

2- IPD technology versus MLCC: Intrinsic constructions and equivalent electrical models

The IPDiA technology exhibits major benefits to be used as assembly silicon interposer or as passive networks. As the scope of this paper is to focus on intrinsic technologies differences, the Surface Mount Device (SMD) form is used.

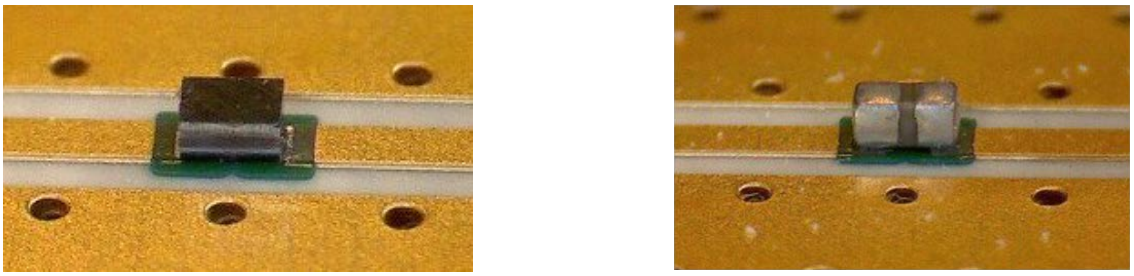

Figure 2: Silicon capacitor used as SMD compared with MLCC SMD

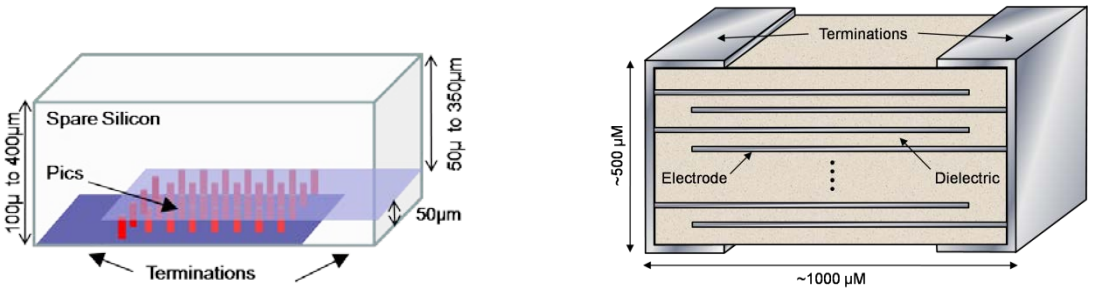

Figure 3: IPDiA Silicon Capacitor & MLCC simplified 0402 SMD construction

The 0402 MLCC component uses its 500µm height to stack multiple electrode layers in order to reach the capacitance targeted (figure 3).
Thanks to its 3D silicon structures, the intrinsic IPDiA capacitor stands in only 50µm thick. This leads to a major difference in the equivalent electrical models.

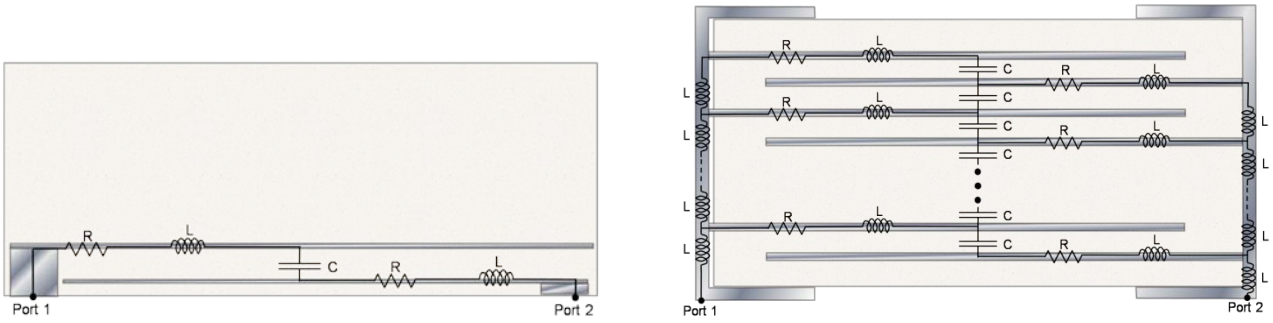

Figure 4: IPDiA Silicon Capacitor (left) & MLCC (right) simplified electrical parasitics related to technologies

The figure 4 shows that the mechanical structure of MLCC capacitors induces more complex parasitic schematic than the Silicon capacitors.

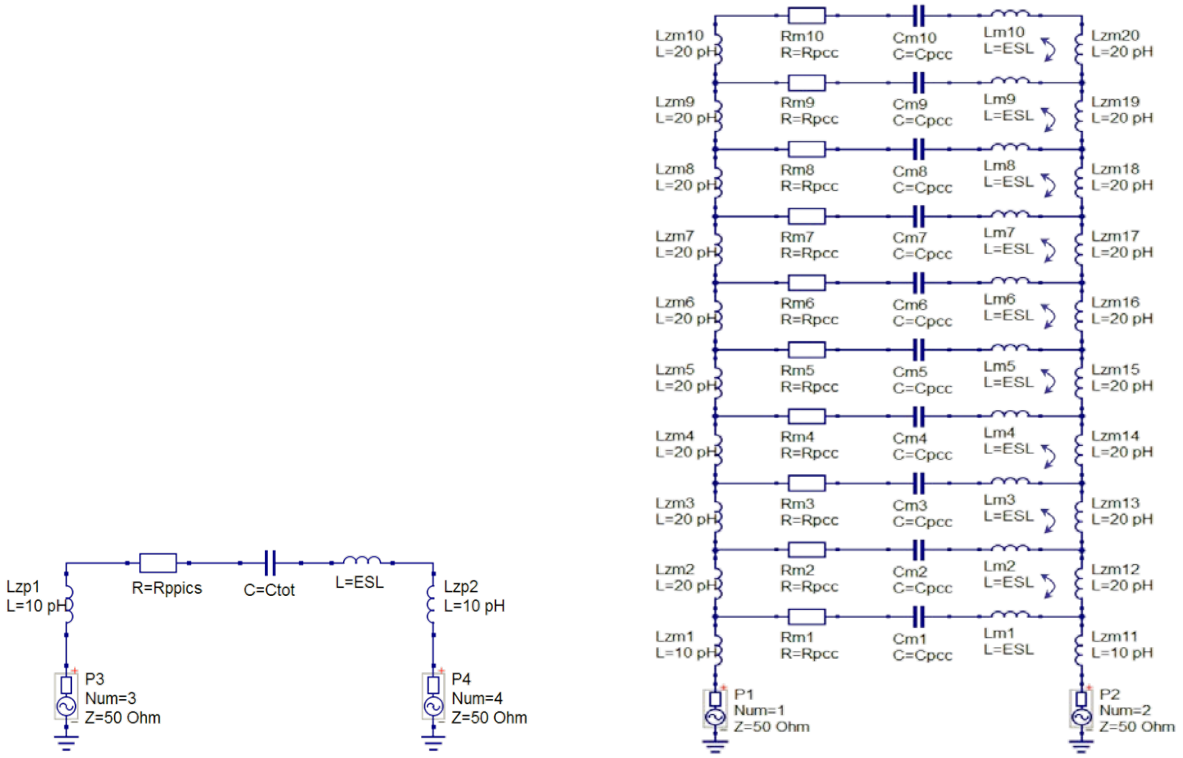

Figure 5: IPDiA Silicon Capacitor (left) & MLCC (right) simplified equivalent electrical model

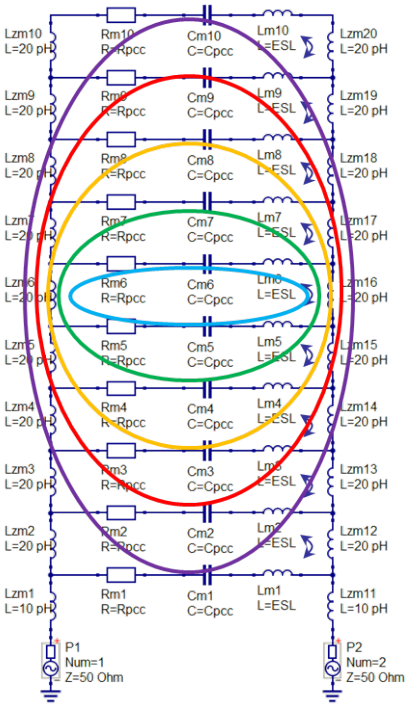

Figure 6: MLCC intrinsic multiple resonant frequencies

The MLCC equivalent electrical model exhibits the inherent multiple resonant frequencies.

3- IPD technology versus MLCC: Simulations of equivalent electrical models

A common way to compare electrical frequency behaviors of broadband capacitors is to simulate scattered parameters.
The insertion losses (S21 in dB) and insertion phase (°) of a 20nF capacitance with overall equivalent electrical parasitics for both technologies have been simulated.

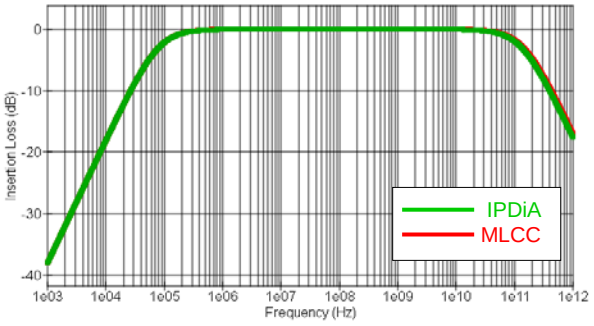

Figure 7: IPDiA Si Cap & MLCC models insertion loss (dB)

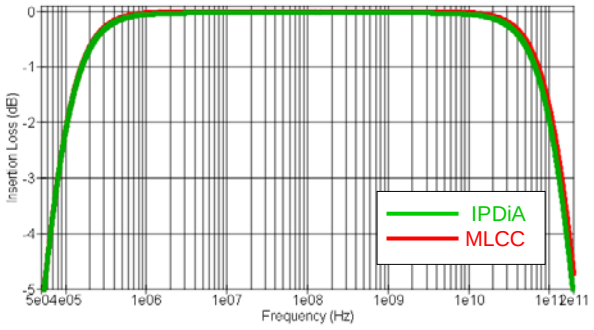

Figure 8: IPDiA Si Cap & MLCC models insertion loss (zoom)

Figure 7 & figure 8 show that the chosen components here have exactly same insertion losses. So the behavior in final application is expected to be the same …

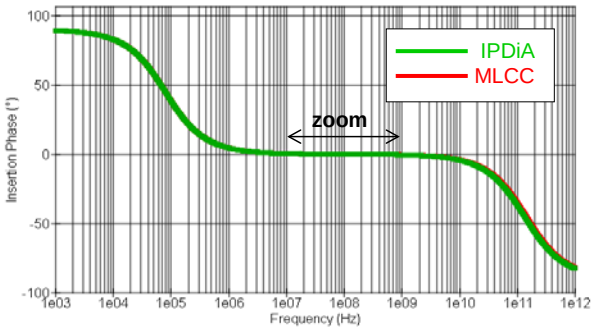

Figure 9: IPDiA Silicon Capacitor & MLCC models insertion phase (°)

Figure 9 shows same temporary conclusion for insertion phase …

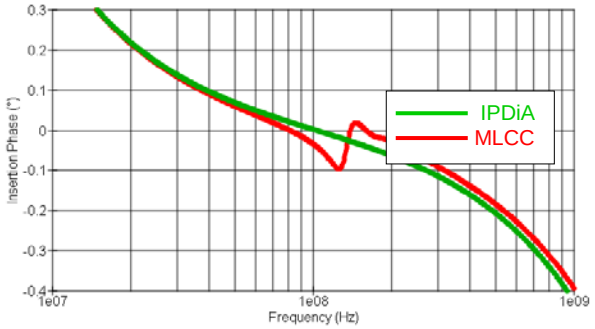

Figure 10: IPDiA Silicon Capacitor & MLCC models insertion phase (zoom)

But figure 10 shows MLCC rapid insertion phase transition around zero degrees which may cause excessive group delay in phase sensitive applications.

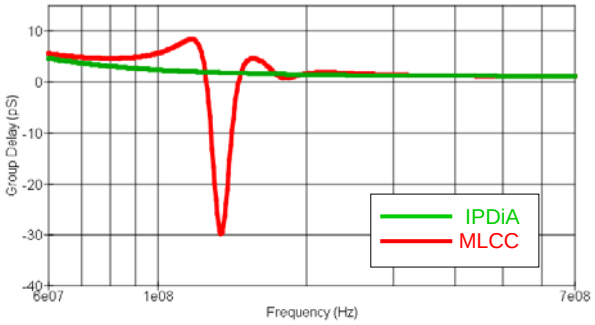

Figure 11: IPDiA Silicon Capacitor & MLCC group delay (pS)

Figure 11 shows definitely a major difference in group delay behaviors. The MLCC capacitor structure is introducing here a frequency dependant group delay of about 30ps. This value has to be compared relatively to a 25Gb/s psk system where phase information is changing up to every 40ps.

Conclusion

Targeting the growing passive component market, several generations of highly integrated capacitors have been successfully developed and industrialized at IPDiA.
Advantages and high performances of this 3D capacitor technology versus its competitors (MLCC) have been demonstrated.
Technology roadmap is focusing on higher capacitor densities and development has already started.

This very high capacitance platform presents lots of interest in different domains; in this paper we have illustrated one of them in the **phase sensitive broadband applications where group delay is key**.

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