Architecture of industrial sensors - interest of silicon passive networks

Sensors are on the way to be smarter and smarter: with more embedded intelligence, the new ones are linked to industrial networks and became extensions of standard computers. In the same time, they have to be more cost efficient and smaller to be implemented everywhere. Last but not least, accuracy and reliability are key factors for components which will control industrial processes.

The various characteristics would be strongly jeopardized by the low reliability of the passive components surrounding the sensing elements and its "intelligence". The reliability of the capacitor as well as the mechanical stresses of handling and soldering standard passive SMD components on the electronics is seen as the Achilles' heel of the sensors.

The "Passive Integrated Connecting Substrate" (PICS)technology can cope with these constraints and open new design opportunities for industrial sensors.

Definition of the Integrated Passive Devices

The PICS technology provides a highly efficient way to integrate several passive components such as high-Q inductors, resistors, accurate planar MIM capacitors and trench MOS capacitors in a single silicon die. This is possible thanks to perfectly controlled and accurate processes, similar to the ones used to manufacture microprocessors or memory chips. The level of technology required to manufacture those Silicon Passive component arrays is the same as the one required for manufacturing CMOS die.

It is important to point out that the fabrication of silicon passive arrays only require standard semiconductor process techniques and the materials used are well known and appreciated for their high reliability.

The main benefits of this technology are miniaturization and stability of performances facing to environmental variations, as well as reliability and global manufacturing cost reduction ("Total Cost of Ownership").

Moreover this process is providing a fully CMOS compatible solution for the integration on chip or multiple chip modules.

Miniaturization of sensors

Even if one or two sensors were enough to monitor an industrial process, it is not today sufficient to do such a work. The main challenge of process control is finally to be ubiquitous in order to improve the global efficiency. This can only be done by increasing the number and types of used sensors.

Concerning the technologies, it can be stated that miniaturization will continue in order to increase the compactness of the sensors and in order to minimize their volume and their weight into the industrial systems.

The miniaturization will be associated with new integration technologies. This will follow the strategic evolution called "More than Moore" that is considered as the most important industrial segment for the future.

In order to tackle both miniaturization and integration, the technologies have to stack both sensing, communication and signal processing capabilities into one package.

Passive silicon networks

First step into miniaturization and integration, the passive networks onto a silicon substrate are a solution to reduce dimensions of sensors.

In addition to the integration scale provided by the PICS technology, sensor applications may also benefit from the PICS packaging form factor.

The usage of the PICS component into a sensor is one miniaturization way that Printed Circuit Board (PCB) is not able to achieve so far. The design rules applicable to the PCB technology have their own limitation in terms of metal stack width and spacing, SMD package dimension, necessary footprint surface for a proper soldering process as well as existing placement accuracy provided by most of the SMT industrial equipment roadmap oriented to "unit per hour improvement" (Cost of Ownership).

Design Rules (all dimensions in µm)	**LTCC**	**Laminate**	**PICS**
Minimum line width	50	65	3
Minimum line space	50	65	5

Table 1 - Typical design rules for LTCC, Laminate and Silicon IPD based circuits

Thanks to such PICS technology, it is possible to shrink circuitries and to drastically reduce the number of components implemented onto the boards.

As one more step ahead, the package-less approach of WL-CSP architecture may allow the best miniaturization factor of PICS usage with optimum pad size and pitch suitable for the specific customer application design rules.

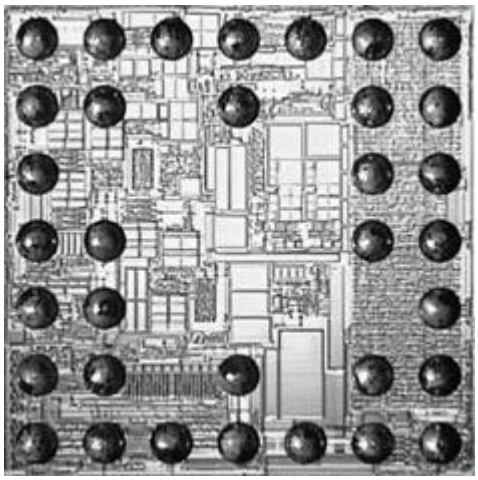

Figure 1 - Example of a PICS die with the WL-CSP architecture

As ASICs regularly used into smart sensing applications, complete passive functions (filtering, decoupling) would be simply integrated into sensors as standard building blocks.

This kind of solution will have several positive impacts on the sensor designs:

- to reduce the number of needed components will improve both global cost of the final products and their reliability;
- standardized designs of passive functions could be "copy & paste" from one sensor series to an another one with limited costs.

Interposer approach

As a normal evolution of the WL-CSP approach, the PICS technology allows the creation of complete "System-in-Package" (SiP) architecture. In these cases, the PICS dies will be used as interposers in place of laminates or ceramic boards.

In that architecture, the PICS devicesare acting as a third-function platform capability:

- firstly to integrate passive component onto the silicon die (PICS function),
- secondly to support external die (Substrate function)
- and finally to interconnect external die and PICS together (Interconnection function).

This last function is dedicated to 2D interconnection at the PICS surface (metal tracks) (Figure 2), as well as to 3D interconnection side to side by conductive TSV technology (Trough Silicon Via).

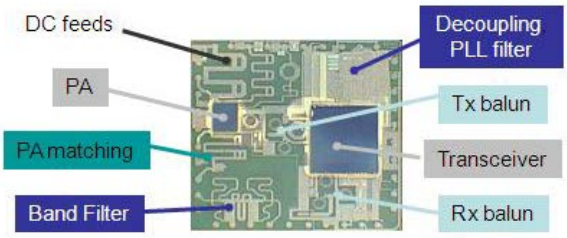

Figure 2 - Example of 2D PICS interposer with active dies

Thanks to die stacking, the miniaturization of sensors can be improved a step further.

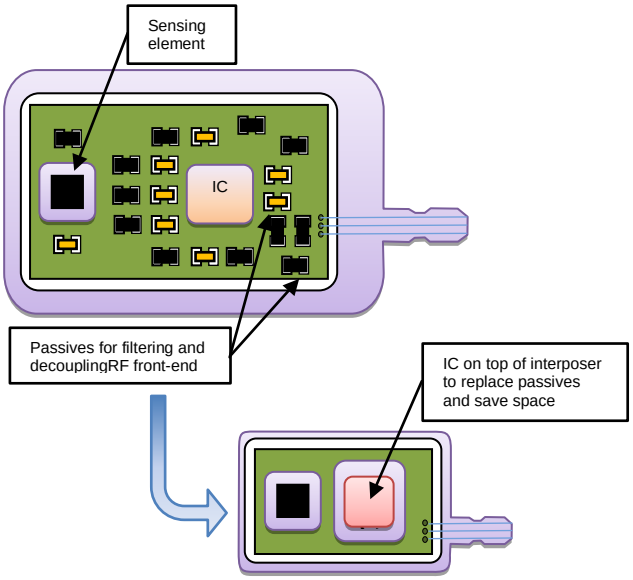

Figure 3 - Architecture evolution with PICS interposer and die stacking

Depending on the environmental constraints expected for the sensors or the selected assembly processes, the interposers and stacked dies could be implemented directly onto other substrates (WL-CSP approach) or packaged.

In any case, these highly integrated sub-systems would be used as standard components in the sensors.

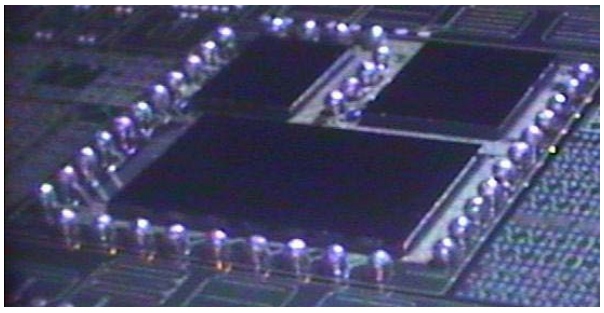

Figure 4 - Sub-system on PICS interposer

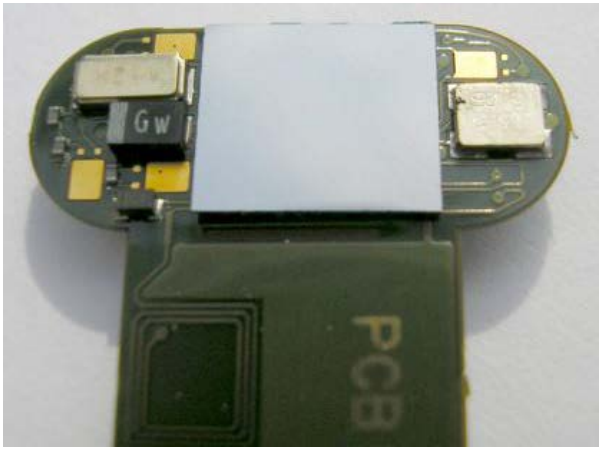

Figure 5 - Its integration as a single component into a sensing system

Performances and advantages of silicon capacitors

This PICS technology exhibits inherent good performance with very high stability (temperature, voltage, ageing), superior reliability and very low parasitic elements (ESR, ESL). It is an excellent alternative to discrete components (MLCC and tantalum capacitors) as its performance is better in a much smaller volume.

Stability

The temperature performance exceeds MLCC and tantalum capacitors, like silicon capacitors, are very stable over the -50°C / +200°C temperature range (<0.002%) ().

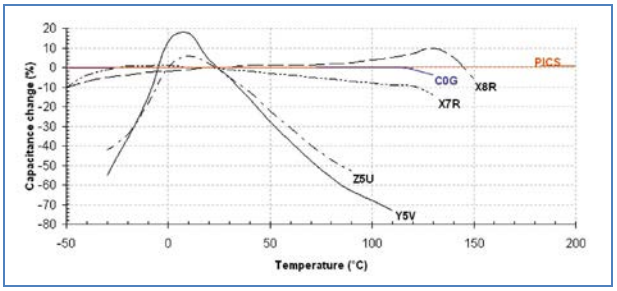

Figure 6 - Temperature performances comparison with various types of MLCC

The capacitance value is also very stable whatever the DC voltage variation applied on the electrodes is, as depicted in Figure 2 (<0.1%/V). There is no trade-off needed between density and stability: “Integrated Passive” technology offers both - unlike MLCC and tantalum components.

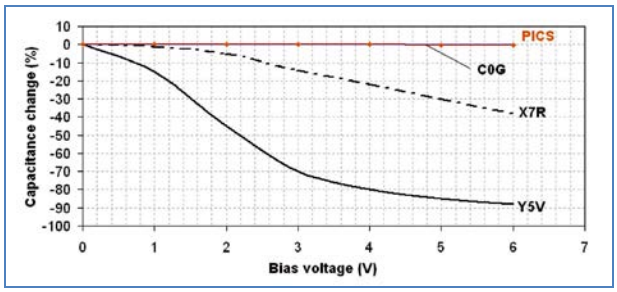

Figure 7 - Voltage stability performances comparisons with various types of MLCC

Reliability

The capacitors are essential passive components in electronic and they constitute 30% of the passive components world market.

Their main default is their relatively high rate of failure compared to the other components (passives or actives). Information on component failure rates provides the manufacturer with a basis for reliability forecasts and allows him to estimate future service requirements. The failure rate depends on the failure criteria, the load and the operating time. The dimension of the failure rate is the reciprocal of time and the unit used is 10–9 / h = 1 FIT (failure in time).

The main advantage of the capacitor built in a silicon passive array is the amazing reliability that exceeds all current market standards.

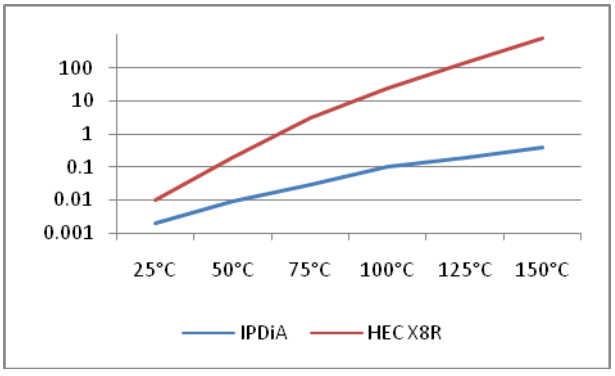

Figure 8 - FIT rates calculated at a "60%" confidence level

More and more industrial sensors have to withstand operating temperatures close to 150°C. Standard capacitors cannot have a long operating life time in such environments, which means the reliability and lifetime of the sensors using them will be decreased sharply.

Silicon capacitors are able to cope with harsh environment conditions such as those encountered in down hole equipment or close to industrial ovens, with temperatures going higher than150 °C.

The projected median time-to-failure is well in excess of 2,000,000 years for SSL devices using the silicon capacitors at 50% of the maximum operating voltage and 85°C (Table 2).

MTTF(years) as function of operating voltage	100% Max. V @ 37°C	50% Max. V @ 37°C	50% Max. V @ 85°C
X7R "0402" size 100 nF	4.40E+04	6.20E+05	2.5E+03
Silicon capacitor "0402" size 100nF	4.16E+06	6.99E+07	2.10E+07

Table 2 - Median time to failure / Silicon capacitor vs. X7R

High density silicon capacitors

Because the PICS technology uses the third dimension to create passive components, the PICS high-density capacitors substantially increase the surfaces of capacitor electrodes and thus its capacitance without increasing the capacitor footprint.

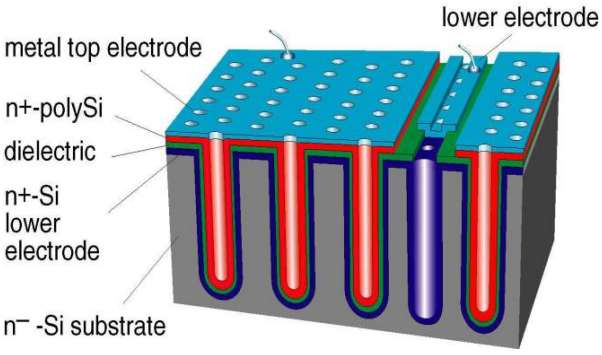

Figure 9 – Cross-sectional view of IPDiA high density capacitor

Figure 9 shows a cross section of the first generation PICS capacitor: the bottom electrode is formed by doped silicon, when the dielectric is a thin layer and the top electrode is formed by deposition of a doped layer. Pores, with high aspect ratios up to 60 with a typical width of 1 µm, in the silicon are realized by dry etching with the so called "Bosch process".

According to the below well-known formula,

$$C = \frac{\varepsilon_0 \times \varepsilon_r \times S}{e}$$

there are several ways to get higher capacitor density:

- increase the permittivity (ε_r) of the capacitor dielectric,
- minimize dielectric thickness (e),
- or increase the surface of the capacitor (S).

Thanks to this 3D approach, IPDiA released this process for mass production and launched derivative options with higher breakdown voltage (Table 3) and demonstrated the feasibility to reach 550nF/mm² at 11 volts breakdown

Capacitor density	Breakdown voltage
250 nF/mm²	11 Vdc
100 nF/mm²	30Vdc
80 nF/mm²	17 Vdc
25 nF/mm²	28 Vdc
20 nF/mm²	50 Vdc
6 nF/mm²	150 Vdc

Table 3 - Capacitor density vs. breakdown voltage

Compared to standard MLCC capacitors, PICS silicon capacitors are providing the stability of well-known C0G components with a "10x"superior density. In the same time, these components can thinned low to 100 µm which allows to stack them directly onto the sensing elements or the "signal treatment" electronics.

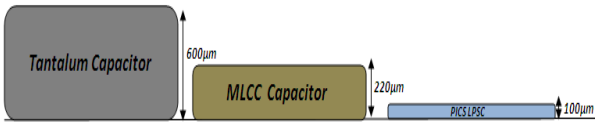

Figure 10 - Thickness comparison

PICStechnology for smarter new sensors

More and more sensors have to be used in industrial processes. In the same time, their reliability, performances, dimensions and costs have to be improved to better cope with new applications and constraints.

Thanks to their intrinsic great characteristics (stability, low ageing, extreme integration, compatibility with high temperatures), Passive Integrated Silicon Subtrates (PICS) are opening new ways and offering technical opportunities for the design of smarter and more integrated sensors.