Assembly Note Silicon Capacitor

Assembly by reflow

Rev1.2

This document describes the attachment techniques recommended by Murata Integrated Passive Solutions for their Silicon Capacitors (including ones with SAC305 terminations) on the customer substrates for reflow process, as well as for flip-chip IPD (Integrated Passive Device) assembled by reflow. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact Murata (mis@murata.com).

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1. Handling Precautions and Storage

Silicon dies must always be handled with precaution in a dedicated environment for assembly. Regarding silicon capacitors, after opening of the packing, the remaining quantities have to be repacked immediately after any process step, in the same conditions as before the opening (ESD bag + N2 is usually preferred).

Avoid storing the capacitors in the following conditions:

- Ambient air containing corrosive gas (Chlorine, Hydrogen sulfide, Ammonia, Sulfuric acid, Nitric oxide, etc.)
- Ambient air containing volatile or combustible gas
- In environments with a high concentration of airborne particles
- In liquid (water, oil, chemical solution, organic solvents, etc.)
- Under direct sunlight
- In freezing environment

To avoid contamination and damage like scratches and cracks, our recommendations are:

- Die must never be handled with bare hands
- Avoid touching or scratching the active face with tools that are not adapted
- The mechanical pressure has to be limited
- Do not store and transport die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD-controlled environments

Plastic tweezers or a soft vacuum tool are recommended to handle our Silicon dies.
For more information about handling, please refer to the dedicated application Note "Recommendation to handle bare dies".

Standard packing is tape & reel but silicon capacitors can be provided within waffle pack, gelpak or sawing frame. Please contact Murata for drawing and references (mis@murata.com).

2. Pad Opening and Solder excess

The top surface of the Murata silicon capacitors is protected with a passivation. The finishing of the contact pads is in nickel gold (generally 5µm nickel and 0.2µm gold) conforming with the soldering process.

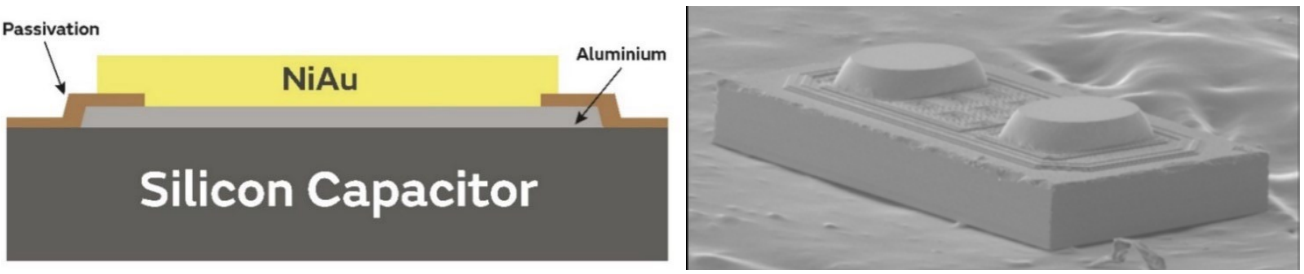


Figure 1: Left side - Simplified view of a Si-cap pad for reflow; right side – SEM view of a Si-cap with SAC305 terminations

Murata recommends having an opening on the PCB substrate which matches the pads of the capacitor (size, position and spacing), what Murata calls “mirror-pad” – see figure 2, 3, 6 and 8.

On the PCB substrate, the metal layer can be larger than the varnish coating opening size, but in this case, the varnish coating opening has to be mirror with the pad size of the capacitor. No need to change the metal landing pad of the PCB substrate, only the opening in the varnish coating needs to be adjusted with Solder Mask Defined design (see figures 6 and 7). These recommendations will improve the die placement, tilting and will avoid the contact between the solder paste and the bare silicon die – see figure 4 and 5.

2.1. Solder joint after reflow

Figure 2: Non-solder mask defined Assembly

Figure 3: Solder mask defined Assembly

Silicon capacitor solder process is specific. Solder paste must not be in contact with the side of the silicon capacitor. Side of silicon capacitor must not be in contact with the landing pad. Correct assembly can be checked with the leakage current level of the capacitor after assembly. Please also check Figure 17 for mechanical measurement procedure of the solder joint after reflow.

Tilt acceptance criteria is defined by customer and target application. Please contact Murata for more information.

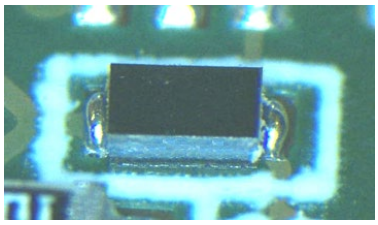


Figure 4 : Example of mis-assembly due to solder paste excess

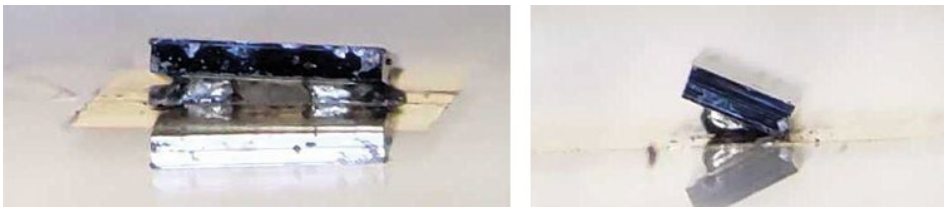


Figure 5 : Si-cap tilting examples, please note the solder excess

2.2. Solder Mask design

On the customer substrate, Murata recommends SMD (Solder Mask Defined) to control the solder flowing on the tracks. Customer must ensure the opening and placement tolerances of the solder mask remain compatible with the silicon capacitor pad dimensions.

Please take good note of the difference between Si-caps with NiAu finishing, that need solder paste on the PCB substrate (left side of figures 6 and 8) and Si-caps with SAC305 terminations (or SAC305 bump) that require no solder paste, but only flux (right side of figures 6 and 8). Solder paste and flux deposition methods are described on Section 4.

2.2.1. Solder Mask Defined

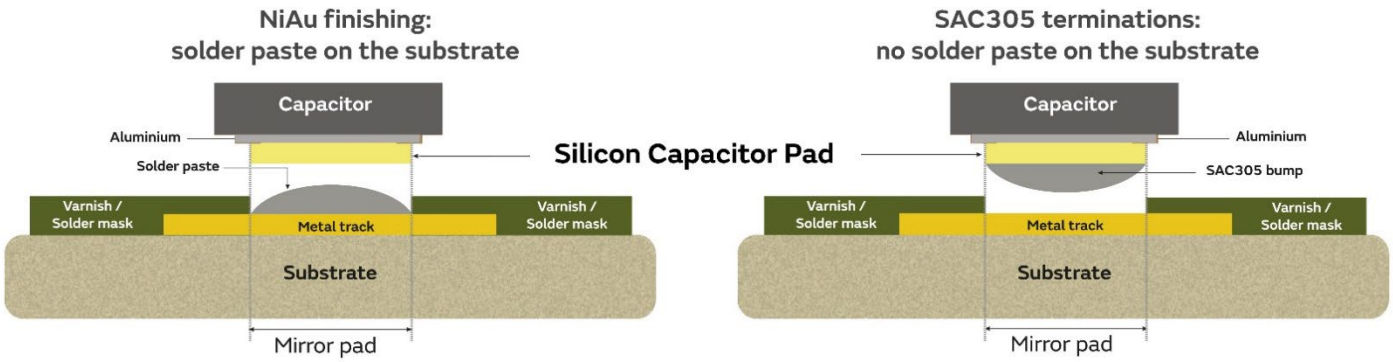


Figure 6: Simplified view of SMD assembly from the side (only one pad is shown here)

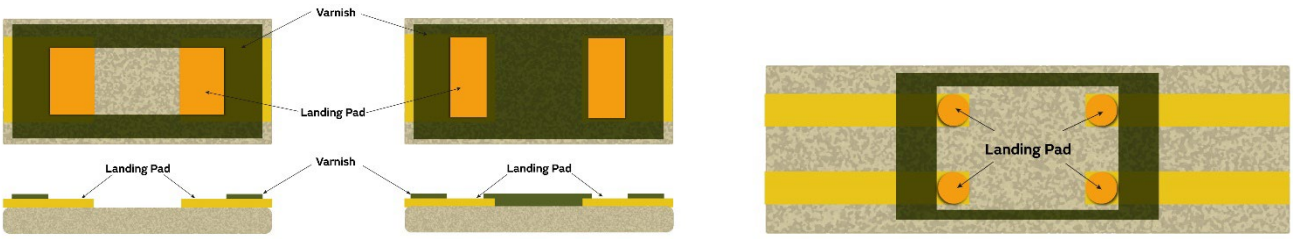


Figure 7: Examples of SMD designs, 2 pads on the left, 4 pads on the right

2.2.2. Non Solder Mask Defined

Figure 8: Simplified view of NSMD assembly from the side (only one pad is shown here)

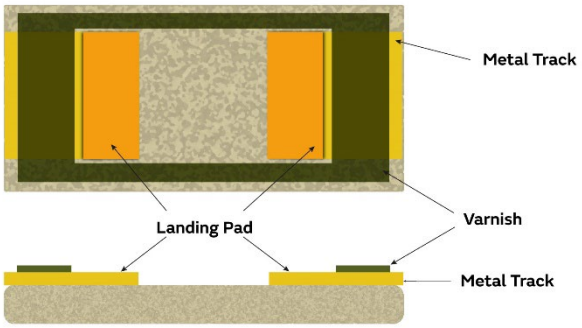


Figure 9: Example of NSMD designs with 2 pads.

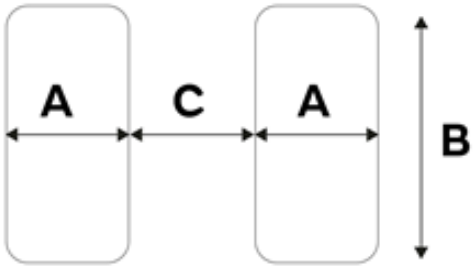
Note : Varnish between the two landing pads can also be applied

2.3. Pad opening

Landing pads for the substrate and die pad dimensions for the Murata silicon die:

Silicon Capacitor Type	Capacitor size (µm)	A (µm)	B (µm)	C (µm)
0201M	600 x 300	100	150	200
0201	800 x 600	150	400	300
0402	1200 x 700	300	500	400
0402M	1000 x 500	260	300	280
0204M	500 x 1000	75	800	200
0603	1800 x 1100	400	900	800
0404M	1040 x 1040	300	850	240
0805	2200 x 1400	500	1200	1000
1206	3400 x 1800	600	1600	2000
1812	4700 x 3600	900	3400	2700

Table 1: Landing pads for capacitors with two pads



Note: For RF and broadband design, please refer to application note "Design guidelines for transmission lines of UBB SiCap"

Silicon Capacitor Type	Capacitor size (µm)	A (µm)	B (µm)	C (µm)
0402M	1000 x 500	90	250	700

Table 2: Landing pads for capacitors with four pads

Note: For RF and broadband design, please refer to application note "Design guidelines for transmission lines of UBB SiCap"

For components with a different number of pads, similar rules can be considered as a base. Please contact Murata for additional support.

3. Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking but manual placement can also be done.

Using a soft tip tool (like rubber) is particularly preferred for the die manipulation. Also, Si-caps are lighter and mainly thinner than other stand-alone capacitor technologies, so please consider reducing the pressure force applied during placement on the board to avoid mechanical defects. As a rule of thumb, you may consider halving the pressure for your first evaluations and increasing it only if necessary.

For more details on picking and placement applied forces and tip tool selection, please look at the dedicated Application Note "Recommendation to handle bare dies".

4. Mounting Process Flow

4.1. Silicon Capacitors with SAC305 terminations

The bumps need flux to activate the soldering reflow. The following processes are compatible:

4.1.1. Flux dipping

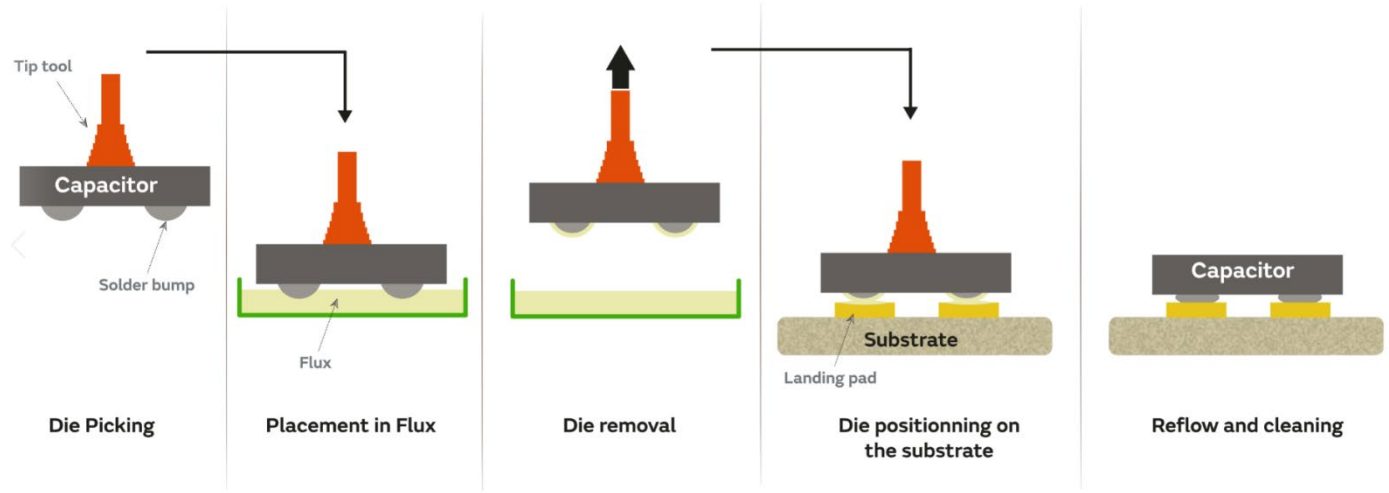


Figure 10: Assembly process by flux dipping on bumped capacitor with SAC305 terminations

4.1.2. Fluxing by stamping

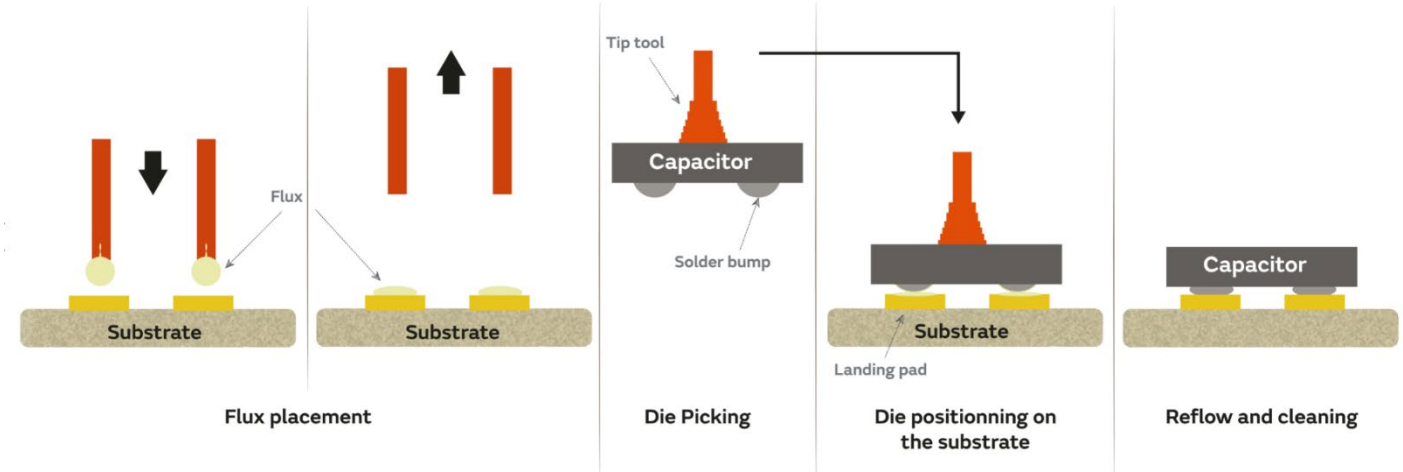


Figure 11: Assembly process by flux stamping on bumped capacitor with SAC305 terminations

4.1.3. Fluxing by spraying

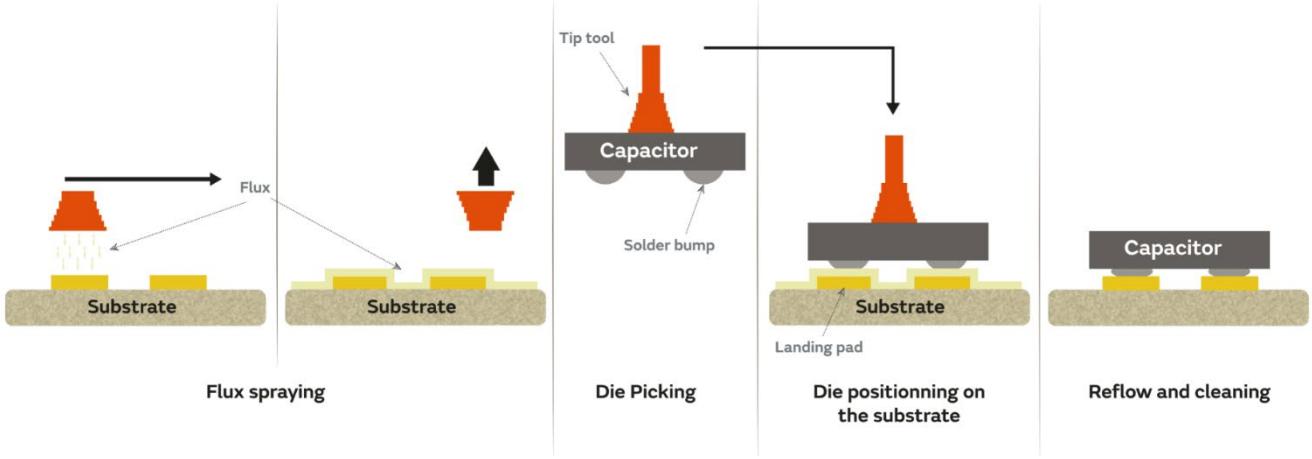


Figure 12: Assembly process by flux spraying on bumped capacitors with SAC305 terminations

4.1.4. Fluxing by screen printing

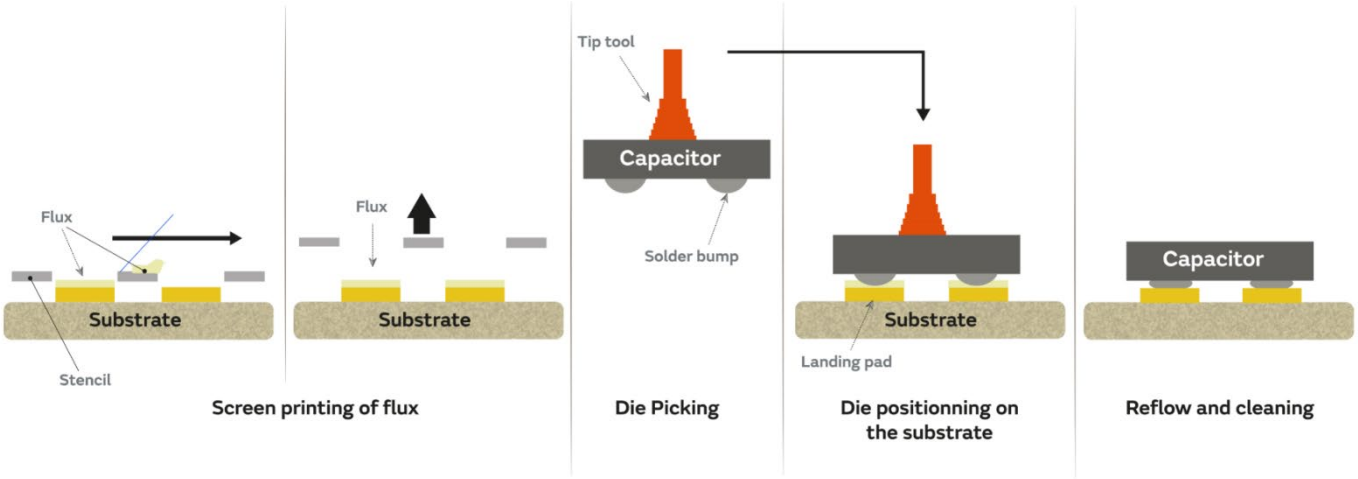


Figure 13: Assembly process by screen printing of flux on bumped capacitors with SAC305 terminations

4.2. Silicon Capacitors with NiAu finishing

We recommend placing the solder paste by screen printing directly on the substrate landing pads:

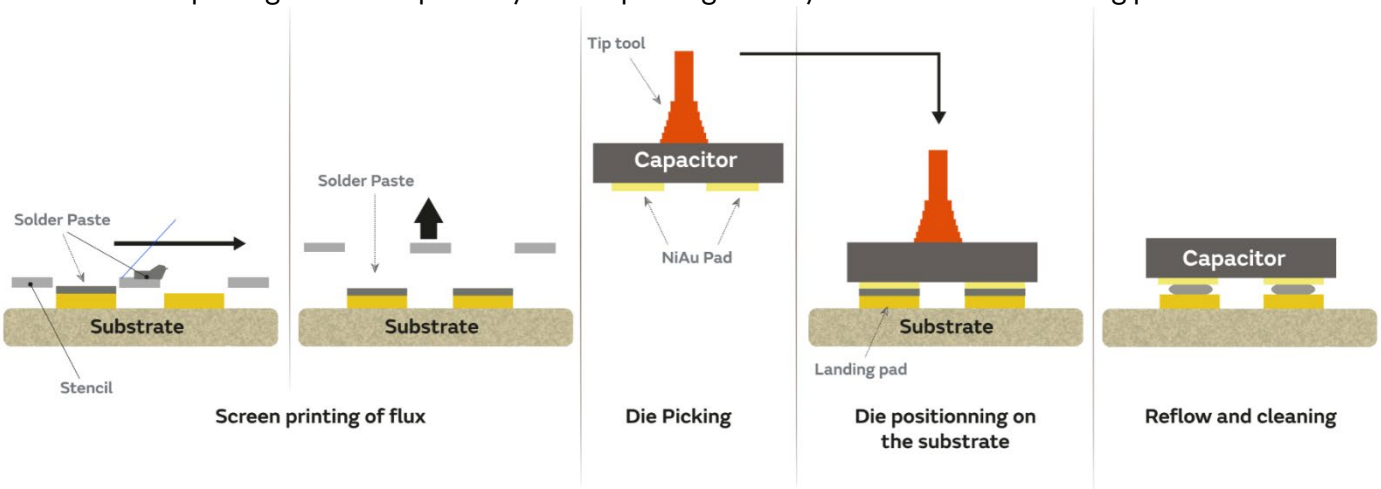


Figure 14: Assembly process by screen printing of solder paste on silicon capacitor

5. Solder print material for Silicon Capacitors with NiAu finishing

SAC305 is commonly used and recommended but other materials compatible with the die pad finishing are also possible. Please contact Murata.

Murata recommends using a type 6 powder size. Type 5 can be used depending on the customer PCB design and application. Type 4 is not recommended for 0201M and smaller pad dimensions. Depending on the die pad size, powder size can be adjusted. However, type 6 compared with type 4 limits the risk of tilting of the capacitor for smaller pad dimensions (refer to part 2).

Alloy	Composition	Solidus	Liquidus	Comments
SAC305	Sn 96.5%, Ag 3%, Cu 0.5%	217°c	217°c	Eutectic
Sn63	Sn 63%, Pb 37%	183°c	183°c	Eutectic Only for allowed applications
AuSn	Au 80%, Sn 20%	280°c	280°c	Eutectic - High temperature
SnPb	Sn 5%, Pb 95%	308°c	312°c	High temperature Only allowed for specific applications

Table 3 : Examples of solder print materials for reflow

For flux cleaning recommendations, please refer to section 8 of this document.

6. Stencil design recommendations

Murata advises in every case that the width of the stencil opening (referred as 'W') should be larger than 5 times the average powder size of your soldering material. This, in order to correctly fill the stencil pocket.

Murata follows the IPC-7525 standard and quantifies the stencil grade based on ratio between stencil's area ratio (AR), aspect ratio (AS) and thickness. Please look at the following formulas and tables to find the stencil grade we recommend.

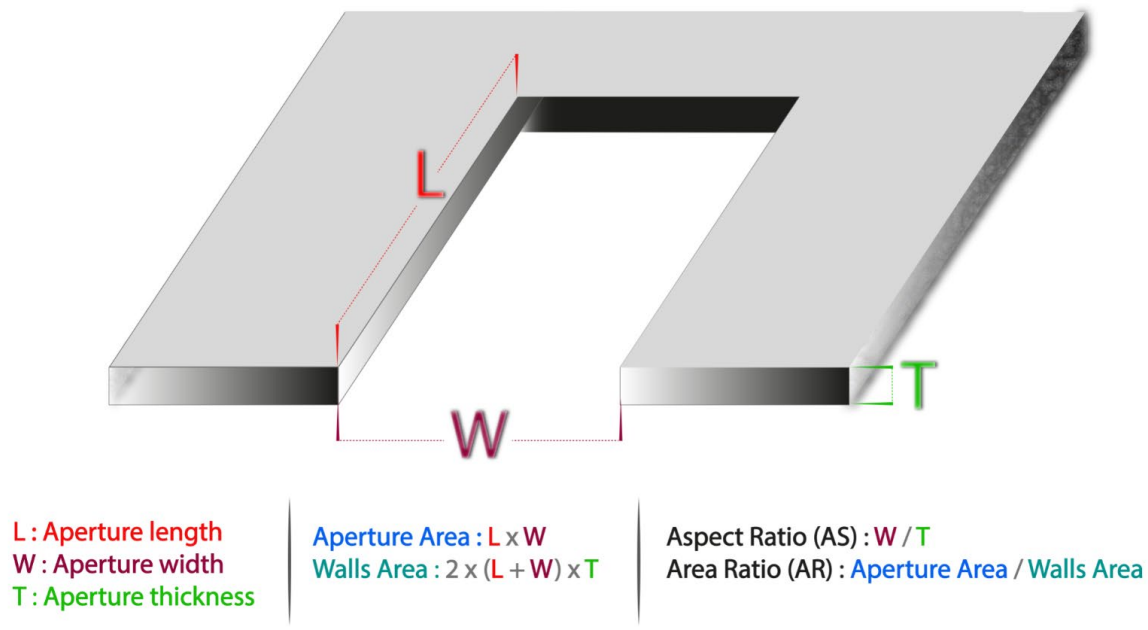


Figure 15: Definitions for stencil aperture

Please compare your stencil's desired thickness, aspect and area ratio with the following tables to define which grade we advise. Please consider the highest grade you will find from each of the three criteria.

Area ratio (AR)	REGULAR	MEDIUM-HIGH	HIGH
	0.66	0.5	0.4
Asepct ratio (AS)	REGULAR	MEDIUM-HIGH	HIGH
	1.5	1.2	1.0
Thickness	REGULAR	MEDIUM-HIGH	HIGH
	110µm	75µm	

Table 4: Stencil grade selection criteria per Area ratio, Aspect ratio and Thickness

Examples of medium-high grade stencils include electroformed or laser-cut technologies.

Examples of high grade stencils include plasma or medium-high grade with surface treatment technologies.

For SAC305, a solder joint thickness of 40 µm +/-10 is targeted to limit the risk of contact between the solder paste and the side of the capacitor. Limiting solder joint thickness will also avoid an excessive tilting of the capacitor, especially for small components. Please contact Murata for other soldering materials and thinner solder joints.

For example, below are some stencil designs advised by Murata (SAC305 type 6 with 50% of flux by volume):

Silicon Capacitor Case Size	Stencil opening size per pad (in µm)	Stencil thickness (in µm)	Stencil grade (roughness and opening profile)
0201M	130 x 200	50	high
0201	150 x 320	100	medium high
0402M	240 x 260	100	medium high
0402	260 x 369	125	regular
0204M	90 x 750	75	medium high
0603	300 x 768	125	regular
0404M	250 x 750	125	regular
0805	400 x 960	125	regular
1206	500 x 1229	125	regular
1812	650 x 3012	125	regular

Table 5: Advised stencil designs per type for capacitors with two pads

Note: Opening sizes are to be adjusted according to flux content and type used.

Silicon Capacitor Case Size	Stencil opening sizeper pad (in µm)	Stencil thickness (in µm)	Stencil grade (roughness and opening profile)
0402M	120 x 120	40	high

Table 6: Advised stencil designs per type for capacitors with four pads

Note: Opening sizes are to be adjusted according to flux content and type used.

For components with a different number of pads, similar rules can be considered as a base. Please contact Murata for additional support.

7. Reflow by soldering

7.1. Reflow recommendations at regular temperatures

Murata recommends convection reflow but vapor phase reflow and infrared reflow could be also used.

The reflow process must be carried out in accordance with the JEDEC J-STD-020-E standard for low temperature reflow like SAC305. For higher temperature solder pastes, like AuSn, please refer to the dedicated Application Note “Silicon Capacitors assembly by reflow with high temperature soldering material”.

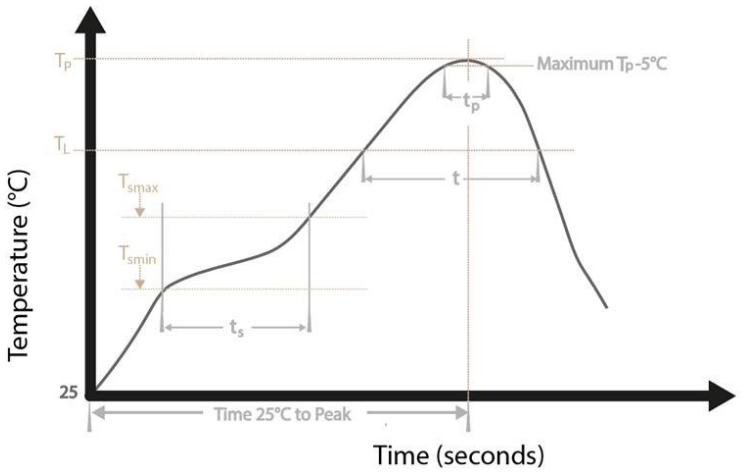


Figure 16: General reflow profile for regular temperature solder pastes (based on J-STD-020-E)

Profile feature	SAC305 (Lead-Free Assembly)	Sn63 (for allowed applications only)
Preheat/soak		
Temperature min (Ts min)	150°C	100°C
Temperature max (Ts max)	200°C	150°C
Time (ts) from (Ts min to Ts max)	60 to 120 s	60 to 120 s
Ramp-up		
Ramp-up rate (TL to Tp)	3°C/s maximum	3°C/s maximum
Liquidus temperature(TL)	217°C	183°C
Time (t) maintained above TL	60s to 150 s	60s to 150 s
Time (tp) within 5°C of the maximum temperature	30 seconds max	20 seconds max
Peak package body temperature (Tp)	260°C max	235°C max
Time 25°C to peak temperature	8 minutes maximum	6 minutes maximum
Ramp-down		
Ramp-down rate (Tp to TL)	6°C/s maximum	6°C/s maximum

Table 7 : Recommended values for regular temperature reflow

According to JEDEC J-STD-020E, the user's peak temperature must not exceed Tp and the time tp has to be respected. Values included in the above table may vary with the soldering material.

For flux cleaning recommendations, please refer to section 8 of this document.

7.2. Procedure for solder joint measurement (after reflow)

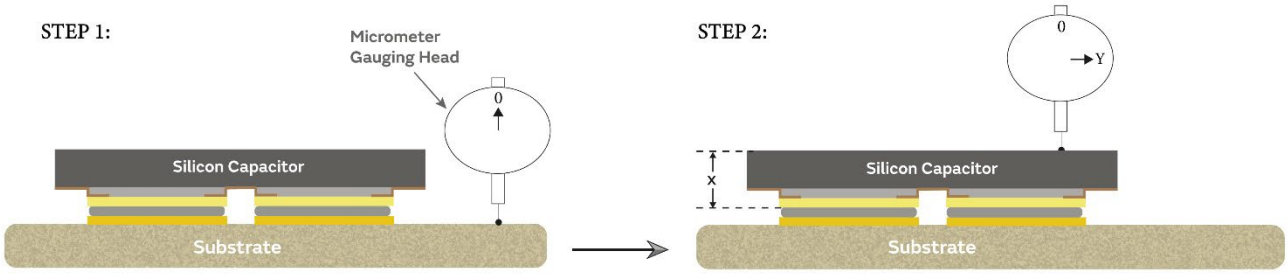


Figure 17: Solder joint measurement protocol

As step 1, the zero-level reference is made at PCB surface.
As step 2, the gauge shows 'Y' as the thickness of the whole assembly.
X represents the thickness of the silicon capacitor, including the silicon capacitor pad.
One should subtract X as well as the PCB landing pad's thickness from Y to get the measured solder joint.

$$Measured\ solder\ joint\ thickness = Y - X - landing\ pad\ thickness$$

8. Cleaning after reflow

For appropriate removal of residual flux, proper cleaning equipment, conditions and solvent must be used. This prevents any residual flux or other foreign substances causing deterioration of electrical characteristics and the reliability of the capacitors.

Water soluble and no clean flux can be used. In case of water-soluble flux, please refer to the solder paste supplier for the cleaning and flux removal. For optimum results, it is recommended to remove the flux immediately after reflow to avoid a potential issue of current leakage or short circuits.

However, Murata does not recommend to use excessive conditions for ultrasonic oscillation, water or air pressure during cleaning which can cause reliability issues. Before starting your production process, please test your cleaning system.

Revision history

Revision	Date	Description	Author
1.0	22/03/2021	Document Creation	C.Muller
1.1	24/08/2022	Addition of chapter 8 dedicated for cleaning recommendations Formatting update	K. Dubois
1.2	23/01/2023	Added storage recommendations to chapter 1	K. Dubois

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