Assembly Note Silicon Capacitor

Assembly by reflow

Rev1.42

This document describes the attachment techniques recommended by Murata Integrated Passive Solutions for their silicon capacitors on customer substrates for reflow processes, as well as for flip-chip IPDs (Integrated Passive Devices) assembled by reflow. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact Murata (mis@murata.com).

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1. Handling Precautions and Storage

Silicon dies must always be handled with precaution in a dedicated environment for assembly. Regarding silicon capacitors, after opening the packing, the remaining quantities must be repacked immediately after any process step, under the same conditions as before opening (ESD bag + N2 is usually preferred).

Avoid storing the capacitors under the following conditions:

- Ambient air containing corrosive gas (chlorine, hydrogen sulfide, ammonia, sulfuric acid, nitric oxide, etc.)
- Ambient air containing volatile or combustible gas
- In environments with a high concentration of airborne particles
- In liquid (water, oil, chemical solution, organic solvents, etc.)
- Under direct sunlight
- In freezing environment

For specific storage conditions, refer to the dedicated Application Note "Storage and shelf life conditions".

To avoid contamination and damage such as scratches and cracks, our recommendations are:

- The die must never be handled with bare hands
- Avoid touching or scratching the active face with unsuitable tools
- Mechanical pressure must be limited
- Do not store and transport the die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD-controlled environments

Plastic tweezers or a soft vacuum tool are recommended to handle our Silicon dies.
For more information about handling, refer to the dedicated Application Note "Recommendations handling bare dies".

Standard packing is tape & reel but silicon capacitors can be provided within waffle pack, gelpak or sawing frame. Please contact Murata for drawing and references (mis@murata.com).

2. Pad Opening and Solder excess

The top surface of the Murata silicon capacitors is protected with a passivation coating. The finishing of the contact pads is nickel gold (generally 5 µm nickel and 0.1 µm gold) conforming with the soldering process (see Figure 1).

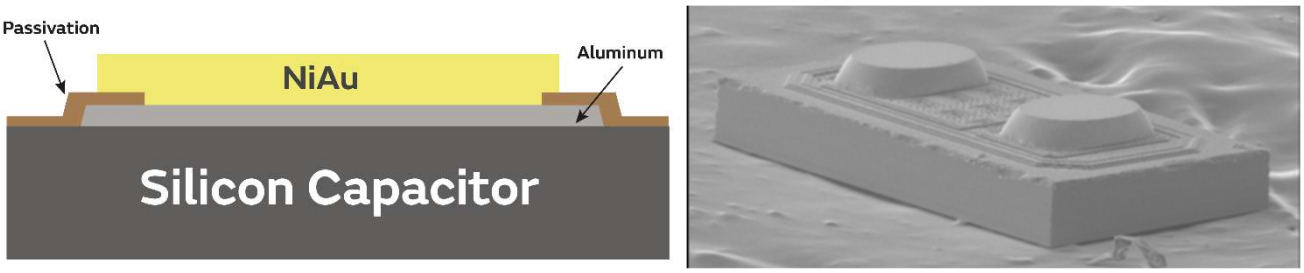


Figure 1: Left side - Simplified view of a Si-cap pad for reflow; right side – SEM view of a Si-cap with SAC305 terminations

There is no need to change the metal landing pad of the PCB substrate, only the opening in the varnish coating needs to be adjusted with Solder Mask Defined design (see Figure 6, 8, 9, 10 and 11). These recommendations will improve the die placement, tilting and will avoid contact between the solder paste and the bare silicon die (see Figure 4 and 5) .

2.1. Solder Joint after Reflow

Figure 2: Non-solder mask defined Assembly

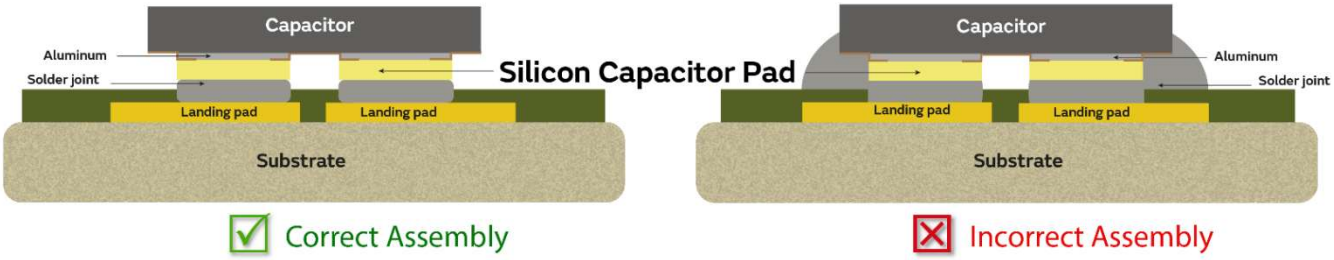


Figure 3: Solder mask defined Assembly

The silicon capacitor solder process is specific. Solder paste must not be in contact with the side of the silicon capacitor. The side of the silicon capacitor must not be in contact with the landing pad. Correct assembly can be checked with the leakage current level of the capacitor after assembly. Please also check Figure 19 for the mechanical measurement procedure of the solder joint after reflow.

The tilt acceptance criterion is defined by the customer and the target application. Please contact Murata for more information.

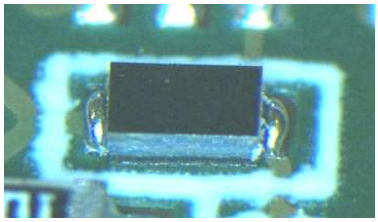


Figure 4 : Example of mis-assembly due to solder paste excess

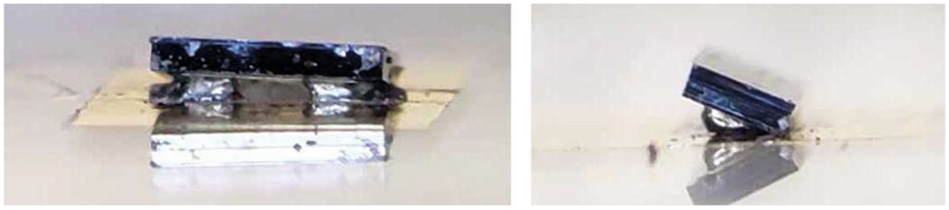


Figure 5 : Si-cap tilting examples, please note the solder excess

2.2. Solder Mask Design

On the customer substrate, Murata recommends SMD (Solder Mask Defined) to control the solder flowing on the tracks. The customer must ensure that the opening and placement tolerances of the solder mask remain compatible with the silicon capacitor finishing (UBM) pad dimensions (see Figure 8, 9, 10 and 11).

Special attention must be paid to the thickness of the solder mask. If the solder mask is too thick, the capacitor body may stand on the solder mask, the bumps would not touch the PCB landing pads and there will be no electrical contact (see Figure 9 and 11).
In case of SMD (Solder Mask Defined) landing pads (see Figure 6), the solder mask thickness must be lower than the height of the bumps (SAC305).
In case of NSMD (Non Solder Mask Defined) landing pads (see Figure 7), make sure that the solder mask is thinner than the bumps and/or that the solder mask is kept away from the die, so that the bumps can touch the landing pad. If the solder mask is thicker than the bumps, prefer NSMD. NSMD design must be bigger than the die, with no varnish between the pads.

Pay attention to the difference between Si-caps with NiAu/ENIG finishing, that need solder paste on the PCB substrate (left side of Figure 6 and 7), and Si-caps with SAC305 terminations (or SAC305 bump) that require no solder paste on the PCB substrate, but only flux (right side of Figure 6 and 7). The solder paste and flux deposition methods are described in Section 4.

2.2.1. Solder Mask Defined

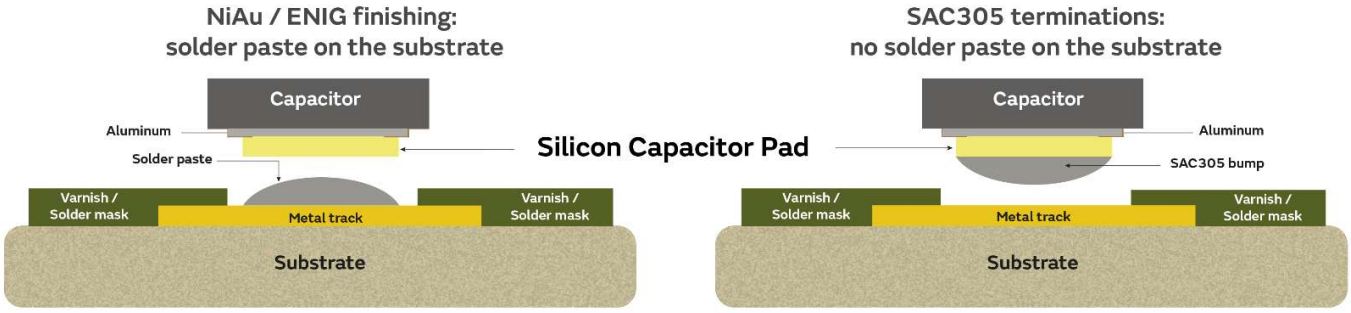


Figure 6: Simplified view of SMD assembly from the side (only one pad is shown here)

2.2.2. Non-Solder Mask Defined

Figure 7: Simplified view of NSMD assembly from the side (only one pad is shown here)

Note: Varnish between the two landing pads can also be applied, if it is thinner than the bumps

2.3. Landing Pads

The tables 1 and 2 show the recommended minimum landing pad dimensions for capacitors with two and four pads (see Figure 8, 9, 10 and 11). These dimensions are defined using the maximum finishing dimensions (such as NiAu/ENIG or SAC305) (see attached Annex). Make sure to take into account the solder mask tolerances.

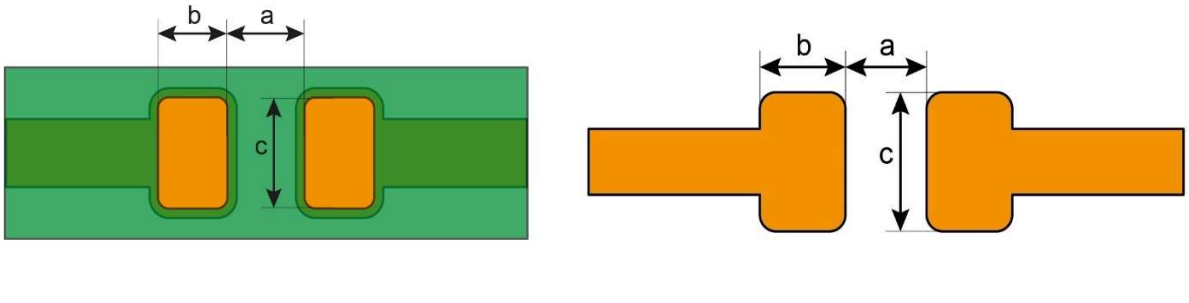


Figure 8: Landing pad dimension indications for capacitors with two pads

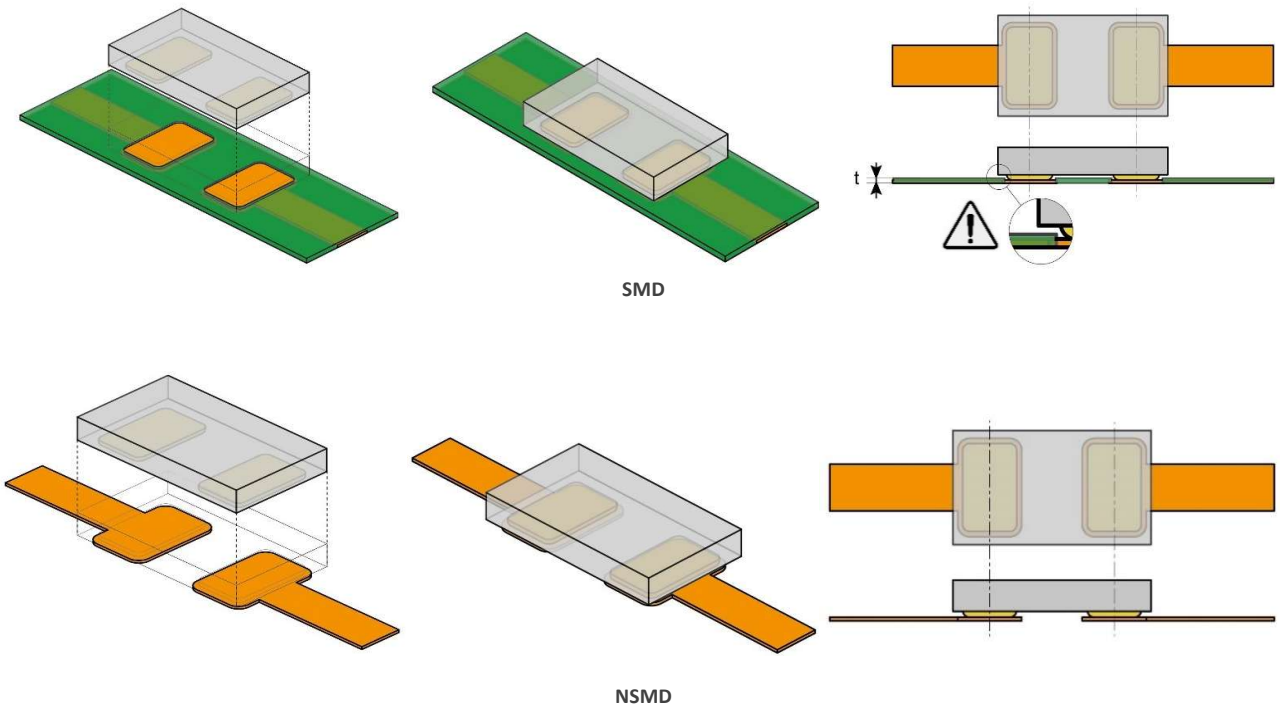


Figure 9: Placement of the two-pad Silicon capacitor on its PCB footprint

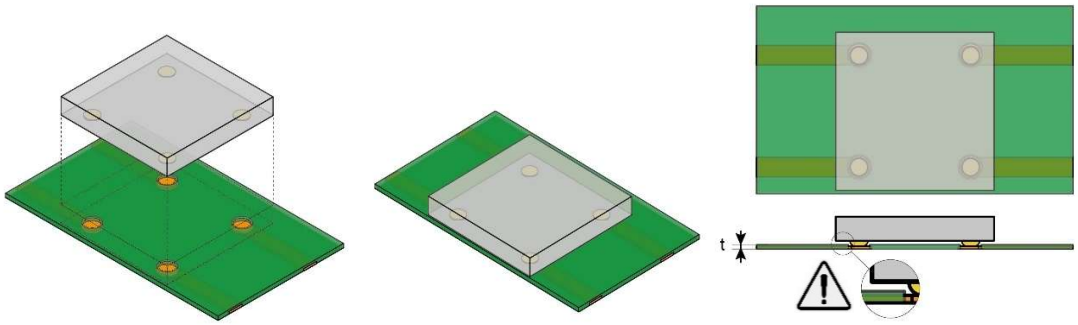
Silicon capacitor type	Capacitor size (µm)	Landing pad dimensions		
		Min. dimensions		Max. dimension
		b (µm)	c (µm)	a (µm)
01005M	400 x 200	135	145	74
0201M	600 x 300	114	164	186
0201	800 x 600	164	414	286
0402	1200 x 700	314	514	386
0204M	500 x 1000	814	114	101
0603	1800 x 1100	414	914	786
0805	2200 x 1400	514	1214	986
1206	3400 x 1800	614	1614	1986
1812	4700 x 3600	914	3414	2686

Table 1: Landing pad dimensions for capacitors with two pads

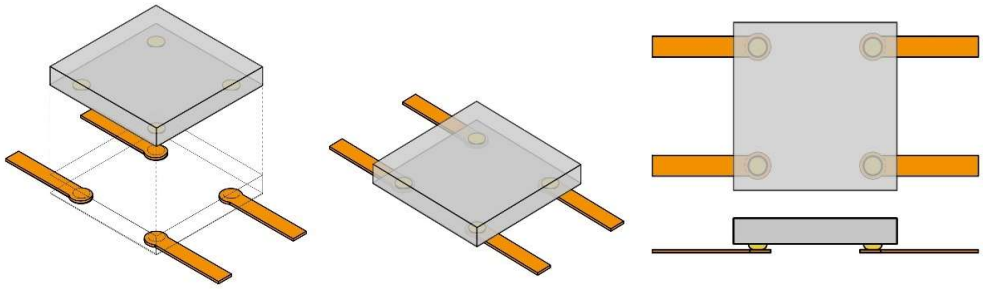
Note: Dimensions “b” and “c” of the landing pads for capacitors with two pads can be considered as minimum values, while the gap “a” between the pads can be taken as maximum values. If you make any modifications to the recommended values, make sure that the pitch of the footprint matches the pitch of the contact pads.

SMD NSMD

Figure 10: Landing pad dimension indications for capacitors with four pads



SMD



NSMD

Figure 11: Placement of the four-pad Silicon capacitor on its PCB footprint

Silicon capacitor type	Capacitor size (µm)	Landing pad dimensions		
		Min. dimension	Max. dimensions	
		Ød$_P$ (µm)	b (µm)	a (µm)
0202M	500 x 500	94	300	300
0402M	1000 x 500	104	250	700

Table 2: Landing pad dimensions for capacitors with four pads

Note: For RF and broadband design, refer to Application Note "Design guidelines for transmission lines of UBB SiCap"

The diameter Ød_P of the landing pads for capacitors with four pads can be considered as minimum values, while the gaps "a" and "b" between the pads can be taken as maximum values. If you make any modifications to the recommended values, make sure that the pitch of the footprint matches the pitch of the contact pads.

For other finishings, refer to the dedicated product specification datasheet or contact Murata Sales Organization.

3. Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking, but manual placement is also possible.

Dies should preferably be handled with a soft tip tool (e.g. rubber). Also, Si-caps are lighter and generally thinner than other stand-alone capacitors, so please consider reducing the pressure applied during placement on the board to avoid mechanical defects. As a rule of thumb, you may consider halving the pressure for your first evaluations and increasing it only if necessary.

For more details on picking and placement forces and tip tool selection, refer to the dedicated Application Note "Recommendation when handling bare dies".

For the dimensions of picking tools, refer to the dedicated Application Note "Nozzle recommendation for Silicon Capacitors assembly" or contact Murata Sales Organization.

4. Mounting Process Flow

4.1. Silicon Capacitors with SAC305 Terminations

The bumps require flux to activate the soldering reflow. The following processes are compatible:

4.1.1. Flux Dipping

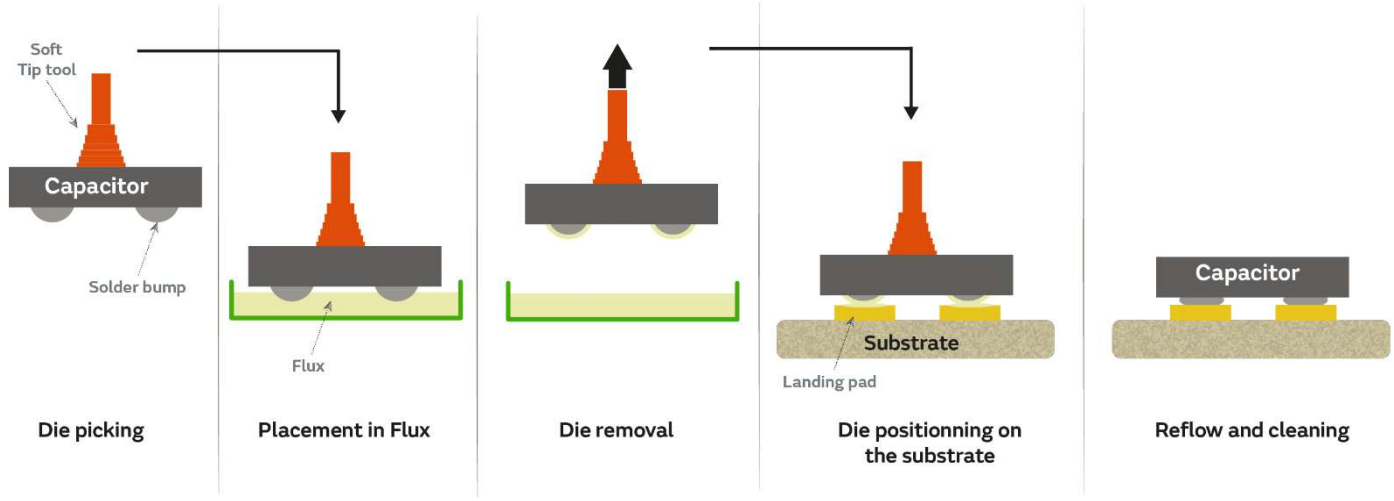


Figure 12: Assembly process by flux dipping on bumped capacitor with SAC305 terminations

4.1.2. Fluxing by Stamping

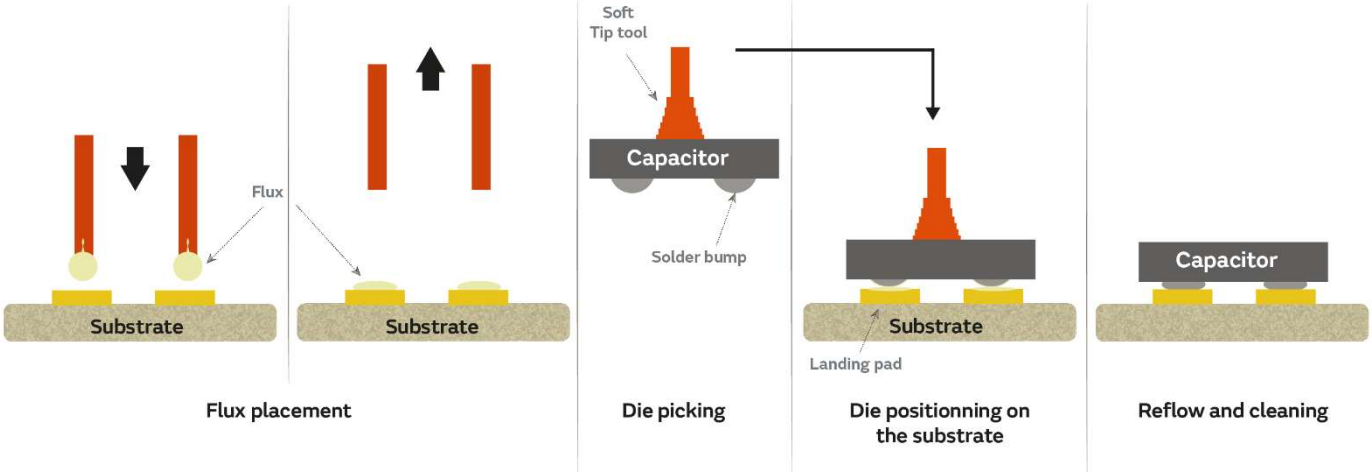


Figure 13: Assembly process by flux stamping on bumped capacitor with SAC305 terminations

4.1.3. Fluxing by Spraying

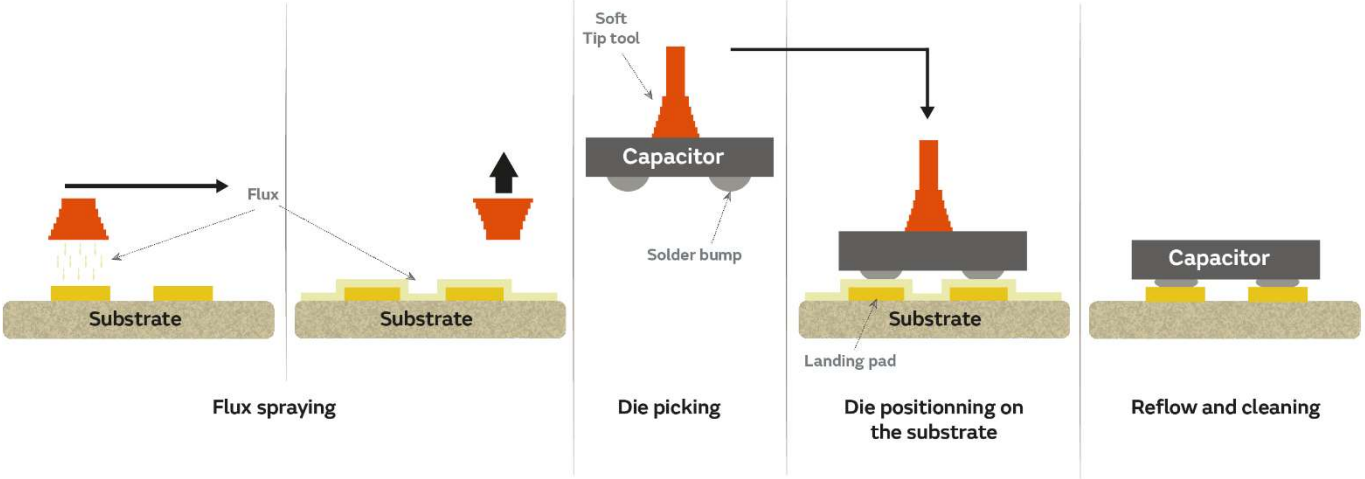


Figure 14: Assembly process by flux spraying on bumped capacitors with SAC305 terminations

4.1.4. Fluxing by Screen Printing

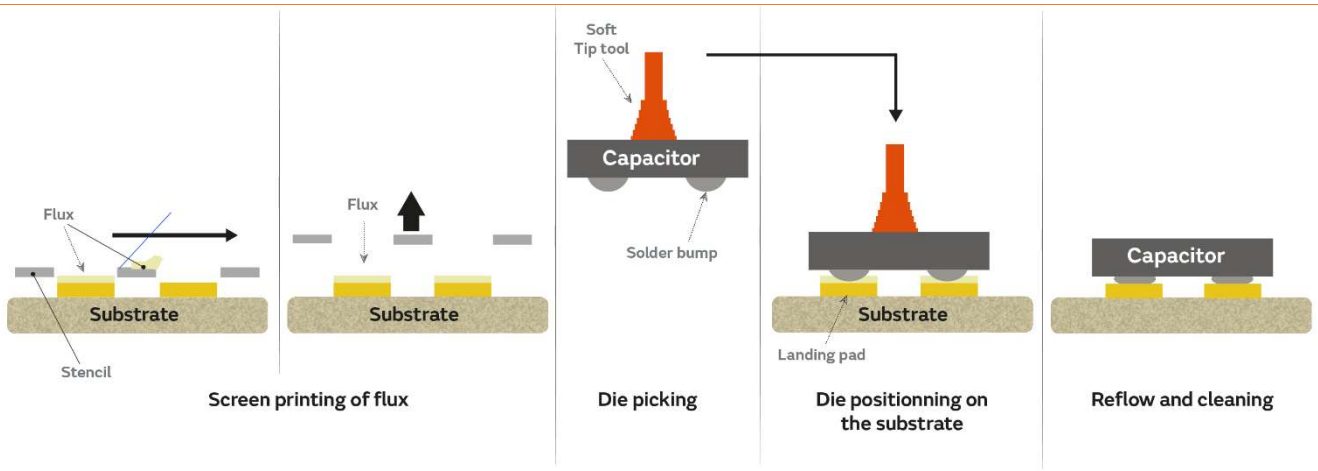


Figure 15: Assembly process by screen printing of flux on bumped capacitors with SAC305 terminations

4.2. Silicon Capacitors with NiAu/ENIG Finishing

We recommend placing the solder paste by screen printing directly on the substrate landing pads:

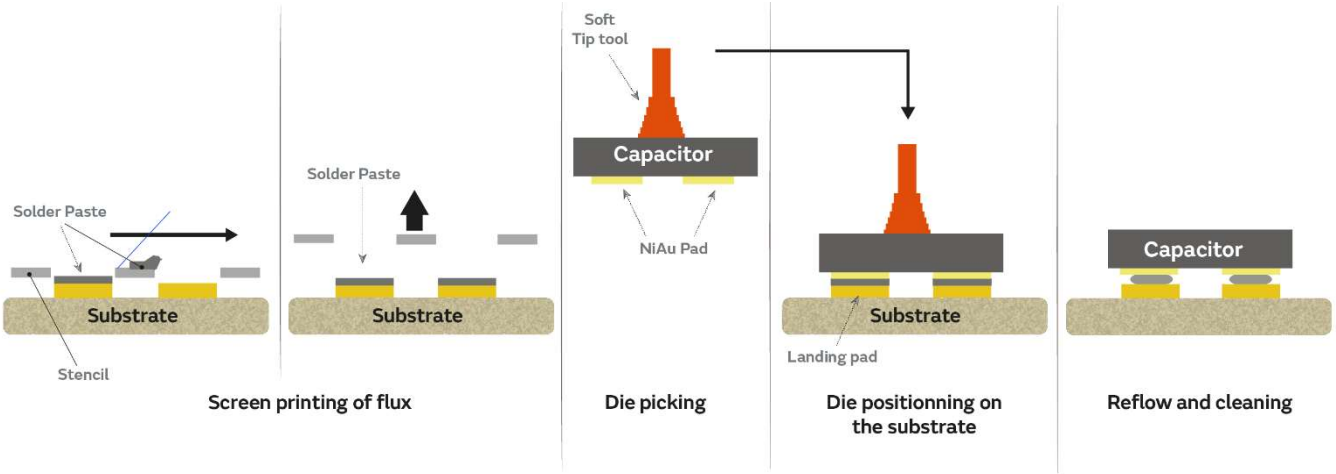


Figure 16: Assembly process by screen printing of solder paste on silicon capacitor

5. Solder Print Material for Silicon Capacitors with NiAu/ENIG Finishing

SAC305 is commonly used and recommended but other materials compatible with the die pad finishing are also possible. Please contact Murata.

Murata recommends using a type 6 powder size. Type 5 can be used depending on the customer PCB design and application. Type 4 is not recommended for 0201M and smaller pad dimensions. The powder size can be adjusted depending on the die pad size. However, type 6 compared with type 4 limits the risk of tilting the capacitor for smaller pad dimensions (refer to part 2).

Alloy	Composition	Solidus	Liquidus	Comments
SAC305	Sn 96.5 %, Ag 3 %, Cu 0.5 %	217 °C	215 °C	Eutectic
Sn63	Sn 63 %, Pb 37 %	183 °C	183 °C	Eutectic Only for allowed applications
AuSn	Au 80 %, Sn 20 %	280 °C	280 °C	Eutectic - High temperature
SnPb	Sn 5 %, Pb 95 %	308 °C	312 °C	High temperature Only allowed for specific applications
SnBi	Sn 42 %, Bi 58 %	138 °C	138 °C	Eutectic - Low temperature

Table 3 : Examples of solder print materials for reflow

For flux cleaning recommendations, refer to section 8 of this document.

6. Stencil Design Recommendations

Murata advises in every case that the width of the stencil opening (referred to as 'W') should be larger than 5 times the average powder size of your soldering material, in order to fill the stencil pocket correctly.
Murata follows the IPC-7525 standard and quantifies the stencil grade based on the ratio between the stencil area ratio (AR), aspect ratio (AS) and thickness. Refer to the following formulas and tables to find the stencil grade we recommend.

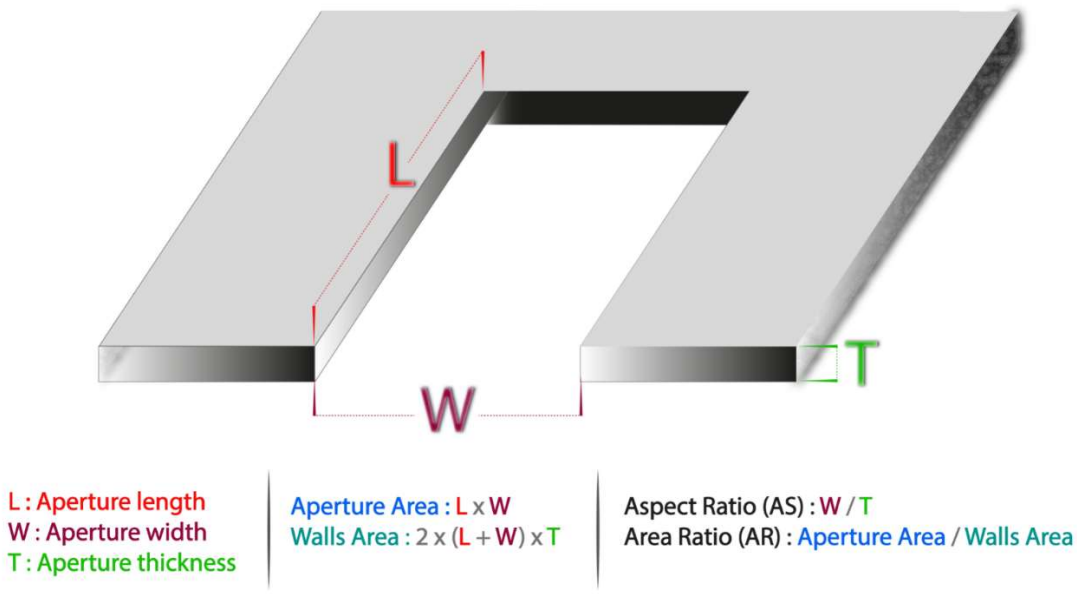


Figure 17: Definitions for stencil aperture

Compare your stencil's desired thickness, aspect ratio and area ratio with the following tables to define which grade we recommend, then consider the highest grade you find from each of the three criteria.

Area ratio (AR)	REGULAR	MEDIUM-HIGH (0.66 – 0.5)	HIGH (0.5 – 0.4)
Aspect ratio (AS)	REGULAR	MEDIUM-HIGH (1.5 – 1.2)	HIGH (1.2 – 1.0)
Thickness	REGULAR	MEDIUM-HIGH (110 µm – 75 µm)	HIGH

Table 4: Stencil grade selection criteria by Area ratio, Aspect ratio and Thickness

Examples of medium-high grade stencils include electroformed or laser-cut technologies.

Examples of high grade stencils include plasma or medium-high grade with surface treatment technologies.

For SAC305, a solder joint thickness of 40 µm +/-10 µm is targeted to limit the risk of contact between the solder paste and the side of the capacitor. Limiting the solder joint thickness will also avoid excessive tilting of the capacitor, especially for small components. Please contact Murata for other soldering materials and thinner solder joints.

For example, a few stencil designs recommended by Murata (SAC305 type 6 with 50 % of flux by volume) are given below:

Silicon capacitor case size	Stencil opening size per pad (in µm)	Stencil thickness (in µm)	Stencil grade (roughness and opening profile)
01005M	105 x 105	40	high
0201M	130 x 200	50	high
0201	150 x 320	100	medium high
0402M	240 x 260	100	medium high
0402	260 x 369	125	regular
0204M	90 x 750	75	medium high
0603	300 x 768	125	regular
0404M	250 x 750	125	regular
0805	400 x 960	125	regular
1206	500 x 1229	125	regular
1812	650 x 3012	125	regular

Table 5: Recommended stencil designs by type for capacitors with two pads

Note: Opening sizes must be adjusted according to flux content and type used.

Silicon capacitor case size	Stencil opening size per pad (in µm)	Stencil thickness (in µm)	Stencil grade (roughness and opening profile)
0402M	120 x 120	40	high
0202M	100 x 100	40	high

Table 6: Recommended stencil designs by type for capacitors with four pads

Note: Opening sizes must be adjusted according to flux content and type used.

For components with a different number of pads, similar rules can be considered as a basis. Please contact Murata for additional support.

7. Soldering by Reflow

7.1. Reflow Recommendations at Regular Temperatures

Murata recommends convection reflow but vapor phase reflow and infrared reflow could be also used.

The reflow process must be carried out in accordance with the JEDEC J-STD-020-E standard for low temperature reflow such as SAC305. For higher temperature solder pastes, such as AuSn, refer to the dedicated Application Note “Assembly Note Silicon Capacitor Reflow at high temperature”.

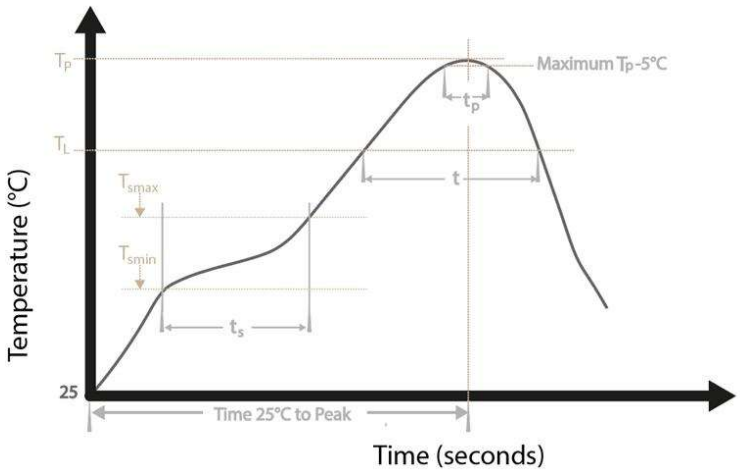


Figure 18: General reflow profile for regular temperature solder pastes (based on J-STD-020-E)

Profile feature	SAC305 (lead-free assembly)	Sn63 (for allowed applications only)
Preheat/soak		
Temperature min. (Ts min)	150 °C	100 °C
Temperature max. (Ts max)	200 °C	150 °C
Time (ts) from (Ts min. to Ts max.)	60 s to 120 s	60 s to 120 s
Ramp-up		
Ramp-up rate (TL to Tp)	3 °C/s maximum	3 °C/s maximum
Liquidus temperature (TL)	217 °C	183 °C
Time (t) maintained above TL	60 s to 150 s	60 s to 150 s
Time (tp) within 5 °C of the maximum temperature	30 s maximum	20 s maximum
Peak package body temperature (Tp)	260 °C maximum	235 °C maximum
Time 25°C to peak temperature	8 min maximum	6 min maximum
Ramp-down		
Ramp-down rate (Tp to TL)	6 °C/s maximum	6 °C/s maximum

Table 7 : Recommended values for regular temperature reflow

According to JEDEC J-STD-020E, the user's peak temperature must not exceed Tp and the time tp must be respected. Values included in the above table may vary with the soldering material.

For flux cleaning recommendations, refer to section 8 of this document.

7.2. Procedure for Solder Joint Measurement (after Reflow)

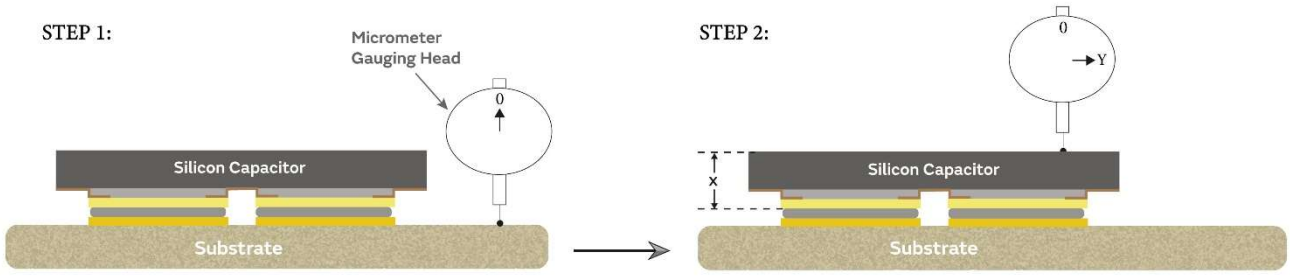


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Figure 19: Solder joint measurement protocol

In step 1, the zero-level reference is made at the PCB surface.
In step 2, the gauge shows 'Y' as the thickness of the whole assembly.
X represents the thickness of the silicon capacitor, including the silicon capacitor pad.
X and the PCB landing pad thickness must be subtracted from Y to obtain the measured solder joint.

$$Measured\ solder\ joint\ thickness = Y - X - landing\ pad\ thickness$$

8. Cleaning after Reflow

For appropriate removal of residual flux, proper cleaning equipment, conditions and solvent are required, to prevent any residual flux or other foreign substances impairing the electrical characteristics and the reliability of the capacitors.

Water-soluble and no-clean flux can be used. In case of water-soluble flux, refer to the solder paste supplier for cleaning and flux removal. For optimum results, it is recommended to remove the flux immediately after reflow to avoid a potential issue of current leakage or short circuits.

However, Murata does not recommend using excessive conditions for ultrasonic oscillation, water or air pressure during cleaning which can cause reliability issues. Before starting your production process, it is important to test your cleaning system and conditions.

Annex

Bump Dimensions

The tables 7 and 8 show the recommended maximum bump dimensions for capacitors with two and four pads (see Figure 20 and 21). The dimensions are obtained using NiAu/ENIG finishings.

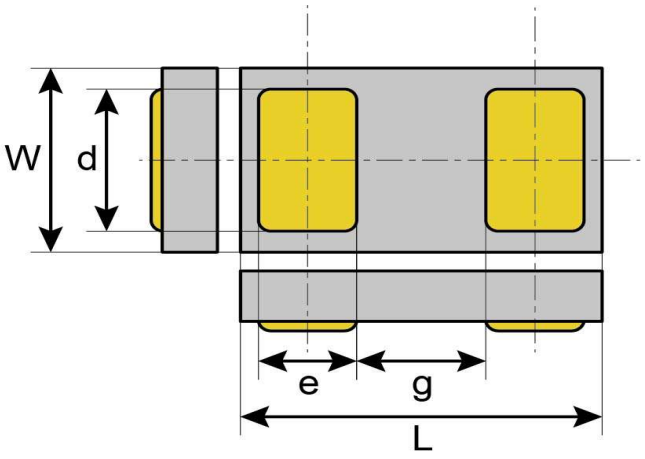
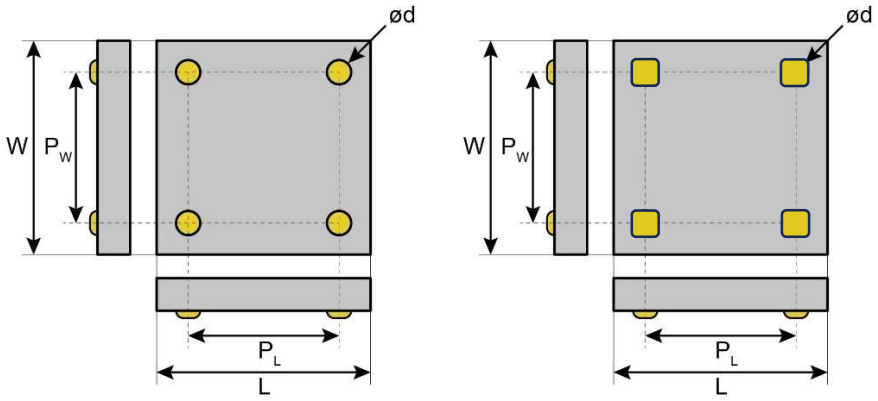


Figure 20: NiAu/ENIG pad dimension indications for capacitors with two pads

Silicon capacitor type	Capacitor size (µm)	NiAu/ENIG pad dimensions		
		Max. dimensions		Min. dimension
		e (µm)	d (µm)	g (µm)
01005M	400 x 200	85	94	124
0201M	600 x 300	112	162	188
0201	800 x 600	162	412	288
0402	1 200 x 700	312	512	388
0204M	500 x 1000	812	112	103
0603	1 800 x 1 100	412	912	788
0805	2 200 x 1 400	512	1212	988
1206	3 400 x 1 800	612	1612	1 988
1812	4 700 x 3 600	912	3412	2 688

Table 8: NiAu/ENIG pad dimensions for capacitors with two pads



0402M **0202M**

Figure 21: NiAu/ENIG pad dimension indications for capacitors with four pads

Silicon capacitor type	Capacitor size (µm)	Bump dimensions		
		Min. dimensions		Max. dimensions
		P_L (µm)	P_W (µm)	Ød (µm)
0202M	500 x 500	300	300	94 (rounded square)
0402M	1000 x 500	700	250	102 (circle)

Table 9: NiAu/ENIG pad dimensions for capacitors with four pads

Disclaimer / Life support applications

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