Low profile 3D-IPD for Advanced Wafer Level Packaging.

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Abstract

Thanks to their 3D structure, the Silicon Capacitors offer drastic improvements in terms of performances compared to the commonly used ceramic and tantalum capacitors. They are also a smart way to reduce the application volume and increase the IP protection level.

With the increasing complexity in the die and package designs and ever increasing cost pressure in today's microelectronic industry, IPDIA is offering for a large range of products, customized or standard components, a low cost packaging solution: the Wafer Level Chip Scale Packaging. While wire-bond interface may remain the preference for many applications, face-down direct chip attachment has gained wide acceptance. More than interacting on electrical functionality, WLCSP is interacting on mechanical and thermo mechanical properties with a higher miniaturization and a transfer directly on printed circuit boards without additional packaging steps.

This paper presents the main characteristics of the 3D-IPD advanced technology emphasizing on its capability and advantages versus discrete components illustrated by different applications using ultra-thin IPD (down to 60µm) and WLCSP .

Introduction

IPDIA , with its PICS process is a major contributor in the promotion of the 3D technology. With its 3rd generation of 3D High Density Capacitors, 250nF/mm^2, running in production with a large variety of products, this company is now moving on the 4th generation, 500nF / mm2. Thanks to the outstanding electrical performances of these Integrated Passive Devices , in terms of stability (temperature, voltage, ageing) and reliability, it is an excellent alternative to discrete component (MLCC and tantalum capacitors) as it exhibits better performances in a much smaller volume.

IPDIA is indeed providing a high-capacitance platform which , combined with the low thickness of the components , 400µm down to 60µm , delivers a high volumetric efficiency.

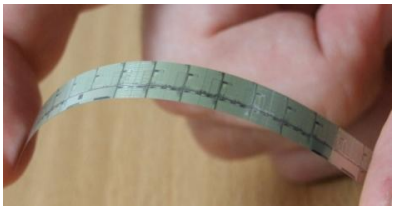

Figure 1: Sample of IPD using the 250nf/mm2 technology thinned at 60µm.

The second Integration level : the packaging benefit

In addition to the integration scale provided by the PICS technology, electronics application may also benefit from the PICS packaging form factor. The usage of the PICS component into a package is one additional miniaturization way that Printed Circuit Board (PCB) is not able to achieve so far. All of the design rules and further roadmap applicable to the PCB technology has its own limitation in terms of metal stack width and spacing, SMD package dimension, necessary footprint surface for a proper soldering process as well as existing placement accuracy provided by most of the SMT industrial equipment roadmap oriented to unit per hour improvement (Cost of Ownership).

There is a second form factor advantage to package the PICS in order to benefit from the packaging design rules in terms of ultra low pad opening dimension, ultra fine pitches, stacking capability in relationship with ultra thin die and

micro-interconnection technology usage. PICS and its packaging combination proposed by IPDiA in a System-in-Package approach provide more than the 3D space reduction, even if it's quite critical for implantable medical modules, LEDs engines, RF system or other specific applications: combination of PICS and packaging provides other advantages such as consumption reduction and energy saving suitable for all portable application, with reduction of leakage currents by interconnection resistance reduction factors. Shortest interconnection between all applicative actives and passive components inside one package is also a positive way for reducing RF noises, particularly used by these applicative domains. In addition to the telecom application, such interest is requested by autonomous and/or portable application with RF communication such as telemetry, home appliance or portable/implantable medical applications as pacemaker, defibrillator or hearing aids. In addition to, active/passive components proximity inside one package provides a better ESD protection closed to power supply input/output pads (i/o), or better signal decoupling. IPDiA is combining most of the more advanced package technologies capability dedicated to PICS component in order to promote and propose the better solution for an easy application adoption approach. At the end, PICS is an adopted way to protect application IP linked to the passive component and its circuitry embedded into one more complex silicon die.

As a MOS-based technology, PICS wafer is then compatible with pad dimension from lower 75µm diameter suitable for advanced packaging technology, up to standard diameters suitable for WLCSP technology usage. The specificity of PICS in WLCSP technology remains the optimized cost for pad limited devices with larger 300µm to 500µm solder bump diameters. It is an optimized gap between advanced C-MOS devices where passive integration has a huge cost impact, and PCB larger scale integrated factors for passive components.

At the packaging level, we may consider two mains technology initiators and differentiators: the first one is definitively the way to process the wafers in order to prepare the die at the right dimension factors in terms of thickness and micro-interconnection approach. A full range of advanced wafer level technologies is supporting that domain. The second one is dedicated to the package architecture orientations suitable for the applicative module in order to promote the product adoption by the customer's applicative platform. Even if PICS component could be used as a companion chip, supporting the main functionality of the platform application, PICS may be combined to one or more functional die and components in a system-in package approach, with extension to SMD, batteries or other miniaturized objects that could be packaged into an heterogeneous module.

Regarding to scale factor, product integration strategy or applicative manufacturing platform capability, PICS may be proposed in a package-less technology such as a simple die suitable for CoB, CoC, COF or CoG wire-bonding platforms (Chip-on-Board, on Ceramic, on-Foil, on-Glass, …) or in a WLCSP form suitable for flip-chip technologies dedicated to the same platforms (FCoB, FCoC, FCoF or FCoG, …). This package-less technology could be extended to a package-less module where PICS acts as an interposer in addition to its IPD functionality, supporting other die through a complete interconnected system over PICS surface. In the same way, this module could be proposed to be wire-bonded or flipped-chip over the same applicative platforms mentioned here above. Finally, packaged approach in various technologies such as HVQFN, LGA, or all suitable packages where SiP technology could be also complementary proposed after a complete validation with the customer in terms of application advantages, costs of the solution, package manufacturing capabilities, the final Board Level Reliability (BLR) and the component adoption by the own customer's manufacturing capabilities.

Package architecture capabilities with PICS devices

a- PICS technology usage in a Wafer Level Chip Scale Package platform (WLCSP)

The package-less approach of WLCSP architecture may allow the best miniaturization factor of PICS usage with optimum pad size and pitch suitable for the specific customer application design rules. It will benefit at the board level in term of interconnection sized optimization compare to a CoB approach. Most of the case, the WLCSP may be handled as a simple SMD when some few precautions are controlled, such as speed approach of the SMT picking head, die picking and die placement force limitations via a pressure gauge system or an over-travel parameters control at the SMT equipment level, the correct speed and acceleration set-up and adapted rubber tip for the pick-up tool. In that form, WLCSP could be manipulated either in standard tape and reel feeding form, or a sawn wafer on tape when a die-ejection system is proposed as an SMT equipment option. Finally, a co-design approach needs to be adopted to insure additional design rules application at the PCB level, such as metallization, organic protection opening rules, µ-vias design and localization, pad dimension, shape and localization with respect to the PICS WLCSP footprint for auto-centering effect during the reflow processing, optimization of the stencil apertures for a correct printing material thickness adapted to optimized bump gap and reliability, flatness of the printed surface free of µ-via technology. The organic solder protection technology may conduct to a proper solder bump and solder printing material composition for BLR optimization concerns. Compared to CoB, this manufacturing strategy provides an optimized process flow, avoiding plasma activation and wire-bonding operation as well as a final dam and fill or glob-top protection technology. Underfilling the PICS WLCP is not necessary useful for reliability enhancement, depending on the physical properties of the substrate and the dimensional design. Most of the PCB

manufacturers avoid the flux cleaning of the PCB after solder reflow, by usage of "no-clean flux" solder print material. If it could be acceptable for large SMD components and packages connections, it is more and more pointed out as a mechanism for solder join degradation in more advanced and miniaturized packages such as fine pitch BGA, CSP and WLCSP packages. IPDiA demonstrates the relationship between flux cleaning and solder join reliability enhancement during thermal cycling reliability tests.

By extension to the wire-bonding technology (CoB, CoC, CoF, CoG), some recommendations also require to pay attention, such as a proper flat die-pad area, avoiding µ-via onto the die-pad area, a proper glue material adapted to substrate metallization and proper behavior under Pressure Cocked Temperature or Humidity Temperature Storage with and without Bias, and finally an optimized material regarding to its physical properties in term of CTE and shrinkage values to optimize the die planarity after the glue curing for a better control of the next wire-bonding operation. For the pick and place consideration, the same recommendations are useful in term of die ejection, picking and placing forces as well as for tooling.

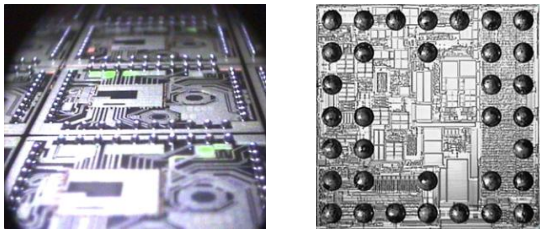

Figure 2: Examples of PICS in WLCSP package architecture

The Integrated Passive wafers are processed with an Under Bump Metallization (UBM) based on Electroless Nickel Immersion Gold technology (ENIG) suitable for solder bump technology. The advantage of PICS technology is driven by a passivation layer suitable for such low-cost and well adapted UBM ENIG technology. For product and SMT process optimization, a 5µm nickel thickness layer is targeted for a proper bump material wettability onto the die pad surface and a complete diffusion barrier well adapted to various bump metal compound such as traditional SAC305 or equivalent dedicated to HASL protection technology PCB family, SAC 127 or equivalent dedicated to OSP protection technology PCB family (As an example, SAC305 is an abbreviation of Tin-Silver-Copper solder compound with 3% silver and 0.5% copper). More specific high temperature solder such as eutectic Au80Sn20 bump composition, Copper-Tin (Copper pillar) technology or other composition like pure Gold dedicated to specific flip-chip process (Thermo-compression, NFC or ACF) could be used in combination with ENIG UBM.

As an extension for WLCSP application, a redistribution Layer (RDL) could be developed over the PICS surface in order to reduce the silicon surface developed for peripheral bump pads and to better distribute the bump locations. This operation consist on a redistribution of the standard PICS pad size of 75µm diameter to extended bump pads of 200µm to 300µm diameter over the full PICS surface. An additional copper metal stack and secondary passivation layer is then processed over the wafer structure, completed with a final UBM localized at the final bump pad metal surfaces. Specific calculation between die cost and RDL cost has to be evaluated in order to estimate the better cost-effective design suitable for the right WLCSP design.

The main factors to design a reliable WLCSP component remains the bump height value to absorb the mechanical shear strengths related to the CTE mismatch between silicon and substrate materials, resulting in solder fatigue or solder/metallization interfaces breakage through repetitive thermo-cycling tests from hot to cold temperature ranges. The bumps localization and composition is another important parameter to consider with respect to relative dimensions of the die, bump and substrate as well as the materials properties (Bumps, metal interfaces, substrate, silicon die), as well as the usage of underfilling process or not in order to observe the first failure apparition at higher cycle numbers by delocalization of the solder join fatigue from board/bump interface to bump/die interface. The design of the WLCSP PICS device has also to be defined as a combination of the maximum ratio between the die length and the die width within a nominal range of 1 to 1.3, as well as the ratio between the die length over the die thickness in consideration with the defect surface density of the PICS back-side. Another specific parameters remains at the substrate level in term of metal repartition and symmetry aspects in relationship with the warpage capability during thermal variations. According to the applicative thermo-mechanical budget defined by the thermo-cycling specification, the final Board Level Reliability (BLR) could be predicted by thermo-mechanical simulations with all of the mentioned parameters, the proper dimensional description of the system, the physical characteristics of the considered materials from the PICS and the applicative substrate (thermo- elastic coefficients CTE, Young Modulus E, Poisson coefficients and mechanical strengths).

b- PICS technology usage as an Interposer platform in WLCSP package

The extension of PICS WLCSP to SiP-WLCSP product using PICS as an interposer platform is developed and proposed by IPDiA. In that architecture, the PICS device is acting as a third-function platform capability: firstly to integrate passive component onto the silicon die (PICS function), secondly to support external die (Substrate function) and finally to interconnect external die and PICS together (Interconnection function). This last function is dedicated to 2D interconnection at the PICS surface (metal tracks), as well as to 3D interconnection side to side by conductive TSV technology (Trough Silicon Via). With respect of all of these building blocks, PICS interposer may be used in different packaging architecture.

i- External die : preparation and interconnection to PICS

The interconnection of external die to PICS interposer is built through a Die-to-Wafer processes range (D2W). Most of the applicative Integrated Circuits (ICs) could be accessed and delivered through the wafer market, except for memories, security or specific proprietary chipset. This wafer business is mainly accessible in the wafer diameter range of 4 to 8 inches, with very few 12 inches diameters availability for standard product range.

The first operation is dedicated to wafer preparation (both ICs and PICS) in term of wafer thinning within the range of 120µm and up for 8 inches wafer technologies, and within the range of 80µm and up for 6 inches wafer technologies. IPDiA capability to handle ultra-thin wafers has been solved with a DBG process (Dicing before grinding) technology suitable for ultra thin die capability. At that stage, there is no thin wafer handling constraints. A proper back-side finishing is improving the defect density level and, by extension the mechanical behavior such as warpage and die-breakage test values. This thinning process was developed on standard wafers as well as on bumped wafers, in order to develop the bumping operations onto ICs and PICS original wafer thickness (680µm or upper) with a very limited handling constraint as well.

The bumping operation is developed with the right process in relation with the die pad size and pitch, and the applicative constraint budget: thermal cycling, power consumption and thermal dissipation specifications. Most of the application may benefit from a solder bump technology using the correct metal compound with respect to the thermal specifications. For pad size/pitch values lower than 100µm/150µm, a galvanic growing process is used to generate pure gold for thermo-compression or thermo-sonic flip-chip processes, or Tin-Silver or Copper-Tin bump structures suitable for soldering flip-chip processes. For pads size/pitch higher than 100µm/150µm, low-cost solder printing or balling processes are used to generate the solder bumps. For the flip-chip technology range using solder bumps, IPDiA is clearly communicating that the flux residue are fully removed with a proper cleaning processes and chemistry for reliability purposes. This specific flux-less process very often makes differences during the BLR evaluation.

ii- 2D Interconnection technology at PICS level

The design of the PICS metal tracks and pads at the die surface is accommodating with 2 interconnection levels: one level named “First Interconnect” is a range of low pitch pads suitable for the external IC die flip-chip such as advanced CMOS. The second one named “Second Interconnect” is designed according to the packaging technology or the customer application substrate (Ceramic, board, flex, etc…) with the correct pad size and pitch dimension. In between the 2 interconnect levels is the full passive network developed with the PICS technology in order to embed the full application.

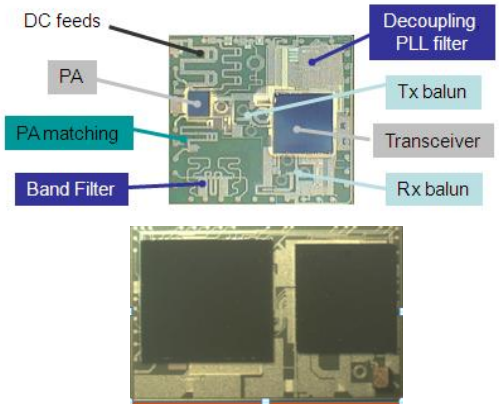

Figure 3: Examples of PICS interposer in RF application (top) and Digital TV with channel decoder, Silicon tuner and LNA transistor functional die (Bottom)

For such architecture, first and second interconnects could be prepared with a similar metal stack with specific metal finishing in relationship with the technologies used for first and second interconnects. Both could be based on Aluminum or UBM end metallization or one could be Al-based suitable for thermo-sonic flip-chip (1st interconnect) or wire-bonding technology (2nd interconnect), while the other could be an UBM finishing suitable for solder bump technology (1st, 2nd interconnects). The external die bump height suitable for the first interconnection is normally designed within a range of [20µm;40µm] or less conventionally higher. Linked to the similarity of physical properties of the external die and PICS component, the D2W will benefit from an underfilling process without specific counter-performances except in RF domain, with the usage of a low-stress, low CTE1 material. Using a jetting technology for the underfilling process of external flipped die set, will also increase the miniaturization effect : the jetting side surface will be less impacted by the material pollution, with a 500µm maximum width while a traditional dispensing may pollute onto 1mm band width. Jetting benefit is also demonstrated by the quantity of underfill material deposited, with a limitation of the bleeding area onto the opposite jetting side, lower than 250µm while a normal dispensing is closed to 500µm bleeding area linked to the time-pressure or Archimedes screw technology accuracy.

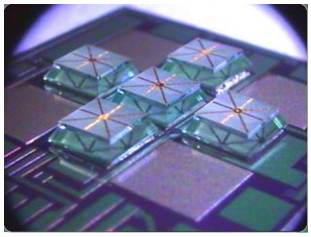

Figure 4 :Example of PICS interposer in LED application : 4 LEDs are flipped over PICS and 5 LEDs are stacked above PICS

External active die could be designed within a thickness range of [120µm;150µm] while the interposer could be designed between 150µm to 400µm. Considering these parameters, a full module would be comprised between 275µm minimum, much lower than any SMD and IC packages technology.

With the same packaging application capabilities discussed previously (PICS WLCSP chapter), the SiP "package-less" module based on PICS interposer could be assemble onto the applicative substrate (Ceramic, Board, Flex, Glass) in a wire-bonding or a WLCSP technologies: the previous recommendations for the PICS WLCSP manufacturability could be applied for the SiP-WLCSP package, with additional comments. SiP-WLCSP usage would be preferred in terms of mechanical picking surface structure: the Interposer back side could easily be picked from a tape& reel cavity and maintain with the standard vacuum pick-up system, while it requires a specific rubber-tip to correctly pick-up and maintain the module from the PICS front-side (external die flipped on it) in CoB application. Regarding to the reliability, the experience in SiP-WLCSP product development demonstrated that the external die interconnection processes are not directly impacted during the Board Level Reliability tests when the SiP-WLCSP is not underfilled. This is the result of a combined benefit of an adapted underfill material usage and a homogeneous silicon assembly structure at the first interconnection level (external die flipped to PICS interposer). The second interconnect level is the only one affected during the BLR test, linked to the same considerations mechanism as described in the PICS WLCSP chapter. Same behavior and limitation is observed between a WLCPS and SiP-WLCSP structure, mainly localized at the solder join or at the 2nd interconnect metallization/Bump interface. Enlarging the 2nd interconnect bump diameter and the resulting PICS interposer-PCB gap would be most of the cases the preferred way compared to an underfilling option to monitor the BLR. Again, a thermo-mechanical simulation may predict such reliability behavior.

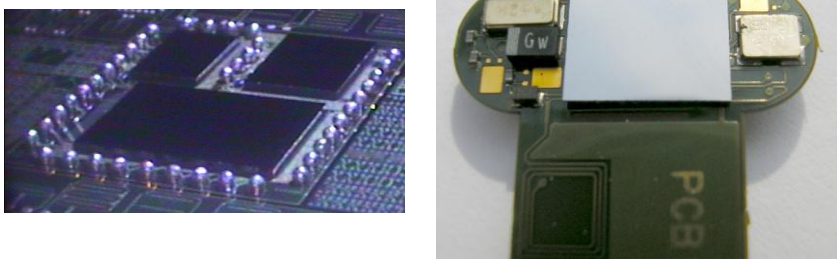

Figure 5: Example of SiP-WLCSP: a controller, RF communication and sensor die set is flipped over a PICS interposer in WLCSP package architecture, and the flex application in medical domain

iii- 3D Interconnection technology : Conductive vias (TSV)

Adding a 3D interconnection with through silicon vias would generate a new functionality to the PICS interposer architecture. Even if that complexity is managed at the PICS process flow, it would be an architecture advantage option at the application level for different usage of the interposer, such as high density laminated substrate application (BGA, LGA) with surface and layers reductions at the laminated substrate. The front side of the PICS interposer is dedicated to the passive integration and external flipped die option, while the back-side would be oriented to interconnection redistribution to the applicative substrate. With such 3D redistribution technology to the back-side, the front-side could be free of 2nd interconnect large pads, and may be designed with the minimum dimension design blocks available with PICS design flow.

Via density is a combination of via ratio (Etching capability measured by the ratio between the via diameter and the via depth, closed to (1/20) on PICS process technology), PICS interposer thickness (Depending on PICS generation, could be between 150µm and 300µm) and routing aspect. Most commonly, via density of 40 to 70 per mm² is reachable. Via structure is an isolated conductive via suitable for face to face interconnection or thermal conduction. Localization and symmetry aspect has to be considered regarding to the interposer mechanical and reliability behaviors. IPDiA developed both metal-based and non-metal conductive material to fill the vias. This application may have some application benefit for the lighting domain, where advanced miniaturized LED engine is build in a wafer-to-wafer (W2W) technology. The LED wafer on sapphire carrier may be processed over the PICS interposer with vias, for both thermal and signal transmission to the final package.

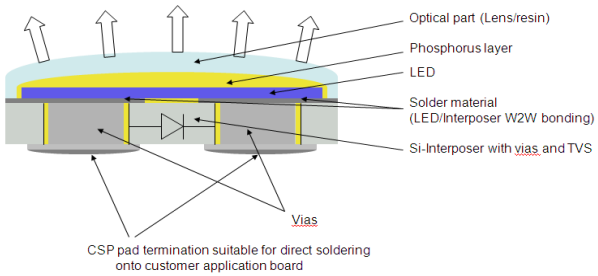

Figure 6 :Example of PICS interposer with via used in W2W technology for LED domain

Conclusion

In combination with the PICS, its packaging technology is enabling the miniaturization and performances in various applicative domains such as Medical, Space, telecommunications and Industrial markets. From the customer applications, product and technology platforms proposed may be used at different integration scale, where the optional enablers are passive, protection and PIN Diodes capability onto silicon, 2D interconnection with external die flipped over and the 3D interconnection face to face with vias technology. Regarding to the cost factor, the global application and miniaturization interests, several PICS architectures and packaging concepts may be proposed and designed from a simple companion chip to a more integrated SIP-WLCSP product. Most of the PCB manufacturers are able to use one or more concepts with a quite simple co-design and manufacturing recommendations through application notes. PICS technology benefit is an easy access to the PCB world in terms of design rules, usage and development costs.

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