Low Profile Integrated Passive Devices with 3D High Density Capacitors Ideal for Embedded and Die Stacking Solutions

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Abstract

Shrinking the size of electronic devices and their interconnections is being pursued vigorously by Semiconductor industry and Research Institutes. Advance in miniaturization technologies already has got impressive impacts on our lives. Radios, computers and telephones, sensors, instruments, electronic brains are in everything from body to washing machines. IPDIA is pushing the limits of miniaturization with its 3D Silicon technology. The mainstream approaches to Integrated Passive Devices miniaturization is limited to High K materials and dies stacking. This paper describes firstly the 3D trench Integrated Passive Devices developed by the company, the products and the roadmaps and secondly the experiments performed to get very low profile IPDs fully functional and highly reliable. The reliability tests methods are explained and the reliability results are shown for IPD, 100µm and 80µm thick, assembled in packaging commonly used in electronics. This work is illustrated by some examples of products using ultra thin IPD down to 50µm.

Introduction

Highly miniaturized components are demanding for new technologies and concepts. IPDIA's concept ,with its process called PICS (for Passive Integrated Connective Substrate),is to integrate passive components such as high-Q inductors , resistors , accurate planar MIM capacitors and trench MOS capacitors in one piece of Silicon . This process is providing a fully CMOS compatible solution for the integration on chip or multiple chip module, [1] ,[2] .

The high density capacitors are fabricated in reactive ion etching etched arrays of macro pores with high aspect ratios up to 60 with a typical width of 1 µm. Capacitors with Oxide /Nitride /Oxide dielectric stacks and polysilicon top electrodes can yield a capacitance density from 6nF/mm² up to 250nF/mm², an electrical breakdown voltage from 150V down to 11V and very low leakage current (<1nA at the working voltage), even when the temperature is exceeding 275°C, [3].

Based on its 3D technology, IPDIA has succeeded in developing the low profile Integrated Passive Devices targeting applications where low thickness is vital such as high density SIM, smart cards and memory modules.

IPD low profile: challenges and roadmap

The main challenge for the low profile technology is to keep the same level of performances as the standard one and the same high level of stability and reliability on ultra thin dies from 100µm down to 30µm. The low profile thickness definition is driven by the 3D trench depth of the High Density Capacitor which varies from 25nF/mm² up to 1µF/mm² (table1) when the deep trenches are respectively targeting 20µm and 50µm depth (figure 1).

Process Node	Capacitor density	Minimum die thickness Low profile thickness
PICS1	25nF/mm²	30µm
PICS2	80nf/mm²	50µm
PICS3	250nf/mm²	80µm
PICS4	500nF/mm²	80µm
PICS5	1µF/mm²	80µm

Table 1: IPD Low profile thickness

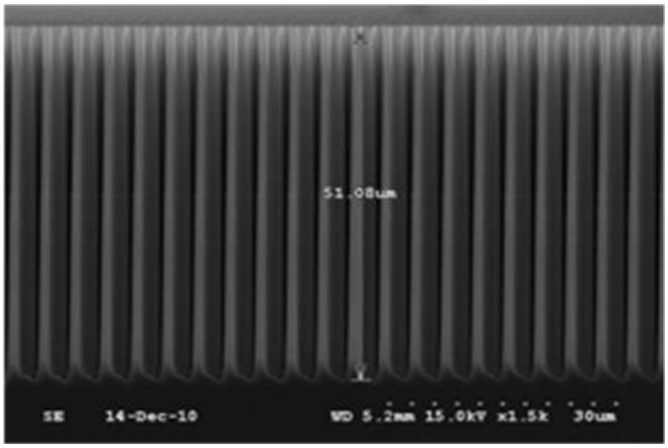


Figure 1 :Cross section of deep trench Capacitors

The figure 2 represents the IPD (Integrated Passive Device) low profile Roadmap. This Roadmap encompasses the release of ultra thin dies as well as the 3D high density capacitors enhancement.

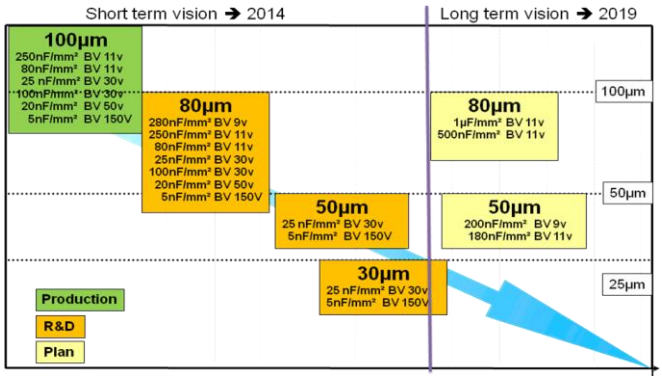


Figure 2 : IPD low profile roadmap

Low Profile 100µm

The LP (low profile) 100µm technology was qualified and introduced in mass production in 2011 [4] . The vehicle selected for the environmental tests was a circuit wire-bonded and assembled in a leadframe-based HVQFN48 package (figure 3).

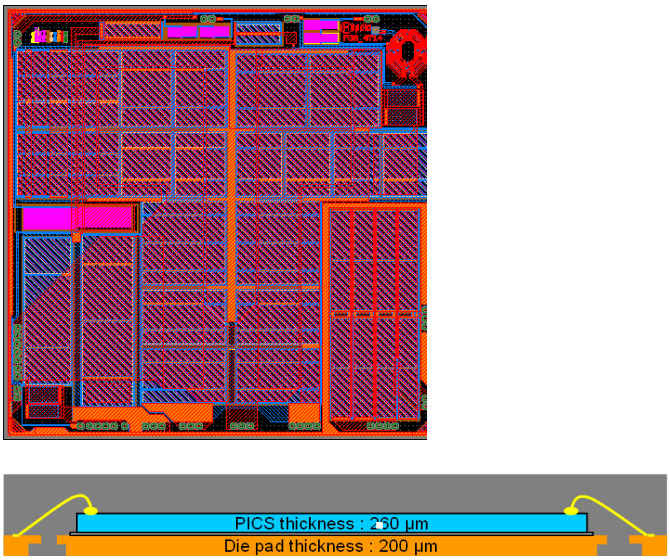


Figure 3: Layout of the vehicle and QFN package
Die size is 5.3 mm * 5.3 mm.

This vehicle was designed, founded, assembled and tested by IPDIA.

Early life test and Long life test:

For EFR (Early Failure Rate) and IFR (Intrinsic Failure Rate), 6*77 parts were exposed to 48h & 1000h DHTL (Dynamic High Temperature Operating Life) +150°C. The modulation was done to evaluate the grinding thickness (100µm / 260µm). No defect occurred on those parts at 1000h (table 1).

Reliability #	Grinding	Quantity	Readpoint	Result	Readpoint	Result
C100791	260	40	48h	0/40	1000h	0/40
C100792	260	37	48h	0/37	1000h	0/37
C100941	100	40	48h	0/40	1000h	0/40
C100942	100	37	48h	0/37	1000h	0/37
C112361	100	40	48h	0/40	1000h	0/40
C112362	100	37	48h	0/37	1000h	0/37

Table 1: EFR and IFR results

844 additional parts were exposed to 48h DHTL +150°C .No defect occurred on those parts.

Highly Accelerated Stress Test:

For HAST, 3*45 parts were exposed to 96 hours 130°C / 85%RH. No defect occurred on those parts.

Reliability #	Grinding	Qty	Readpoint	Result	Readpoint	Result
C112961	100	45	precond	0/45	96h	0/45
C112962	100	45	precond	0/45	96h	0/45
C100891	100	45	precond	0/45	96h	0/45

Table 2: HAST results

Thermal cycling performances:

Temperature Cycling test (TMCL) is conducted for the purpose of determining the resistance of a part to exposure at extreme high and low temperatures. Effects of temperature cycling include cracking and delamination of finishes, cracking and crazing of embedding and encapsulation compounds, opening of thermal seals and case seams, leakage of filling materials, and changes in electrical characteristics due to mechanical displacement or rupture of conductors or of insulating materials. The Technology qualification vehicle was the one described previously, a 5.3mm * 5.3mm silicon die in PICS3 technology, grinded at 100µm thickness, assembled in a HVQFN48 package, as illustrated in Figure 3. This package was selected for its high sensitivity to thermo mechanical constraints, see the figure 5 which illustrates the thermo-mechanical stress landscape for IC – Package interaction, based on extensive package stress modeling [5]. The TMCL endurance is driven by 3 key contributors: the design, the package and the process.

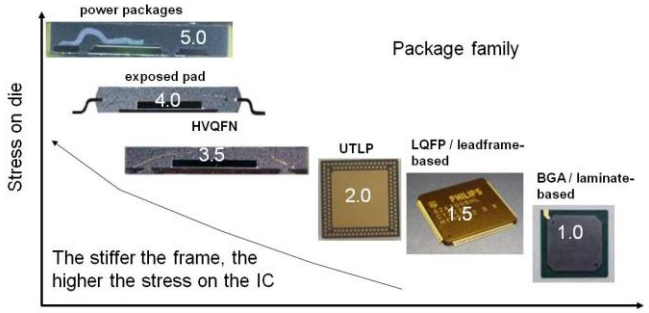


Figure 5: Stress on die versus package (courtesy of NXP)

Test methodology:

TMCL tests were done at package level on a minimum of 231 DUT (Device Under Test) from 3 lots with no more than 90 DUT from any one lot. Parts are preconditioned per JESD22-A113 and tested prior to temperature cycling. The technology qualification vehicle was exposed to 1000 cycles -65°C / +150°C (JEDEC), with intermediate test point at 200 cycles.

The effect of Thermal Cycling is illustrated on Figure 6

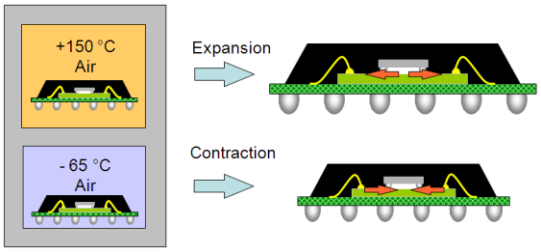


Figure 6: Effect of thermal cycling

4*77 parts were exposed to -65°C/+150°C cycles in order to evaluate two process parameters:

- Grinding thickness (100µm / 260µm)
- Secondary passivation with an organic material 10µm thick

JEDEC recommends a temperature cycling test of 500 cycles. In order to investigate process robustness, the parts were exposed to 500 additional cycles (table 3).

Reliability #	IVD	Grinding	Readpoint	fails	Readpoint	fails	Readpoint	fails	Readpoint	fails
C100801	yes	100	precond	1/77	200c	0/76	500c	5/76	1000c	24/71
C100802	no	100	precond	0/77	200c	0/77	500c	0/77	1000c	6/77
C100803	no	260	precond	0/77	200c	0/77	500c	0/77	1000c	0/77
C100804	yes	260	precond	0/77	200c	0/77	500c	0/77	1000c	1/77

Table 3: Thermocycling results

A number of defects was observed on the modulation "100µm-grinding with secondary passivation (IVD)":
One part was damaged during preconditioning and 5 parts were defect at 500 cycles: 2 capacitors were shorted, typical signature of thermo-mechanical constraints (figure7)

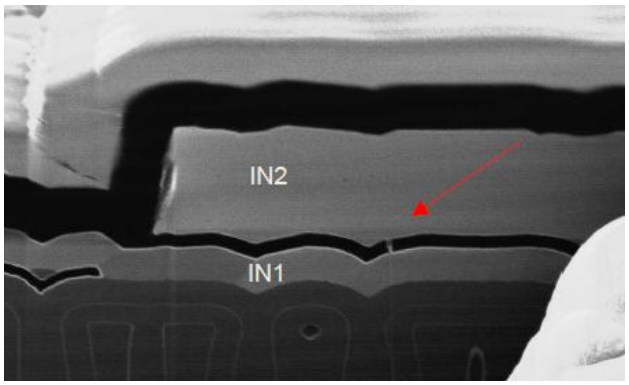


Figure 7: Short between Metal 2 (IN2) and Metal 1(IN1)

The modulation "100µm-grinding with secondary passivation" is confirmed as the worst combination regarding TMCL performances (24 additional parts fail).
Without secondary passivation, the modulation "100µm-grinding" passes JEDEC specification of 500cycles but six parts fail at 1000 cycles. The modulation "260µm-grinding" has significant reliability margin since no failure is observed up to 1000cycles. This indicates a strong influence of substrate thickness: the thinner, the weaker.

The modulation "260µm-grinding with secondary passivation" passes 500 cycles but one part fails at 1000 cycles. This indicates that secondary passivation generates mechanical constraints after thermo cycling.

2*77 additional parts were exposed to -65°C/+150°C cycles:

- Grinding thickness 100µm
- No secondary passivation

Reliability #	IVD	Grinding	Quantity	Readpoint	Fails	Readpoint	Fails	Readpoint	Fails
C112401	no	100	77	precond	0/77	200c	0/77	500c	0/77
C112402	no	100	77	precond	0/77	200c	1/77	500c	2/76

Table 4: Thermocycling results

One part was defect at 200 cycles, 2 parts at 500cycles .The rejected parts show IN1 to IN2 metallic shorts (figure7).

The conclusion is that this package is not compatible with the 100µm thickness.

Additional tests were performed at less critical temperature conditions (-55°C + 125°C) and on samples with stress relief before the grinding. The typical use conditions for a number of common applications (High End Server, Avionic Cockpit, Telecom Hand Held Application…) have been compared to 3 possible test conditions: condition C (-65°C / +150°C), condition B (-55°C / +125°C) and condition G (-40°C / +125°C).In the case of Telecom Hand Held Application, 5.0 years field lifetime is equivalent to 202 cycles condition C(-65°C/+150°C), 344 cycles condition (-55°C/+125°C) or 446 cycles condition (-40°C/+125°C).

2*77 additional parts grinded at 260µm were exposed to 500 cycles -65°C/+150°C, and 2*77 parts grinded at 100µm were exposed to 1000 cycles -55°C/+125°C (Table 5):

Reliability #	Grinding	Test	Readpoint	fails	Readpoint	fails	Readpoint	fails
C113351	260	TMCL 150	precond	0/77	200c	0/77	500c	3/77
C113352	260	TMCL 150	precond	0/77	200c	0/77	500c	3/77
C113341	100	TMCL 125	precond	0/77	200c	0/77		
C113342	100	TMCL 125	precond	0/77	200c	0/77		

Table 5: additional thermocycling results

Concerning the 260µm samples, no failure was observed at 200 cycles -65°C/+150°C, 6 failures were observed at 500 cycles .These 260µm samples are more robust than the 100µm samples that failed at 200 cycles in the same conditions(table 3 &4).
Concerning the 100µm samples, no failure was observed at 200 cycles -55°C/+125°C. No failure was observed at 500 cycles -55°C/+125°C. Three failures were observed at 1000 cycles -55°C/+125°C.

Due to different temperature coefficients of materials used in the package and the chip, large forces will be exerted on material interfaces during temperature cycling (TMCL), possibly leading to metal shift, passivation or IDL (intermetallic dielectric layer) cracking. Package stress rules are described in the PICS process manual to prevent such phenomenon.

Process improvement:
In order to improve TMCL performances on the low profile technology, 9 additional lots of parts grinded at 100µm were exposed to 500 cycles -65°C/+150°C. Three thicknesses of the IDL were investigated:

- Standard 5kÅ
- 9kÅ
- 15kÅ

No defect was observed at 200 cycles for the three modulations. 17 samples out of 231 failed at 500 cycles for the 5kÅ standard. All 227 parts passed 500 cycles for the 9kÅ modulation. All 231 parts passed 500 cycles for the 15kÅ modulation (table 6).

Reliability #	IDL	Qty	Readpoint	result	Readpoint	result	Readpoint	result
C113974	5k	80	precond	0/77	200c	0/76	500c	3/77
C113975	5k	80	precond	0/77	200c	0/77	500c	5/77
C113978	5k	80	precond	0/77	200c	0/77	500c	9/77
C113976	9k	75	precond	0/77	200c	0/77	500c	0/73
C113977	9k	80	precond	0/73	200c	0/73	500c	0/77
C113971	9k	80	precond	0/77	200c	0/77	500c	0/77
C113972	15k	80	precond	0/77	200c	0/77	500c	0/77
C113973	15k	80	precond	0/77	200c	0/77	500c	0/77
C113979	15k	80	precond	0/77	200c	0/77	500c	0/77

Table 6: Thermocycling results versus IDL thickness

This no-failure situation demonstrates that TMCL performances have been significantly improved by the increase of the Intermetallic Dielectric Layer.

Acceleration factor (AF) due to temperature cycling test is described by the Coffin-Manson Equation:

$$AF = (\Delta T_{stress} / \Delta T_{use})^n$$

ΔT_{stress} = temperature swing during stress test

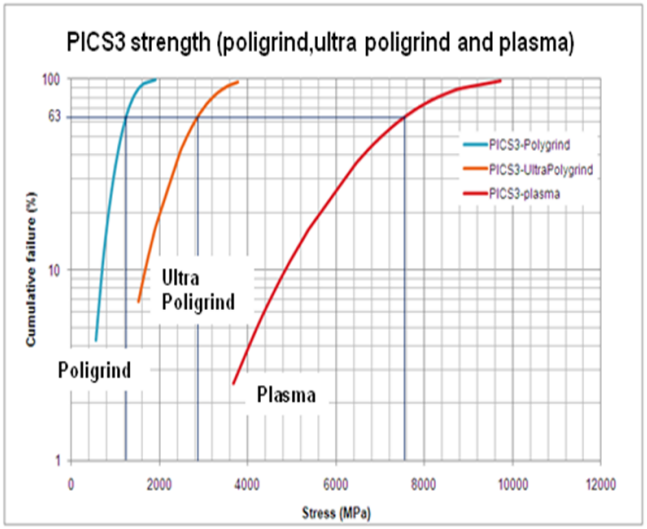
ΔT_{use} =temperature swing during use

n=Coffin Manson exponent; 3.0 for 3D IPDIA technologies

In the case of Telecom Hand Held Application, cumulative failure for the Low Profile 100µm IPDIA technology is now less than 1% after 23 years in use.

Low Profile 80µm

To carry on the execution of the low profile roadmap, the thinning conditions have been studied through a DOE that applied to the coarse and fine grinding steps (mesh size and final thickness) as well as the finishing step (no step vs. Ultra Poligrind vs. plasma).Setting up proper grinding and stress relief steps is key to eliminate substrate damages and preserve electrical and mechanical performance of ultrathin PICS dies. A "ball on ring" test [6] was used to compare the mechanical strength of the samples after thinning by measuring the failure stress of 80µm-thick specimens (figure 8)



Test	Slope	Stress (Mpa)	Mean deflection(µm)	Regression(%)
	β	63%	α(µm)	R^2(%)
Poligrind	3,94	1233	160	97
Ultra Poligrind	4,18	2865	230	92
Plasma	5,07	7569	440	96

Figure 8: PICS strength versus 3 grinding conditions.

The plasma relieved samples exhibited the highest characteristic strength (Weibull @63,2%). The thinning parameters that offered the highest strength were then implemented to supply 80µm-thick PICS wafers in order to perform accelerated aging tests.

Some wafers were sawed in samples of 10mm x 38mm (made of 7 dies) dedicated to a 4 point bend (4PB) test (see Figure 9).

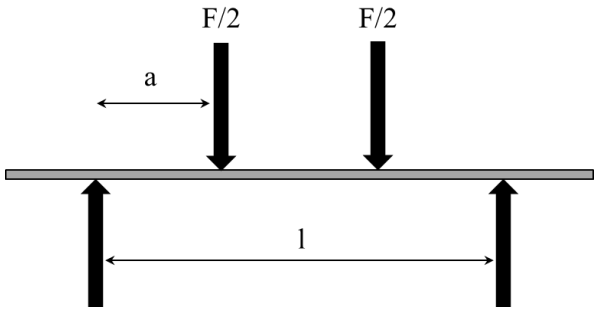


Figure 9 : 4 point bend (4PB) setup

In that aim, a home-made tool designed, manufactured and operated at CEA-Leti was used to bend 4 samples simultaneously (see Figure 10) by moving a mobile part (outer span l=30mm) within a "y" range towards a fixed part (inner span l-2a=10mm).

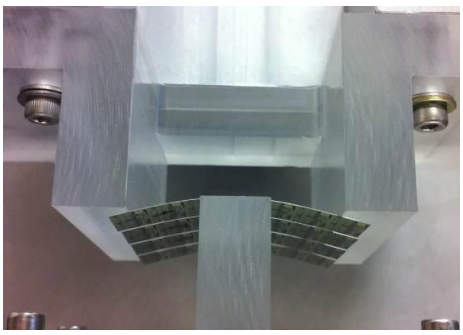


Figure 10: 4PB tool with 4 bent PICS samples

In order to fit with normalized bending conditions for smart cards applications, a radius of curvature "R" of 40mm was imposed in the middle of the samples. Equation (1) gives a value of 2mm for "y". The corresponding stress applied to the 80µm-thick samples was 160 MPa.

$$y = \frac{a\,(3l - 4a)}{6R} \qquad \textbf{(1)}$$

Smart card normalized test required 10 bendings (both sides) on 10 samples. In this work, 50 000 bendings were performed (both sides) on 12 samples. Electrical characteristics of 3D capacitors after bending were compared with initial values. Electrical tests have been done using CEA-Leti's automatic prober after positioning the samples on dedicated silicon carriers with etched cavities (see Figure 11).

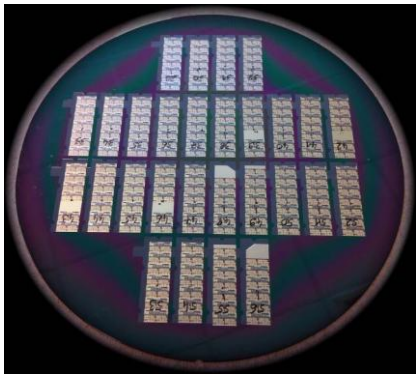


Figure 11: Silicon carrier with 28 samples to be probed

Two 3D capacitors (C_1 and C_2) were measured (C value, tanδ and I(V)) on the center die of each sample. Measurement results before/after bending are given in Table .

		Mean		Stdev	
		Before	After	Before	After
C_1	C (nF)	12.62	12.48	0.23	0.23
	tand δ	0.068	0.127	0.001	0.056
	I(V=9V) (nA)	24	23	2	2
C_2	C (nF)	17.53	17.48	0.11	0.11
	tand δ	0.074	0.174	0.002	0.068
	I(V=9V) (nA)	416	388	64	64

Table 7 : Electrical tests before/after 50 000 bendings on 12 samples at 160 MPa

Among the 12 samples the maximum variation before/after bending is 1.2% for the capacitance and 11.5% for the leakage current. Variations of tanδ are higher (up to 292%) because of test issues, since the samples' warp make the contact resistance with the probes unstable. More restricting conditions by increasing the bending amplitude to the limit of silicon breakage (observed for y=3.8mm) were also tested. 4 samples have been measured before and after 10 000 bendings with a "y" value of 3.5mm, which corresponds to R=24mm and σ=290 MPa (see Table 8).

		Mean		Stdev	
		Before	After	Before	After
C_1	C (nF)	12.92	12.80	0.12	0.12
	tand δ	0.066	0.090	0.007	0.032
	I(V=9V) (nA)	26	26	2	2
C_2	C (nF)	17.14	17.04	0.74	0.74
	tand δ	0.066	0.189	0.013	0.128
	I(V=9V) (nA)	508	488	146	147

Table 8: Electrical tests before/after 10 000 bendings on 4 samples at 290 MPa

No significant change in the C value (<1%) and in the leakage current (<10%) of the 2 capacitors was measured, which shows that the PICS technology is compatible with thin dies subject to very aggressive mechanical stress conditions.

This qualifies the PICS technology for smart cards applications since the 3D capacitors are not damaged during the bending test.

Thermocycling performances:

TMCL tests were carried out on 77 dies coming from the same set of thinned wafers .The package and the conditions were the same as for the 100µm low profile technology.

One defective package (figure 12) was detected after 200 cycles. No more failures until 1000 cycles

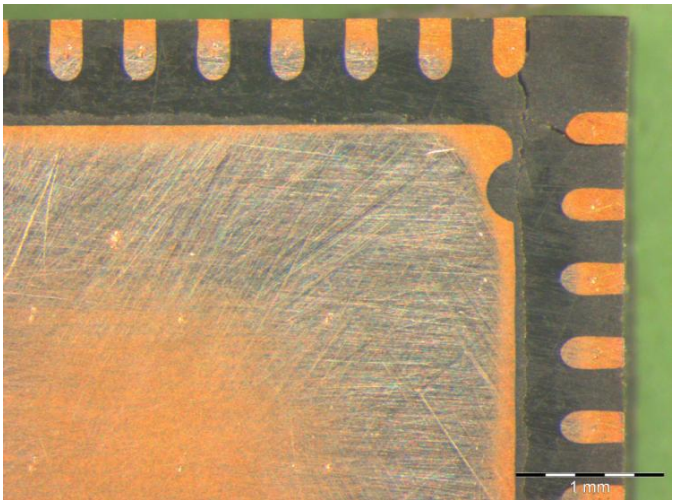


Figure 12: crack observed on the package (top corner)

Additional TMCL tests will be performed on PCB (FR4) boards with 3 different types of assembly: HVQFN, Flip Chip and COB (chip on board) to end up with the process qualification.

Application:

The LP passive devices are suitable for all the advanced low profile consumer applications such as RF devices, cameras, LCD modules as well as memory products like smartcards, RFID, memory cards and modules. They are designed to be surface mounted on board with or without a package, flip chipped or wire bonded. They can also be embedded in a PCB (figure 13), placed directly beneath active components or stacked (figure 14), allowing higher packaging densities and higher performances to be achieved.

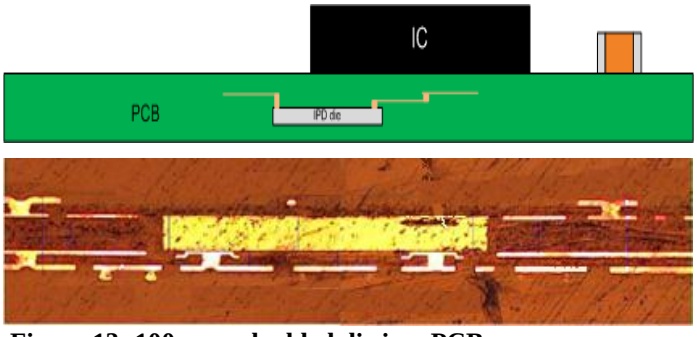


Figure 13: 100µm embedded die in a PCB

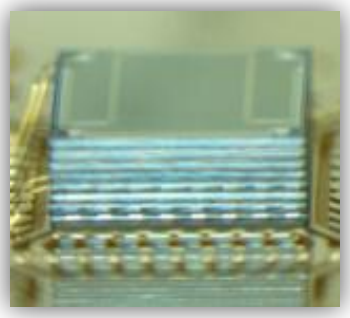


Figure 14 : 10 Capacitors stacked in a package height of 1.5mm

Conclusions

The low profile IPDIA technology capability is limited by the density of the trench capacitor, more explicitly by the depth of the trench. The 100µm Low Profile node is qualified. The preliminary reliability results obtained on the 80µm LP are also very promising. In addition to being one of the lowest-profile IPD manufacturers on the market, IPDIA is providing the lowest profile 3D Silicon capacitors with a superior stability and reliability over a wide temperature range.

The work done for the nodes 100µm and 80µm qualification is predicting a safe qualification of the 50µm & 30µm nodes.

Acknowledgement

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