Power amplifier performances and miniaturization improvement based on Wire Bondable vertical Silicon Capacitors

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Abstract — This paper presents Wire Bondable vertical Silicon Capacitors (WBSC) performances in high-frequency high-power applications up to 10 GHz and results on capacitance value versus die size. These capacitors combine ultra-deep trench MOS capacitors of few nF and single layer MOS capacitors of few pF in a 0101 single package. The performances of these capacitors have been compared with conventional commercialized vertical capacitors. The benefits of using these capacitors have been quantified thanks to their integration in a power amplifier.

Index Terms — high density silicon capacitors, decoupling for power amplifiers, microwave integrated circuits, high power capacitors.

I. Introduction

The single 1nF WBSC capacitor in 0101 package size is suitable for DC decoupling and filtering functions in all RF and microwave power applications for wireless communication, radar and data broadcasting systems. The Integrated Passive Devices technology developed by IPDiA also provide industry-leading performance particularly in terms of capacitor stability over the full operating DC voltage & temperature range. In addition, intrinsic properties of the silicon lead to a low dielectric absorption and a close to zero piezo electric effect resulting in no memory effect. This Silicon based technology is RoHS and REAch compliant.

II. WBSC Capacitors Building

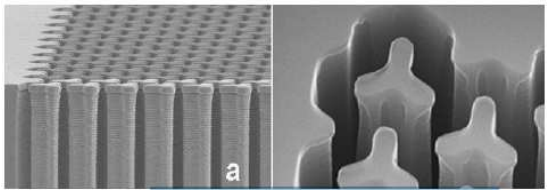
The SiCap technology of IPDiA with advanced 3D topology is comparable to a total area of 80 ceramic layers. The use of a very efficient silicon based dielectric avoids the compromise between capacitance value and electrical performance.

These high density 3D capacitors make up the beating heart of the IPDIA PICS™ technologies: the combination of patented [1] high aspect-ratio micrometric 3D structures (50:1 pores or trenches, drilled in the silicon by Deep Silicon Reactive Ion Etching, see Figure I) with standard dielectrics (silicon oxide and/or nitride) from the semiconductor industry in single (or multiple) Metal Insulator Metal (MIM) architectures (Figure II) enables the process of capacitors with densities as high as 250nF/mm².

3D trench capacitors (figure I) provide outstanding density integration performances as well as remarkable electrical characteristics (low ESR and low ESL) when compared with external components described in [2], [3], [4], [5]. This is mainly because of the individual components proximity and layout flexibility inside the circuit.

Figure I

Cross-sectional SEM images of 3D MOS embedded trench capacitor manufactured by IPDiA



These Si capacitors in ultra–deep trenches enable the integration of high capacitance density from 1.3nF/mm² to 250nF/mm², as shown in figure II (with a break-down voltage of respectively 450V to 11V). A dielectric stack of silicon nitride and silicon dioxide associated to an N-type very low-ohmic silicon substrate is used to produce these small devices. Figure II presents the capacitance densities currently available at IPDiA. The increase in minimum break-down voltage from one generation to the next one is the combination of advances in dielectric material deposition, etching techniques, and device geometry in order to keep the highest capacitance density versus voltage.

Figure II

WBSC capacitance density versus min break-down voltage

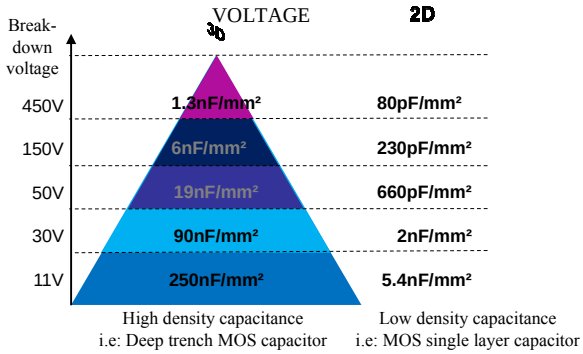
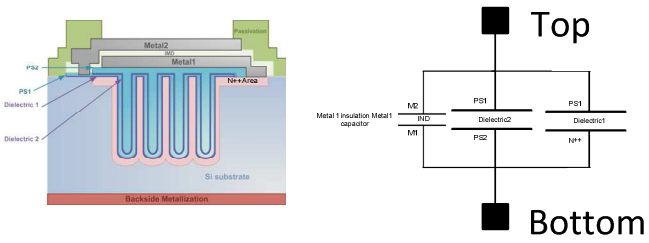


FIGURE III

On the left: CROSS SECTIONAL VIEW OF THE MIMIM ARCHITECTURE USED IN THE IPDIA PICS™ TECHNOLOGY. On the right: SCHEMATIC (VOLUNTARY SIMPLIFIED) OF THE CAPACITORS PARALLELIZED IN A MIM ARCHITECTURE TO OFFER A HIGHER CAPACITANCE VALUE THAN IN SINGLE MIM IPDIA PICS™ TECHNOLOGIES

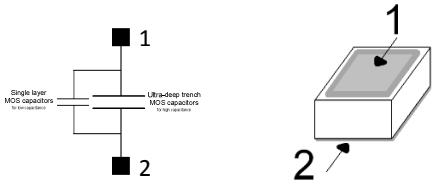


As in figure III, $C_{TOTAL} = C_{MIM} + C_{Trench}$ with $C_{MIM}=C_{M1\text{-}N++}$ & $C_{Trench}=C_{PS1\text{-}N++}$

In this paper, the 19nF/mm² capacitance density node is considered. For this technological node, the bottom electrode is the very-low-ohmic Si substrate while the top electrode (PS1) is connected to the first aluminum metal layer. The number of contacts to the capacitor electrodes is maximized to reduce resistive losses. This WBSC Capacitor combines ultra-deep trench MOS capacitors for high capacitance value of 1nF and single layer MOS capacitors for low capacitance value of 10pF, together in a single 0101 package size.

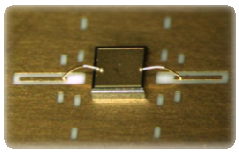
FIGURE IV

1nF//10pF-0101 WBSC CAPACITOR BLOCK DIAGRAM AND 3D VIEW OF WBSC CAPACITOR PIN CONFIGURATION



III. WBSC CAPACITORS STABILITY OVERVIEW AND RF CHARACTERIZATION

FIGURE V: WBSC capacitor test board



The WBSC capacitors exhibit high Q-factor (low ESR < 33mΩ), very high self-resonance frequency (SRF) (low ESL < 12pH), very low capacitance change over temperature and voltage variation (respectively Graph I: ±0.5% from -55°C to +150°C and Graph II: 0.02%/V) as well as a very high reliability and low leakage current. The dielectric stack deposited using a high temperature process (900°C) is leading to an excellent uniformity and stability of the capacitance value, and also to a memory effect close to zero. Moreover, the silicon substrate brings low dielectric absorption (see table I) and almost no piezoelectric effect.

Thanks to our Silicon substrate, our WBSC capacitors have at least 6 times lower dielectric absorption than ceramic capacitors.

TABLE I

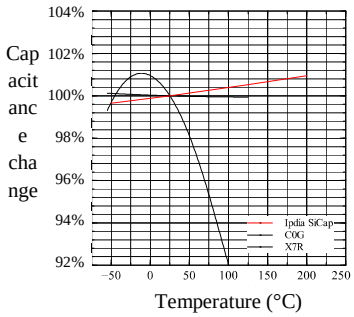
DIELECTRIC ABSORPTION COMPARISON

Type of capacitor	Dielectric absorption
Class-1 ceramic capacitors, NP0	0.6%
Class-2 ceramic capacitors, X7R	2.5%
Silicon capacitors	0.1%

Temperature and voltage measurements show that WBSC capacitors behave as robust devices in various configurations. For instance, the ΔC/C variation is lower than 80 ppm/°C in the –50 °C/+150 °C temperature range. As shown in Graph I for the case of a 1nF//10pF WBSC capacitor, ΔC/C variations are linear over temperature.

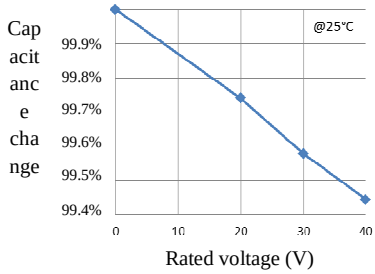
GRAPH I

1NF//10PF - 0101 WBSC CAPACITANCE VALUE VERSUS TEMPERATURE

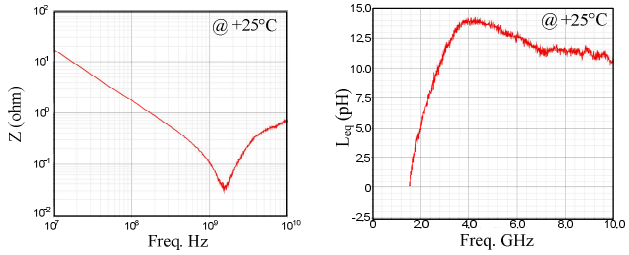


GRAPH II

1NF//10PF - 0101 WBSC CAPACITANCE VALUE VERSUS RATED voltage: 0.02%/V



GRAPH III
1nF//10pF - 0101 WBSC IMPEDANCE AND ESL CHARACTERISTIC VERSUS FREQUENCY IN SHUNT MODE



Graph III shows the extracted equivalent inductance (L_{eq}) values resulting in shunt mode. This measurement mode allows to mathematically remove the extrinsic parasitic elements like wire bonding without de-embedding them; only a de-embedding of access line is needed.

TABLE II
1nF//10pF - 0101 WBSC CAPACITOR PERFORMANCES

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value		-	1	-	nF
L	Capacitor length	±0.01mm		0.294		mm
W	Capacitor width	±0.01mm		0.294		mm
h	Capacitor heigth	±0.01mm		0.10		mm
T_{OP}	Operating temperature		-55	20	150	°C
DC_T	Capacitance temperature variation	-55°C to 150°C	-0.5	-	+0.5	%
BV	Breakdown Voltage		50	-	-	V
DC_{RVDC}	Capacitance voltage variation	From 0V to RV_{DC}	-	-	0.02	$\%/V_{DC}$
IR	Insulation resistor	@ 25°C & RV_{DC}	10	-	-	GΩ
ESL	Equivalent Serial Inductance	@ SRF	-	-	12	pH
ESR	Equivalent Serial Resistance		-	-	33	mΩ

The self-resonance frequency (SRF) can then be simplified as follow:

$SRF = \frac{1}{2\pi\sqrt{ESL}}$ where C is the capacitance value of capacitor and ESL is the Equivalent Serial Inductance.

The extracted ESL including the top electrode interconnect is approximately 12pH for a 1nF//10pF WBSC capacitor, resulting in a frequency resonance higher than 1.5GHz, thanks to appropriate interconnect strategy. When the ESL is lower, the SRF is higher. Therefore, a capacitor can be used to provide capacitive impedance for a higher frequency range.

IV. WBSC CAPACITORS COMPARISON

GRAPH IV
1NF//10PF 0101 WBSC VERSUS CERAMIC 1NF CAPACITOR
On the left: S21 AT 25°C
On the right: L_{EQ} AT 25°C

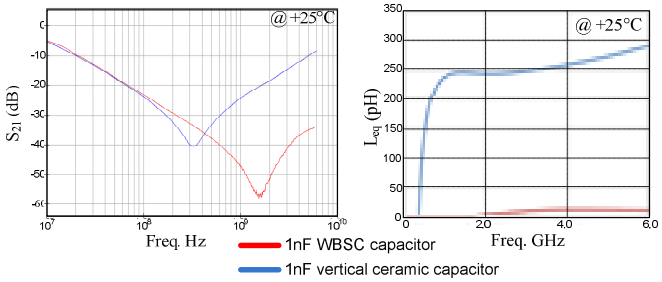


TABLE III
CAPACITORS COMPARISON

Symbol	Parameter	Conditions	WBSC	Cer. Cap. 1	Cer. Cap. 2	Unit
C	Capacitance value	@ 25°C	1nF//10pF	1	1	nF
SRF	Self Resonance Frequency	@ 25°C	1500	600	200	MHz
WVdc	Working DC voltage	@ 25°C	20	50	50	V
X/Y	Component Size x/y		294x294	890x890	635x635	µm
T	Component Thickness		100	178	178	µm

To confirm the out-coming results, the performance of the WBSC capacitor has been compared with two conventional commercialized 1nF vertical ceramic capacitors. Graph IV shows that the intrinsic parasitic elements in broadband ceramic capacitors are very high compared with the WBSC capacitors. On top of this, a comparison made with other silicon capacitor manufacturers shows that only few 10s or 100s of pF are achieved when the WBSC capacitance is 1 nF in 0101.

V. WBSC CAPACITORS INTEGRATION WITH MOS POWER AMPLIFIER

The high-frequency communication infrastructure market, including base stations for mobile communications and broadband capable wireless systems, continuously expand.

As the designs of circuit modules become smaller and require lower power consumption, lower-profile and high-frequency low-loss (low ESR & ESL), capacitors are therefore absolutely necessary.

Since WBSC capacitors have low intrinsic parasitic elements, high capacitance density and use a silicon base substrate, they are the most adequate capacitors for the ultra large band decoupling function in these applications. In most cases, for the decoupling function, the WBSC capacitor resonates with either coils or resistors and can produce resonance at a specific high frequency.

With a 0101 package size, the wire bonding length can be minimized, and the extrinsic parasitic elements can thus be reduced.

In the following example, we will see how the noise of the power supply can be reduced thanks to the WBSC capacitor and its shorter bond wire.

The test bench consists in a LNA, with its power supply decoupled by a 1nF capacitor (ceramic or WBSC) connected through a bond wire. This bond wire is simulated with 1nH for WBSC (wire length=1mm) and with 2nH for ceramic cap (wire length=2mm). A noise generator (at $10^{-6}V^2/Hz$) is replacing the supply and the noise at the LNA output is measured.

The S-parameter files of each capacitor are used in order to obtain a more realistic simulation.

FIGURE VI
TEST-BENCH SCHEMATICS FOR NOISE SUPPRESSION SIMULATION: WBSC VS CERAMIC CAPACITORS

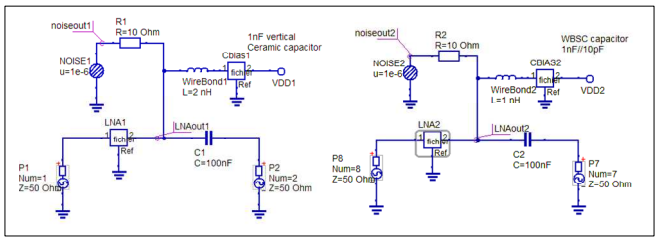
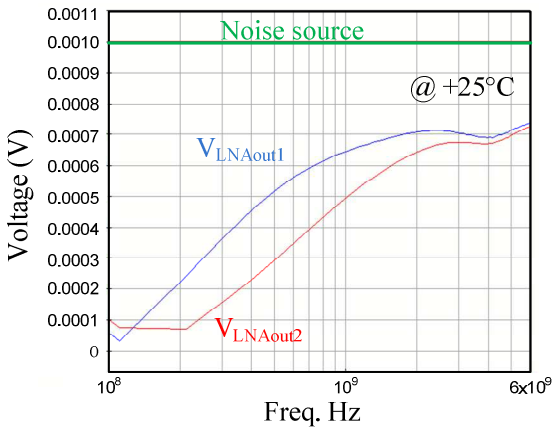


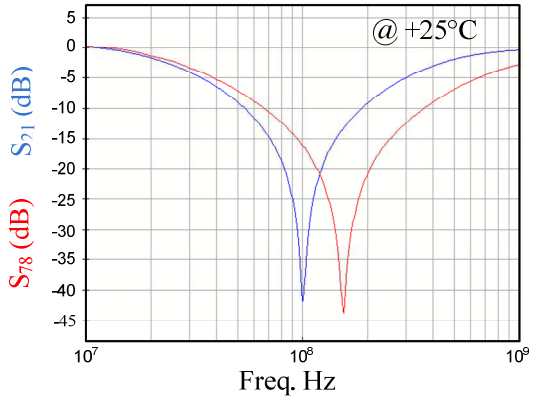
FIGURE VII
NOISE SUPPRESSION SIMULATION: WBSC VS CERAMIC CAPACITORS



The red curve represents the white noise at the LNA output1, with the WBSC capacitor, while the blue one represents the white noise at the LNA output2, with the ceramic capacitor. The noise suppression is more efficient with the WBSC capacitor. The WBSC capacitor allows to improve the noise immunity higher than 7dB in comparison with the ceramic capacitor.

This could also be seen by considering the S21 (or S78) of the system: the rejection at higher frequencies is more important with the WBSC capacitor, as shown on Figure VIII.

FIGURE VIII
REJECTION SIMULATION: WBSC VS CERAMIC CAPACITORS



VI.

VII. CONCLUSION

The WBSC Capacitors from IPDiA show high power, broadband frequency, lifetime, miniaturization and performance stability and are therefore ideal for demanding applications such as wireless communication, radar and data broadcasting systems. The very last large band vertical PICS™ process generations can propose a wide range of breakdown voltages while preserving an interesting capacitance density with unequalled level of microwave performances.

This paper has highlighted the possibility to improve the noise immunity performances (very high DC noise rejection) of an RF power amplifier application by using the decoupling WBSC silicon capacitor. The specific process and component developed for these applications mentioned, have allowed to reduce extrinsic *(like wire bonding length, short ground connection, …)* and intrinsic parasitics *(monolithic capacitor with all unitary 3D capacitors in 50µm depth instead of 500µm in ceramic technology)*; compared to the existing ceramic capacitors. Main benefit of this is an extreme miniaturization in X, Y and Z with a very high density capacitance specifically developed for RF power applications.

Developments are now focused on extending “high voltage versus high capacitance density vertical process” to larger elements and to demonstrate co-integration with resistance to be used in the field of the high efficiency high frequency power amplifier.

REFERENCES

[1] C.Bunel, F.Murray,"Silicon based integrated capacitors: new solutions for combined miniaturization and high performance." CARTS international 2014, Santa Clara

[2] H. Jacquinot and D. Denis, “Wide frequency band scalable modeling of 3D embedded decoupling capacitors,” Proc. Spanish Conf. Electron Devices, 2013, pp. 1–4.

[3] J. H. Klootwijk, K. B. Jinesh, W. Dekkers, J. F. Verhoeven, F. C. van den Heuvel, H.-D. Kim, D. Blin, M. A. Verheijen, R. Weemaes, M. Kaiser, J. J. M. Ruigrok, and F. Roozeboom, “Ultrahigh capacitance density for multiple ALD-grown mim capacitor stacks in 3-D-silicon,” IEEE Electron Device Lett., vol. 29, No. 7, pp. 740–742, Jul. 2008.

[4] 3. M.K. Matters-Kammerer, K.B. Jinesh, T.G.S.M. Rijks, F. Roozeboom and J.H. Klootwijk, “Characterization and Modeling of Atomic Layer Deposited High-Density Trench Capacitors in Silicon,” IEEE Transactions on Semiconductor Manufacturing, vol. 25, 2012, pp. 247- 254.

[5] A. Bajolet, J.-C. Giraudin, C. Rossato, L. Pinzelli, S. Bruyère, S. Crémer, T. Jagueneau, P. Delpech, L. Montès, and G. Ghibaudo, “Three-dimensional 35nF/mm2 MIM capacitors integrated in BiCMOS technology,” in Proc. 35th ESSDERC, Grenoble, France, 2005, pp. 121–124.