# Silicon interposers with Integrated Passive Devices, an excellent alternative to discrete components.

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**Abstract**

*A new way of designing high density silicon capacitors that are intended to be co-integrated with TSV for advanced silicon interposers is presented. This new kind of design; called "mosaic" enables to manufacture IPDs with capacitor density up to 500nF/mm² while maintaining ultra low ESR. PICS™ "mosaic" capacitors implement localized elements set in parallel on a grid that behave as a parallel network and exhibit the following characteristics:*

- *The global "mosaic" capacitor has a linear dependency with $C_{Global}=N*C_{Local}$ where N is the number of repetitions of the localized element and $C_{Local}$ its capacitance*
- *ESR and ESL have an inverse dependency with N : $L_{Global}=L_{Local}/N$ and $ESR_{Global}=ESR_{Local}/N$.*
- *Thanks to the 1/N variation of both ESL and ESR; and the N/1 variation of C respectively, the products ESR*C and ESL*C are nearly constant which respectively means that the cutoff and SRF of the device are also constant, whatever the N value is. The global capacitor performances (like SRF) are driven by the most elementary building block and almost independent from the capacitor size*

*Key words: silicon interposer, integrated passive devices, high density silicon capacitor, ultra low ESR, PICS™ technologies.*

## Introduction

IPDIA is one of the key players in the integrated passive devices manufacturing. Thanks to its proprietary Passive Integration Connective Substrate (PICS™) technology range, passive components such as capacitor, resistors, inductors, diodes (…) can be integrated onto silicon with a minimal footprint and without any tradeoff on the device performances [1]. Among these passive components, high density 3D capacitors make up the beating heart of the PICS™ technologies: the combination of patented [2] high aspect-ratio micrometric 3D structures (50:1 pores or trenches, drilled in the silicon by Deep Silicon Reactive Ion Etching, see Figure 1) with standard low-k (silicon oxide and/or nitride) from the semiconductor industry in single (or multiple) Metal Insulator Metal (MIM) architectures (Figure 2) enables the process of devices up to 250 nF/mm².

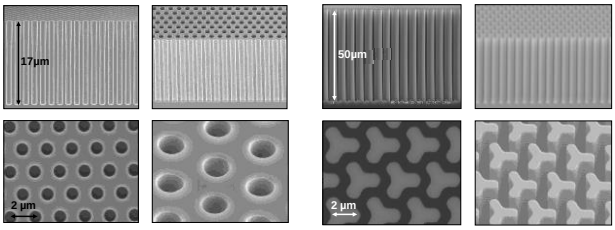


**Figure 1: SEM micrographs example of the high aspect-ratio structures etched in the silicon substrate (pores of AR ~ 17:1 on the left, tripods of AR~50:1 on the right)**

Such a capacitor density is reached with the production proof process called PICS3™ currently used to provide high-end capacitors for many applications, like pacemakers, enabling in this former case, a significant size reduction of the implantable device and thus, a lower invasive surgery.

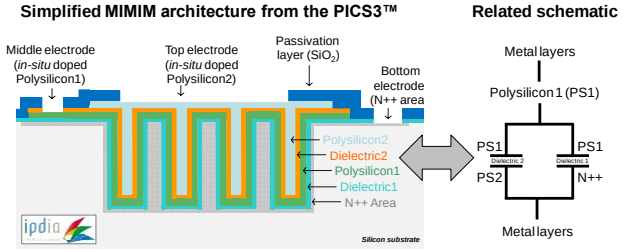


**Figure 2: On the left: cross sectional view of the MIMIM architecture used in the PICS3 technology. On the right: the schematic (voluntary simplified) showing how the capacitors are parallelized in a MIMIM architecture to offer a higher capacitance value than in single MIM**

## IPDIA PICS™ technologies

These 3D silicon capacitors based on the various PICS™ processes from IPDIA exhibit outstanding performances such as:

- Capacitance density up to 250 nF/mm² with breakdown voltage ($V_{BD}$) of 11V minimum
- « Intrinsic lifetime » $t_{0.1\%}$ > 10 years @ 3.6V, 100°C (60% C.I.) even for corner batches
- Low leakage for low power consumption (typically < 5 nA/µF and down to < 0.2 nA/µF @ 3.2V/25°C)

- High capacitance stability with respect to temperature (70 ppm/°C over the range -55°C/+200°C) or voltage (<0.1%/V)

IPDIA's roadmap regarding capacitor density can be divided in two approaches: on one side, the "square path" and on the other side, the "cubic path". The first one aims at integrating the highest capacitance with a minimum footprint onto silicon. The second one aims at stacking the highest amount of PICS™ capacitors in parallel so as to provide capacitor stacks in the tens of µF range for applications where high energy in a small volume is a key requirement (see Figure 3).

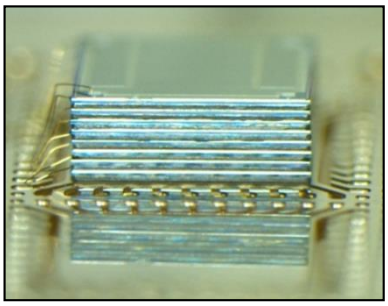

**Figure 3: Example of an IPDIA "cubic path" realization (die stack of 8 PICS3™ capacitors of 2.2µF each and thinned to 80µm, leading to a 17.6µF device)**

One can easily note that the denser at "square path" level, the more efficient the "cubic path" to enable high value capacitor stacks. In that sense, IPDIA is continuously improving capacitor integration onto silicon. R&D efforts on this item can be summarized with the equation below:

$$C = \frac{\varepsilon_0 * \varepsilon_r * S}{t}$$

**Equation 1**

According to Equation 1, one can easily note that whatever the architecture (single or double MIM), capacitance density integration increase can be obtained by playing on three main factors:

- Increase the dielectric constant $\varepsilon_r$ (by changing/optimizing the dielectric material)
- Increase the electrode surface of the capacitor (with deeper/denser 3D structures)
- Reduce the dielectric thickness (which is challenging if $V_{BD}$ and/or lifetime are expected not to be degraded)

The very last generation of the PICS™ technology (called PICS4™) still uses very high aspect ratio 3D structures in a MIMIM architecture but combines them with highly engineered high-k layers [3] (i.e. with a higher $\varepsilon_r$) to reach the 500nF/mm² value [4].

Such improvements were obtained without any tradeoff with respect to lifetime, leakage or breakdown voltage. However, the implementation of these high-k layers has lead to new integration constraints: as high temperature sensitive materials, the high-k layers does not allow high thermal budget for post process steps (initially estimated at 600°C max). As a consequence, the *in-situ* phosphorous doped polysilicon that is typically used as both middle and top electrode materials could not be re-crystallized at high temperature with a conventional furnace annealing. Thus, its intrinsic resistivity is higher than for earlier PICS™ technologies. To overcome this disadvantage inherent to the integration of high-k materials, several scenarios are currently studied, among which:

- Rapid Thermal Annealing (RTA) experiments are being performed to find the thermal budget that results in the best tradeoff between electrode resistivity and dielectric properties of the high-k layers in term of permittivity and lifetime.
- Specific style of design, where PICS structures are implemented in a way intended to mostly parallelize electrodes resistance such as to reduce global capacitor ESR. This PICS™ capacitor design style is called "mosaic" and is compatible with both PICS3™ and PICS4™ processes.

This paper thus focuses on the outstanding electrical performances that can be reached with these "mosaic" PICS™ devices able to provide ultra low ESR capacitors for demanding applications. These passive components are intended to be co-integrated with the IPDIA Through Silicon Vias (TSV) technology so as to propose 3D silicon interposers with IPD thus enabling a significant size reduction for space constrained devices.

**IPD performances: a new PICS™ design concept for low ESR applications**

The standard way to design PICS™ capacitors consist in defining a block of high aspect-ratio 3D micrometric structures (i.e. tripods for the PICS3™ process) that enable to reach the specified value and then in sizing the required areas for contacting the three electrodes from the MIMIM architecture. These contact dimensions are defined according to each electrode material sheet resistor with the objective to maximize capacitance density while maintaining contact areas large enough (see Figure 4) to obtain reasonable ESR (i.e., in the 100mΩ range for a 1µF capacitor).

With this style of design, the current is mostly flowing in the electrodes along large distances to reach individual PICS™ pores. As a consequence the ESR is driven by the capacitor shape/outer extend and the ESR is hardly tunable by design.

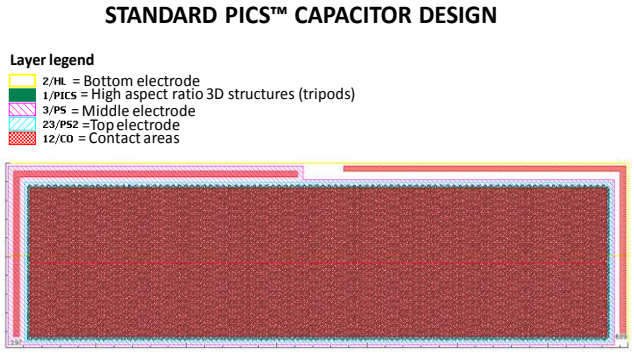


**Figure 4 : Example of a standard 689µm*197µm (27nF) PICS3™ capacitor design (top view) showing the contact areas (red) of future metal layers on bottom electrode (yellow), middle electrode (hatched pink) and top electrode (hatched blue). Note that contact surface on**

**top electrode is huge while contact surface accessing to bottom and middle electrode are relatively small. Note also that middle electrode sheet resistance is 4 times higher than bottom electrode sheet resistance.**

The "mosaic" style of design overcomes this issue with a global capacitor element designed as a grid of localized capacitors elements that are all parallelized. With this approach, the design of the localized element can be tuned to match any requirements in term of ESR or Capacitance (C). Indeed:

- The global capacitor targeted value C, is correlated to the number N of localized elements to be parallelized on the grid such that the capacitance value of the localized element is C/N,
- The global ESR target taken as a function of 1/N that is forcing the ESR of the localized element,
- The ESR of the localized element being correlated to the local density of metallization contact to capacitor electrodes.

This approach has several obvious advantages among which a perfect scalability, and a lower sensitivity to electrode quality (i.e. resistivity) as long as contact are provided locally, resulting in a lower ESR and constant contact density overall the structure.

The Figure 5 represents a "mosaic" PICS™ capacitors made out four repetitions of a localized capacitor cell (containing the high aspect ratio 3D structures and the oversized contacts areas all around). The Figure 6 gives a projection of the ESR to Capacitance dependency, extracted out of real elements (interpolated) and idealized projection (extrapolated) by having a parallelized approach. The perfectly linear slope in a Log.Log representation of the ESR as a function of Capacitance corresponds to the behavior of an idealized grid where perfect discrete RC (localized element) are connected in parallel on the grid.

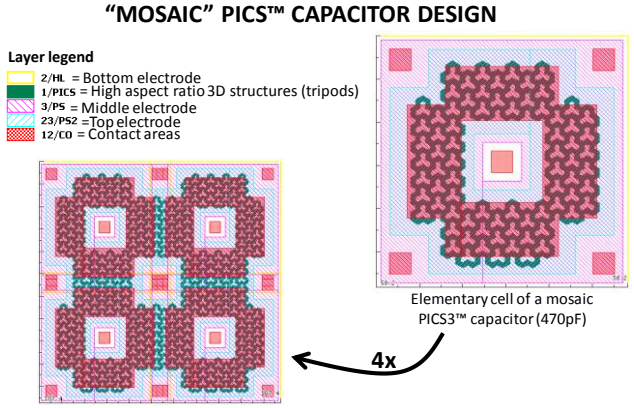


**Figure 5: Focus on the 58.2µm*58.2µm elementary cell of a mosaic-style PICS3™ capacitor (420pF). Elementary cells are parallelized as necessary to reach the required capacitance value**

The scope of the present study was to demonstrate the validity of the above approach. For that, several mosaic PICS3™ capacitors where designed, assembled from a localized 420pF capacitor building block which was repeated 4x, 9x or 30x leading to devices of respectively 1.7nF, 3.9nF and 12.6nF (see Figure 7).

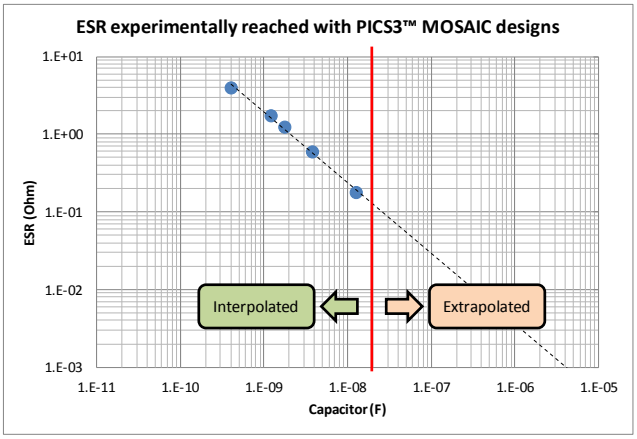


**Figure 6: ESR performances typically obtained with PICS3™ capacitors when designed in the "mosaic" way. Note that the capability of such devices to reach low (i.e. <<100mΩ) seems quite high.**

These devices were characterized in reflection to ground (T network) with GSG probes in the 300 KHz to 20 GHz frequency range at ambient temperature.

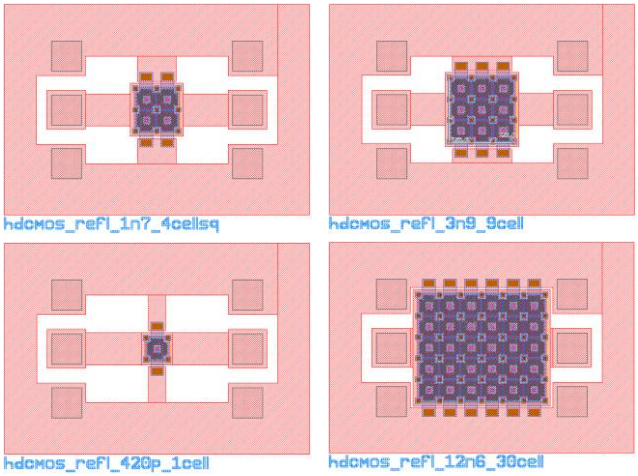


**Figure 7: GDS view of the various mosaic PICS3™ capacitors investigated. Note that GSG contacts are available for a proper de-embedding of the devices**

**RLC extraction and capacitor scaling model**

We first aimed at extracting the RLC model of the 1.7nF block and then build the idealized model of a global 12.6nF capacitors build by parallelization of 1.7nF or 3.9nF blocks. The idealized model was then correlated with real measurement performed on the 12.6nF capacitor at wafer level.

The RLC model extracted for the 1.7nF capacitor is a classical serial RLC network, where a tuning capacitor has been added to account for the structure internal coupling (see Figure 8). This RLC network is best fitted to the experimental measurements. Similar extraction work is performed on the 3.9nF and 12.6nF elements (Figure 9).

These extracted models were fitted with measurements done at wafer level. The results show that there is a excellent fit between measurements and model over the investigated frequency range whatever the capacitor size or the studied parameter (i.e. capacitance, reactance, inductance or resistance), see the 12.6nF results presented on Figure 10 by way of example.

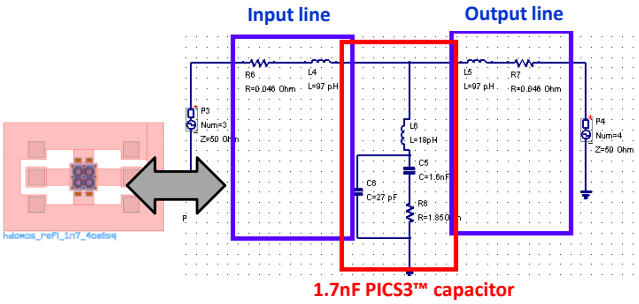


**Figure 8: The 1.7nF capacitor can be described as above: access lines are made from Resistor and Inductors (R6=R7=46 mΩ and L4=L5=97pH). The vertical branch that depicts the PICS3™ capacitor is made from an LCR serial circuit with L6=18pH, C5=1.6nF and R8=1.85Ω) with a 27pF capacitor (C6) in parallel of C5 and R8 that describes all the capacitive couplings that exist in a PICS3™ capacitor due to the high amount of 3D structures**

| | DEVICE ID (nF) | 1.7 | 3.9 | 12.6 |
|---|---|---|---|---|
| ACCESS LINE (INPUT) | R6 (Ohm) | 0.046 | 0.043 | 0.03 |
| | L4 (pH) | 97 | 88 | 50 |
| PICS3 CAPACITOR | L6 (pH) | 18 | 8 | 2 |
| | C5 (nF) | 1.6 | 3.64 | 12.6 |
| | R8 (Ohm) | 1.85 | 0.86 | 0.274 |
| | C6* (pF) | 27 | 62 | 200 |
| ACCESS LINE (OUTPUT) | L5 (pH) | 97 | 88 | 50 |
| | R7 (Ohm) | 0.046 | 0.043 | 0.03 |

**Figure 9: The extracted values for each RLC model related to the 1.7nF, 3.9nF and 12.6nF devices**

One observes out of the RLC values presented on Figure 10 that:

- Extracted capacitance is very well matched for all cases with targeted value.
- The extracted value for the global capacitor has a linear dependency with $C_{Global} = N * C_{Local}$ where N is the number of repetitions of the localized element,
- While ESR and ESL have an inverse $L_{Global} = L_{Local}/N$ and $ESR_{Global} = ESR_{Local}/N$.
- It is also noticeable that the tuning capacitor (internal coupling) geometrically scales with the size of the global capacitor.

### RLC extrapolation

Another representation of those observations can be found on the Figure 11 where a 12.6nF equivalent global array has been simulated out of the repetitions 3 and 8 repetitions of respectively 3.9nF and 1.7nF capacitors parallelized on an ideal grid. Comparisons of the RLC characteristics calculated from the model and the direct measurements of the 12.6nF block are showing a very good match over the frequency range as presented on Figure 11:

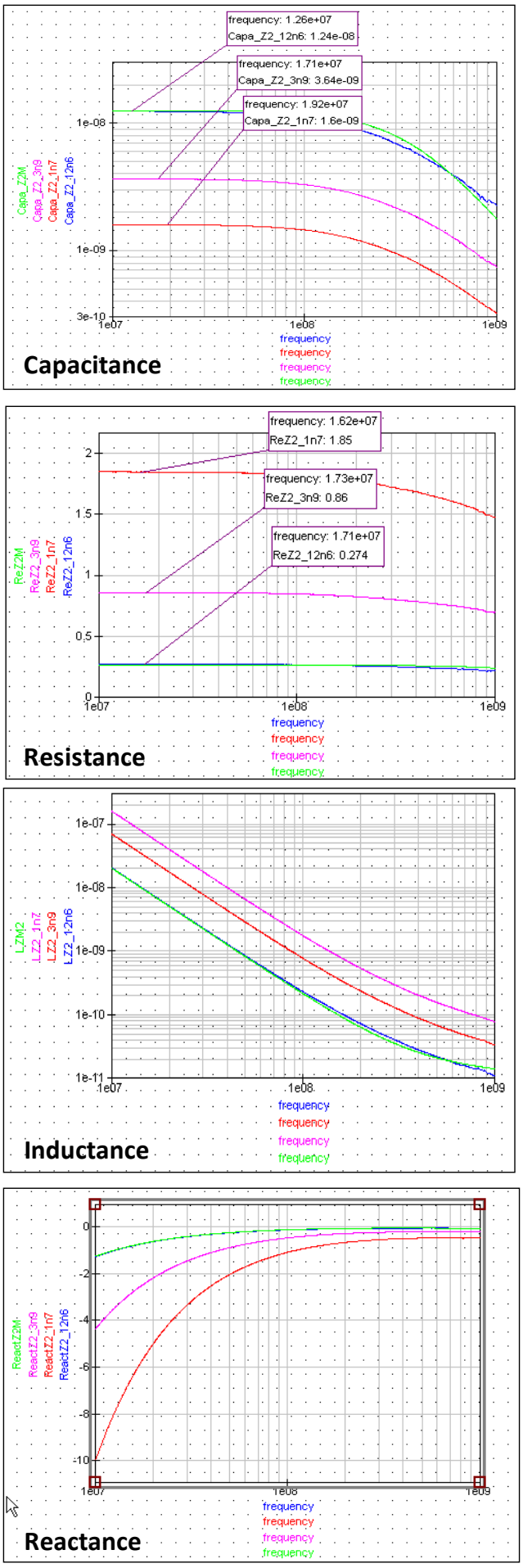


**Figure 10: Capacitance, Inductance, Resistance and Reactance measured at wafer level on the 3 investigated**

**capacitors: 1.7nF in red, 3.9nF in pink and 12.6nF in blue. The extracted and tuned RLC model behavior of the 12.6nF capacitor is shown in green. These two former set of curves (blue and green) are superposed, showing how measurements and idealized model are in perfect coincidence. The same kind of behavior is also found on the 1.7nF and 3.9nF capacitors models when compared with wafer level characterizations (not shown here)**

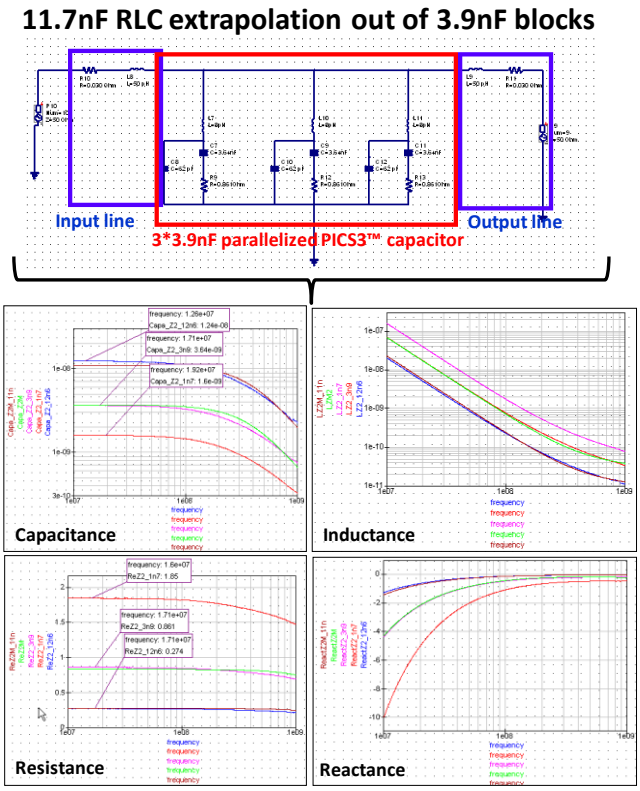


**Figure 11: Capacitance, Inductance, Resistance and Reactance measured at wafer level on the 3 investigated capacitors: 1.7nF in red, 3.9nF in pink and 12.6nF in blue. The extracted and tuned RLC model behavior of the 3.9nF capacitor is shown in green. The simulated virtual 11.7nF capacitor build from three parallelized 3.9nF elementary capacitor is shown in brown. Note that blue and brown are superposed, showing how measurements and model fit well.**

From this set of results, one concludes that while parallelizing localized capacitor cells in a "mosaic" design, the capacitance scales up geometrically, while ESR and ESL geometrically scale down with structures repetition. In other words, the more the elementary cell repetition (i.e. the higher N), the higher the device capacitance and the lower the device resistance and inductance.

Finally, according to those results one observes that the Self Resonance Frequency (SRF) should be independent from C scaling (as long as LC product is nearly constant) and thus be only a function of the localized element design. One can also observe on the Figure 11 that reactance is always negative confirming that "mosaic" PICS™ capacitors are purely capacitive devices in the considered frequency range.

Same reasoning applies to the cutoff frequency as long as the RC product remains also constant.

**Numerical scaling model**

Based on these results, we decided to perform similar analysis over a larger frequency span (10MHz – 20GHz). However the simple RLC extracted model as presented above is too coarse to provide a good fit at very high frequency. For that reason, we decided to build parallel networks directly out of localized element S-parameter measurements. For building the parallel network, we have followed the simple formalism as below:

- De-embed the S-parameter block matrix [S] from an elementary PICS3™ Mosaic capacitor using respectively open/short Y/Z transform deduction scheme
- Build the Y-parameter matrix [Y] by conversion from scattering [S] matrix
- Cascade *n* times the [Y]-parameter matrix (considering a parallel chaining) leading to a *n**[Y] where *n* = number of repetitions of the elementary PICS3™ Mosaic capacitor and [Y] the admittance matrix
- The scaled block is assumed to be a macro T block (i.e. in reflection) with scaled capacitance, as it is analyzed through [Z] transform.

The results of these calculations are presented on Figure 12. They show that scaled 12.6nF capacitor made from 3 parallelized 3.6nF blocks (or from 8 parallelized 1.7nF blocks) simulations give an almost perfect fit with the experimental measurements performed on a 12.6nF capacitor at wafer level and this, up to 20 GHz. It is also noticeable that:

- the reactance always remains negative indicating that the SRF is not reached on any element over the frequency span although it is visible that some resonance are taking place around 10GHz. This clearly indicates that the ESL is rather low.
- Those resonances are localized in the same frequency range whatever the global capacitance value is, indicating that the product ESL * ESR ≈ SRF is nearly constant.

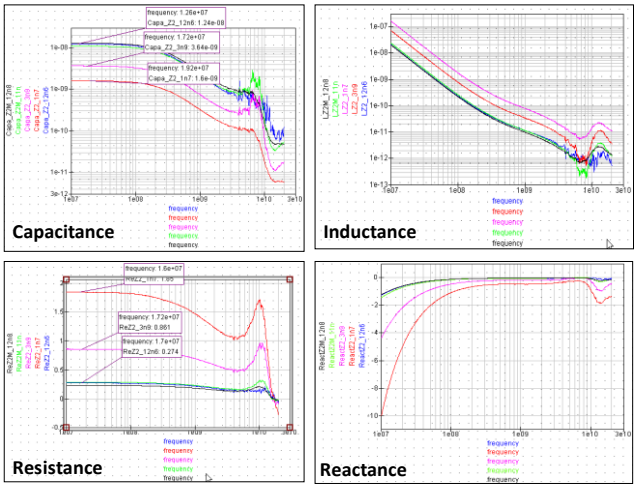


**Figure 12: Capacitance, Inductance, Resistance and Reactance measured at wafer level with respect to frequency up to 20 GHz for the 3 investigated capacitors:**

**1.7nF in red, 3.9nF in pink and 12.6nF in blue. The calculated behavior from S-parameter block of a virtual 12.8nF capacitor build from 3 parallelized elementary cells of 3.9nF is shown in green while the virtual 12.8nF capacitor build from 8 parallelized elementary cells of 1.7nF is shown in black. Note that blue, green and black curves are superposed, showing how measurements and model fit perfectly even up to 20 GHz.**

## Conclusions

The PICS™ processes from IPDIA enable the manufacturing of high-end passive components such as 3D silicon capacitors for demanding application regarding lifetime, miniaturization and performance stability like medical implantable devices. The very last PICS™ process generation called PICS4™ is able to double the capacitance density with respect to the previous one, leading to 500nF/mm² capacitor density thanks to highly engineered high-k layers. So far, this density drop go with a higher ESR since high-k materials are not able to withstand the thermal budget required to enhance the conductivity of the polysilicon material used for electrodes in the PICS™ capacitor MIMIM architectures.

A new way of designing PICS™ capacitor, called "mosaic", implementing localized elements set in a parallel grid has been demonstrated. When build with this approach, the PICS™ capacitor exhibits the following remarkable characteristics:

- Linear dependency of capacitance with $C_{Global}=N*C_{Local}$ where N is the number of repetitions of the localized element,
- Inverse linear dependency for the ESR and ESL with $L_{Global}=L_{Local}/N$ and $ESR_{Global}=ESR_{Local}/N$.
- Constant ESR*C and ESL*C resulting in constant cutoff and self-resonance frequencies
- These frequencies are driven by the design of the localized block.
- SRF >> 3GHz have thus been demonstrated for 12.5nF capacitors.
- With this approach, the resistivity of the electrodes becomes secondary with respect to the global capacitor performance as long as C and ESR/ESL can be tuned almost independently by design. This design style, combined with the optimized electrode used in the PICS3™ or PICS4™ devices, are leveraging large ESR and ESL reduction and capacitor with resistance down to 10mOhm are envisioned.

Development are now focused on extending "mosaic" concept to larger elements and to demonstrate co-integration into advanced silicon interposer intended to be used in the field of the high frequency DC/DC conversion or wideband filtering.

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