Ultra High Density Capacitors merged with Through Silicon Vias to enhance performances.

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Abstract
IPDIA presents itself as the 3D Silicon leader providing innovative platforms for customers who want to demonstrate technological concepts based on Through Silicon Vias.
The market segments Medical, Lighting, and Industrial addressed by the Ipdia Technology are adopting 2.5-D and 3-D technologies to increase the performance and density of their devices through the use of silicon interposers and through-silicon vias (TSVs).
The via last approach developed by IPDIA allows large possibility of integration combining TSV with active or passive devices such as High-density trench capacitors, MIM capacitors, Resistors, High-Q inductors or Zener diodes .

The purpose of this paper is to focus on through-silicon vias (TSV) combined with IPD, providing an interposer which could have two sides with devices. Emphasis is placed on 3D trench capacitor technology with an update of the roadmap .Examples of applications using chip-to-chip interconnections through a passive TSV interposer in a 3D IC integration system-in-package (SiP) are briefly presented. Some important results and recommendations are summarized: the process steps for passive devices interposer /TSV/redistribution layer (RDL)/microbumps /, the design rules .A comparison between TSV on active chips and passive interposer with TSV will be detailed.

1. Introduction

IPDIA is supplying TSVs for interposers with or without IPDs, high quality passive components [1], [2], [3]. Main applications are high value added products. The targeted products and markets are medical devices, aerospace, professional electronics and telecom infrastructure whereas it is just emerging in the Consumer Applications. IPDIA has expanded its through-silicon via (TSV) capabilities with a 150mm mid-end manufacturing operation including micro bump technology down to 40µm, temporary bond/de-bonding, and backside via reveal, isolation, and metallization.

2. 3D Trench Capacitor technology: the key differentiators and roadmap.

IPDIA is offering a fully mature and reliable technology providing Capacitors with Oxide/Nitride /Oxide dielectric stacks and polysilicon top electrodes yielding a capacitance density of 250nF/mm² with a minimum electrical breakdown voltage of 11V ,very low leakage current (<1nA at the working voltage), extremely high reliability (FIT < 1) and high stability . Derivative options with higher breakdown voltage are also available and the 550nF/mm² was demonstrated in 2012. Obviously this huge capacitance density increase is achievable thanks to higher k-dielectric nanolaminates and to the ALD (atomic layer deposition) enabling excellent step coverage of the deposited layers (figure1).This new worldwide record on Silicon brings high capabilities in terms of integration.

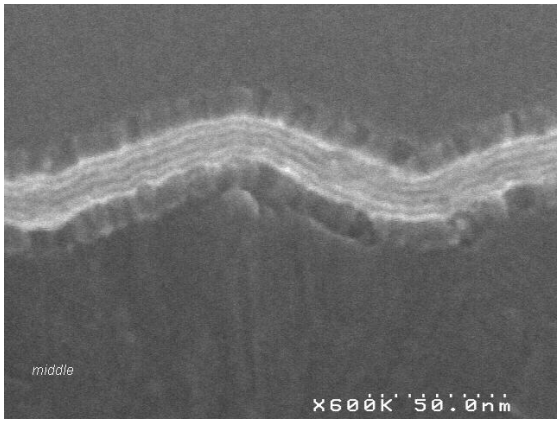

Figure 1: higher k-dielectric nanolaminates deposited in high aspect ratio pores.

The key differentiators are the following:

- The capacitor density associated to the performances and the low profile capability with a thickness varying from 80µm down to 30µm.
- High temperature and voltage stability, the capacitance variation doesn't exceed 2% from room temperature to 250°C whereas the MLCC industry shows more than 60 % variation.
- High reliability with a FIT (Failure in Time) below 1 at 225°C.
- Ultra low leakage current: IPDIA dielectrics demonstrate a typical insulation resistance above 1 **ΩF** at 300°C whereas the class II dielectric insulation resistance drops significantly when the temperature exceeds 200°C.
- The 3D Silicon capacitor can be co-integrated with high Q factor inductors, Zener diodes for high efficiency ESD protection devices .and Through Silicon Vias .

3. Examples of application :

The TSV can be combined with the 3D high density Capacitors, Resistors and high Q inductors as described in figure 2. When combined with micro bump bonding and advanced flip chip technology, this technology enables a higher level of functional integration and performance in a smaller form factor [4]

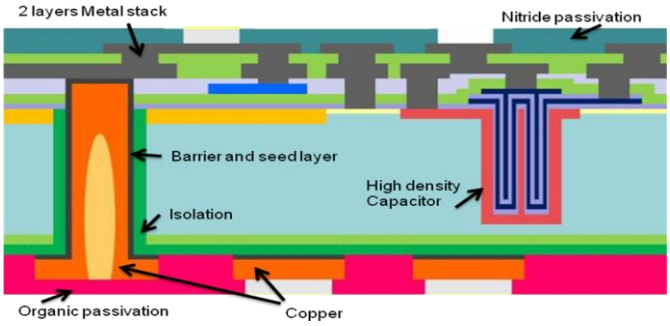

Figure 2. Silicon interposer with TSVs and High Density Capacitors , Polysilicon Resistors, MIM capacitor and Copper inductors .

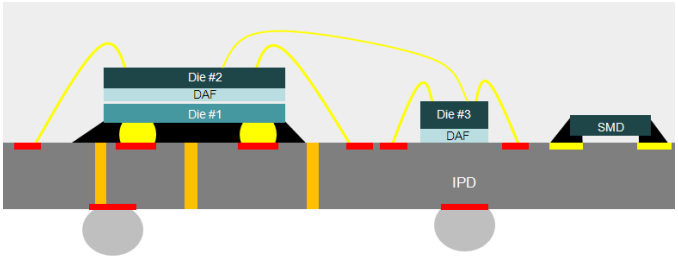

Figure 3: Example of 3D integration with IPD and TSVs

The TSV can be backside processed in pre-existing active CMOS wafers (figure 4). This solution, for example, brings indeed high value in the industry of advanced system-on-chip (SOC) probe cards, with technology leadership in both memory and SOC probe card markets. This solution addresses semiconductor test requirements and enhances the acceleration of the innovation in wafer test in position to meet the needs and roadmaps of logic and memory semiconductor device manufacturers.

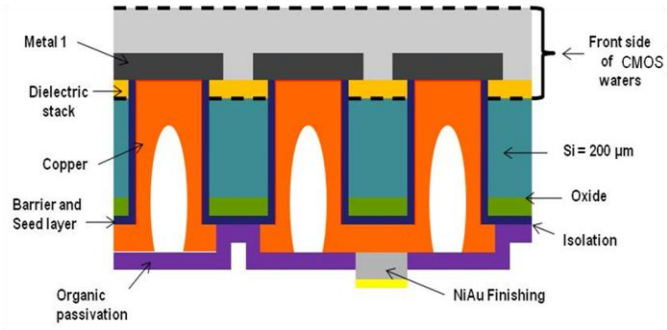

Figure 4 : Drawing of TSVs on Actives

The via last process developed by IPDIA has been expanded to 2,5D passive interposer including high density capacitors ,RF MIM capacitors , resistors and inductors and 3D interposer .

The key features are listed below:

- Up to 3 layers metal stack aluminum or combined aluminum/copper available up to 12µm thick for High Quality factor inductors .
- Wafer Thickness = 200µm
- Standard via diameter 75µm / pitch 125µm
- Low temperature oxide (<250°C) and Ti/TiN diffusion barrier for copper conformaly deposited (Figure 5)
- Copper super-filling by Electro Chemical Deposition
- Low K backside passivation
- Solderable Under Bump Metallisation (electroless NiAu or aluminum cap)
- Fine pitch copper tin pillars (figure 6) or gold posts (figure 7)

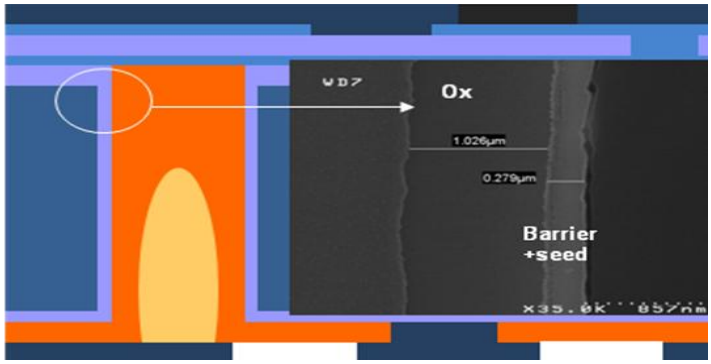

Figure 5 :Isolation + barrier + seed layers

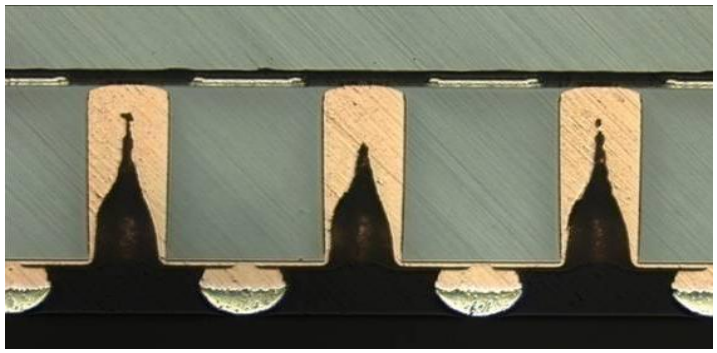

Figure 6 :Fine pitch Copper Tin pillars

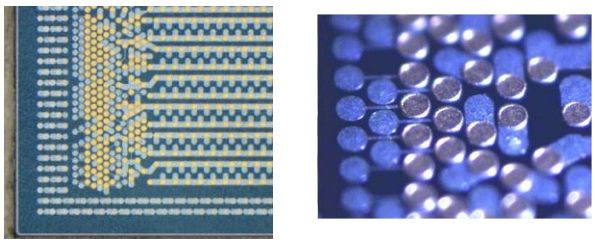

Figure 7: fine pitch gold posts

4. Measurement Results and Discussion

Electrical modeling of a TSV structure was carried out to define the required design rules. A test vehicle with different test structures was fabricated on high resistivity (1K Ω·cm) silicon substrate. Several Ground Signal Ground RF structures were implemented to extract the TSV RLC model in both reflection and transmission. The characterization was conducted at ambient temperature in a frequency range of 300Khz up to 20Ghz. The extracted RLC parameters show that the TSV structure can be used with good confidence in the DC to RF domains.

Figure 9 shows the TSV equivalent model extracted from the test structures .The model implements RLC in the signal propagation path (feed through) as well as lateral parasitic involved in the substrate and via to via coupling (figure 8) .The vehicle used for extraction implements copper vias with a via-hole diameter of 75 µm . The thickness of the Cu is fixed as 8 µm and the thickness of the insulating thick oxide is fixed as 1, 25 µm.

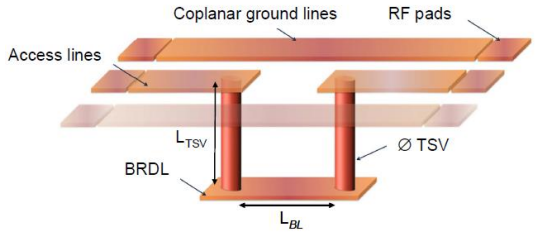

Figure 8. Dual Via Chain schematic view

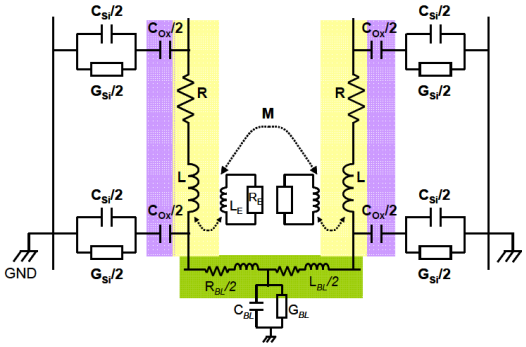

Figure 9 :TSV equivalent model , which composed of *R*, *L*, *C*, and *G*

The proposed TSV model is based on the physical structure of the TSV and is verified up to 20 GHz. The TSV inductance *L* and resistance *R*, the oxide capacitance C_{ox}, silicon substrate capacitance C_{si} and the corresponding conductance G_{si} are obtained from the test structure . All the extracted parameters are reported in table 1.

Parameters	Rdc	L	Cox	Csi	G
Test structures	124 mΩ	35pH @10 GHz	From 3 to 1,25pF Tox=1,25um	From 100 to 45 fF	< 1mS up to 20 GHz

Table 1: Equivalent Circuit Model Parameters of G-S-G TSV Structure.

The low conductance (G) is appropriate for design configuration where high isolation schemes are required. This characteristic is due to the high resistivity substrate [10],[11] combined with a sufficient via pitch . The Capacitance of the Silicon (Csi) that is dominating inter-TSV coupling path in the RF domain (above 2 GHz) is in the order of 50fF and slightly reduces (as expected) for larger pitch. The graph below is representing 2 TSVs intrinsic parasitic: the substrate capacitance (Csi) and the oxide (Cox) capacitance, estimated to 1,25pF (for an oxide thickness of 1,5um, a TSV diameter of 75µm and a depth of 200um).

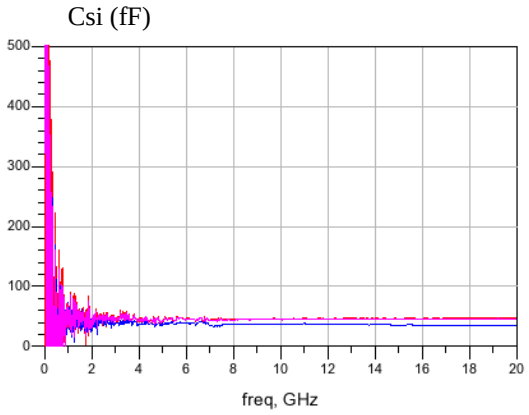

Figure 10 : Inter-TSV equivalent capacitance for a TSV pitch od 250µm (pink) and 500µm (blue)

The Figure 11 shows the measured and simulated S-parameters of a test structure implementing a transmission through 2 vias inter-connected by adapted lines (see figure 8) measured @ wafer level..

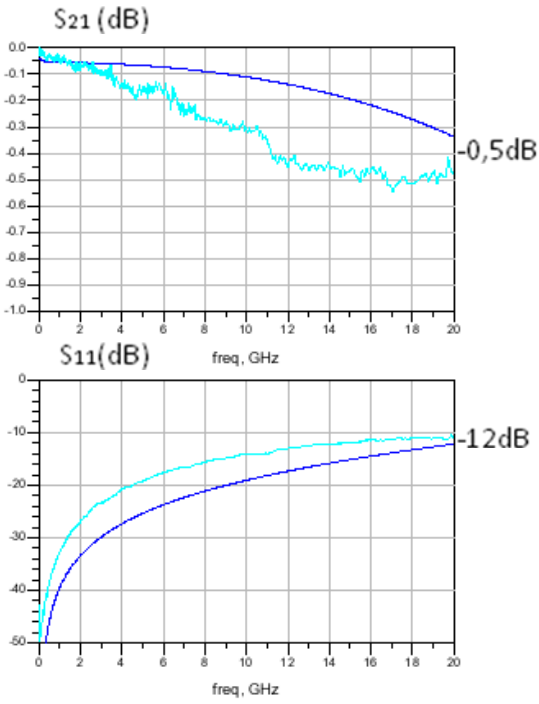

Figure 11 : Measured and simulated S-parameters: Transmission coefficient, S21, Reflection coefficient, S11 for

TSV .remarkably the insertion loss @ 20 GHz is <0,5dB and the reflection to GND is -12 dB

7. Conclusions and Recommendations

Passive integration technologies coupled with 2,5D/3D-interposers bring differentiation and miniaturization. Main driver is the packaging integration density, with Integrated Passive Devices, Through Silicon Vias and external IC integration.

The TSV via last process developed by IPDIA can be co-integrated in a Silicon interposer with high value capacitors, resistors, RF MIM capacitors and copper inductors. This TSV process can also be used on CMOS wafers.

A test vehicle implementing TSV parasitic extraction structures has been processed and characterized. An equivalent RLC electrical model has been extracted in a frequency domain from 300Khz to 20 GHz. Some important results and recommendations are summarized in the followings:

1) The parameters calculated using the analytical equations confirmed that the proposed TSV model approach leads to a well-defined physical-based model.

2) The simulation and measurements show that thanks to a dielectric deposited with high thickness along the via sidewall a good electrical insulation is achieved [12],[13]. This combined with proper substrate characteristics allows reduced insertion loss i.e. lower than 0.5 dB at 20GHz,.

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