Ultra Low Profile Silicon Capacitors (down to 80 µm) applied to Decoupling Applications. Results on ESR/ESL.

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Abstract

This paper covers technological advances on ultra low profile silicon capacitors for embedded applications and System in Package modules. It also presents a novel approach to design high density PICS® silicon capacitors to control and optimize their ESR values preserving low intrinsic ESL values that are beneficial for applications at very high frequencies.

Keywords:
*Ultra low profile capacitors, silicon capacitors, ultra low ESR, ultra low ESL, decoupling applications, PICS®
technology.*

Introduction

As consumers are eager to get the most cutting-edge products, manufacturers have to adapt their technologies and continue to drive innovations to offer the most advanced electronic equipment. Two key features must often be considered for electronic devices: size and performance.

In the case of embedded applications and System in Package modules, not only must the size of the device be optimized in x and y axes, the thickness is also highly important. IPDiA is the 3D Silicon leader providing a full range of silicon capacitors, including some with ultra-low profile - down to 30 µm - developed and offered for decoupling applications with space constraints (memory products like smartcards, memory modules, RFID packages, flash memory cards, etc).

In terms of performance for decoupling applications, the main feature that needs to be improved is the signal integrity of the integrated circuit. On top of the low profile feature, these applications are very demanding in signal integrity and decoupling capacitors are considered to be one of the best solutions in terms of efficiency and cost to reduce the voltage fluctuation. However, decoupling capacitors are not perfect and their performance depends not only on the capacitance but also on the Equivalent Series Resistance (ESR) and on the Equivalent Series Inductance (ESL) [1], [2]. Figure 1 shows the equivalent circuit of a capacitor, taking into account the parasitic effects induced by the ESR and the ESL [3].
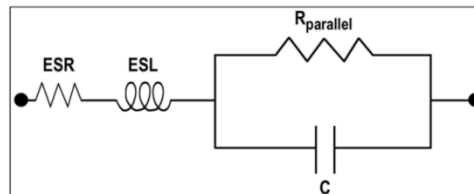

Figure 1: Electrical schematic of a decoupling capacitor

The total ESR figures the energy loss in the system combining dielectric losses (frequency dependent) with the resistance of the electrodes (constant value). Figure 2 shows the typical shape of the curve obtained for a capacitor when considering the impedance versus the frequency.
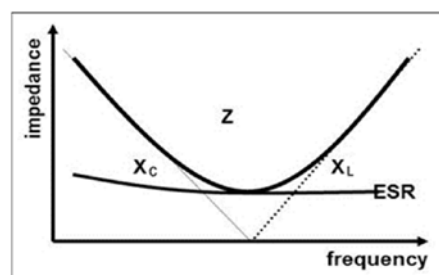

Figure 2: Typical curve Z vs f

This comes from $|z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$ where $\omega = 2\pi f$

- At low frequencies, the impedance related to the ESL tends to zero and Z depends mainly on the capacitive term.
- At the self-resonance frequency, the inductive and capacitive values cancel each other out and the only parasitic effect is due to the resistance of the conductive parts of the capacitor. At this point, the capacitor reaches its minimum impedance.
- At high frequencies, the capacitive part tends to zero and Z depends mainly on the ESL.

For a long time, ESR was the main parameter to be considered. But as the race for higher-speed applications gathers pace, capacitors with low inductive parasitics at high frequencies are needed [2]. This trend leads manufacturers and designers to take into account the ESL parameter. This further complicates the work of designers, who need to consider the constraints imposed by these parameters. The IPDiA R&D team has addressed this issue with its high density capacitors. The ESR/ESL performances obtained after reshaping the PICS capacitor structure will be described in this paper.

Ultra Low Profile Silicon Capacitors

The race to more and more miniaturization is the daily concern of electronic designers and this is especially true for embedded and System in Package applications where the z constraint is added to the x and y constraints. The results given in the following paragraph were detailed in 'Low Profile Integrated Passive Devices with 3D High Density Capacitors, ideal for embedded and Die Stacking Solutions' [4].

1/ PICS technology: the path to miniaturization

The manufacture of IPDiA passive components is based on the PICS technology (Passive Integration Connecting Substrate) developed in IPDiA's own R&D center. This technology takes advantage of the thickness of silicon to integrate hundreds of passive components such as high-Q inductors, resistors, MIM capacitors and trench MOS capacitors in one single die. This technology has already proved its efficiency in terms of area saving. The 3D trench depth of the silicon capacitor drives the results obtained in terms of thickness and capacitor density. Table 1 shows the die thickness obtained and the corresponding capacitor density.

Process Node	Capacitor Density	Minimum die thickness
PICS1	25 nF/mm^2	30 µm
PICS2	80 nF/mm^2	50 µm
PICS3	250 nF/mm^2	80 µm
PICS4*	500 nF/mm^2	80 µm
PICS5*	1 µF/mm^2	80 µm

Table 1: Die thickness and the corresponding capacitor density
*Under development

IPDiA R&D experts are working continuously in collaboration with leading institutes to anticipate the demands for 'smaller, faster and better'. Figure 3 shows the IPD (Integrated Passive Devices) low profile roadmap.
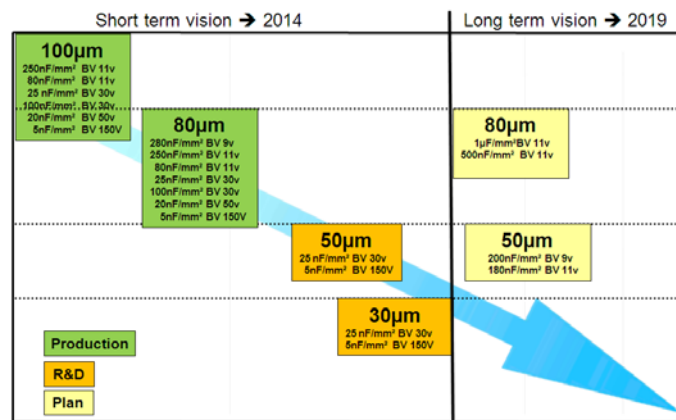

Figure 3: IPD low profile roadmap

2/ Low Profile Silicon Capacitors down to 100 μm for embedded systems

Passive components have proved their value in enhancing the performance of the IC, but electronic designers need to consider the space these components take up in the overall system and find solutions to get the smallest possible footprint, especially for embedded applications. The low profile 100 μm silicon capacitors qualified and in mass production since 2011 at IPDiA, have been developed with the aim of keeping a high level of flexibility, efficiency and accuracy within the embedded system. Several tests on IPDiA low profile silicon capacitors have proved the superior stability and reliability of the components over a wide range of temperatures. It has been shown that cumulative failure for the low profile 100 μm technology is less than 1 ppm in 10 years of use for tests conducted from -65 °C to +150 °C [4]. Figure 4 shows a 100 μm die embedded in a PCB.
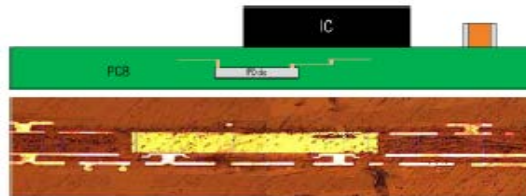

Figure 4: 100 μm die embedded in a PCB

3/ Low Profile Silicon Capacitors down to 80 μm for System in Package

IPDiA R&D experts have worked on low profile silicon capacitors down to 80 μm with suitable form factor and performance in System in Package for memory products (smartcards for instance). 80 μm IPDiA silicon capacitors have been subjected to electrical tests after normalized bending conditions for smart card applications. Stability has been improved with a maximum capacitance variation before/after bending of 1.2 % and 11.5 % for the leakage current. In conclusion, this has qualified the PICS technology for smartcard applications since the 3D capacitors were not damaged during the mechanical tests [4].

ESR/ESL Contribution

To cope with the increased demand for more sensitive devices and faster transition in the IC, power integrity must be guaranteed and therefore impedance minimized while maintaining the availability of a wide range of capacitance values. The output ripple voltage is directly related to ESR values. As input/output voltages of modern DC/DC converters are getting lower & lower, this input/output ripple due to ESR is an increasingly important parameter that has become challenging to solve with standard MLCCs. In the past decades, all capacitor parameters were measured at a standard of 1 MHz, as DC/DC converters were operating at 10 kHz. But in today's high frequency world where the trend in DC/DC converters is to operate in ranges of tens of MHz, this is far from sufficient. Ideal values for a good high frequency capacitor for a given capacitance could run in the order of about 50 mΩ at 200 MHz, 110 mΩ at 900 MHz and 140 mΩ at 2 GHz. To reach a global impedance of 140 mΩ at 2 GHz, as this frequency is way above the SRF, several MLCCs must be added in parallel. Designers, however, need to find a capacitor with very low impedance over a broad frequency range.

IPDiA R&D's team of experts has addressed the ESR issue and has worked on finding the best compromise between high capacitance and low ESR. The following results have been fully detailed in 'Silicon Interposers with Integrated Passive Devices, an excellent alternative to discrete components' [5]. The aim of their research is to work on a new generation of PICS capacitors using PICS4 technology to reach a value of 500 nF/mm^2. On the basis of

$$C = \frac{\varepsilon_0 * \varepsilon_r * S}{t}$$

experts have worked on the very high aspect ratio 3D structures commonly used in PICS technology and adapted the nature of the dielectric material to increase ε_r and consequently C. A value of 500 nF/mm^2 has been reached with the same performance as that obtained with PICS3 in terms of lifetime, leakage current and breakdown voltage. However, high K stack used for higher density capacitor is more sensitive to high thermal budget. Consequently, the thermal budget after high K deposition has been reduced, resulting in higher capacitor electrode resistivity. To overcome this new constraint, research has shifted to define a new PICS capacitor with quasi-fractal design, the so-called 'Mosaïc' that provides a way of reducing the ESR/ESL of the global structure. The approach consists in increasing the contact density with the electrode to obtain a less resistive backend (metallic) grid. Optimization is carried out to minimize the grid ESR and ESL while the individual Mosaïc cells are massively parallelized to control the global ESR/ESL.

Figure 5 represents the new 'Mosaïc' PICS capacitor design compared with the standard design. The elementary cell which serves as a basis of the Mosaïc is also shown.

STANDARD PICS™ CAPACITOR DESIGN

"MOSAIC" PICS™ CAPACITOR DESIGN

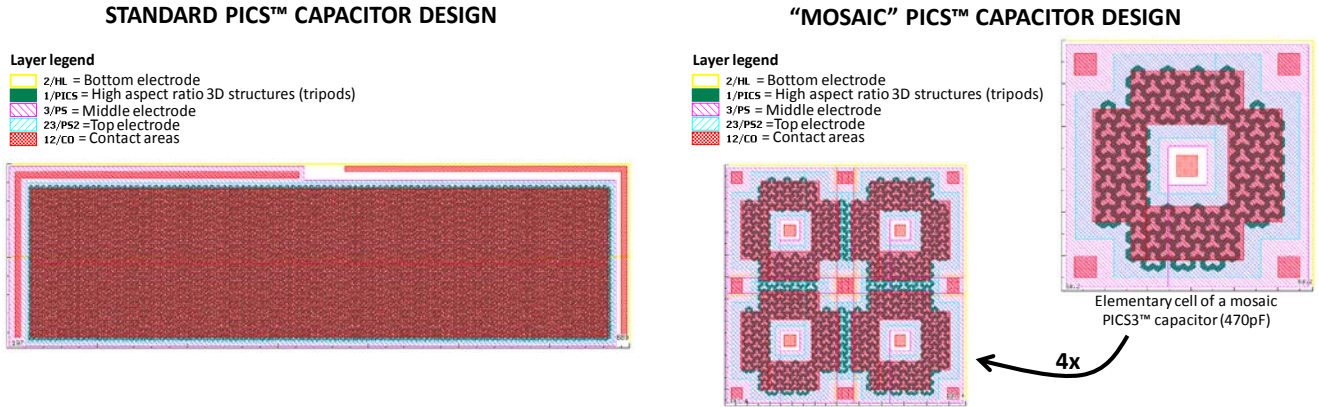Elementary cell of a mosaïc
PICS3™ capacitor (470pF)

4x

Figure 5: Standard PICS capacitor design compared with Mosaïc PICS capacitor design. The ESR is driven by the capacitor shape/outer extend in the standard design when it depends on the localized element in the Mosaïc. ESR_{Global} becomes a variation of 1/N in the second case, N being the number of elementary cells parallelized.

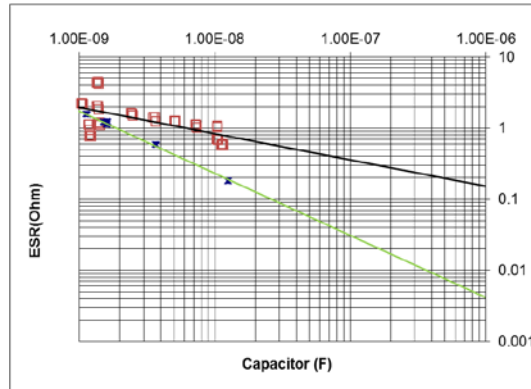Results on ESR for standard PICS capacitors and Mosaïc PICS capacitors are shown on Figure 6.

Figure 6: Comparison of PICS3 unconstrained design (black line) vs Mosaïc design (green line) for 1 type of Mosaïc cell. Other ESR compromises can be achieved in Mosaïc by changing the basic cell design.

A significant improvement can be observed: thanks to the new design set-up for PICS capacitors, the ESR value is reduced by a factor of 10 for a typical capacitance value of 100 nF.

For a specific Mosaïc design, so fixed contact density and fixed capacitance density, figure 7 shows the variation in ESR with respect to the size of the capacitive element. As stated earlier, we see that the capacitive element is assimilated to a parallel network where C is proportional to n (n=number of repetitions) while ESR is proportional to 1/n. The chart shows real silicon measurements up to 12 nF, and extrapolated results for larger capacitors.
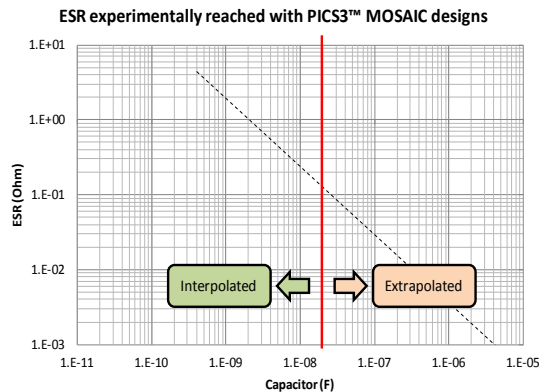

Figure 7: ESR vs capacitance for a Mosaic PICS capacitor design

These promising results are paving the way to a new generation of capacitors with ESR possibly as low as 10 mΩ.

Figure 8 shows the ESR characteristic corresponding to different MOSAÏC design. Each design presents a different trade-off on capacitance density based on PICS3 technology. The capacitance density reduction corresponds to a higher contact density providing superior ESR/ESL characteristics.
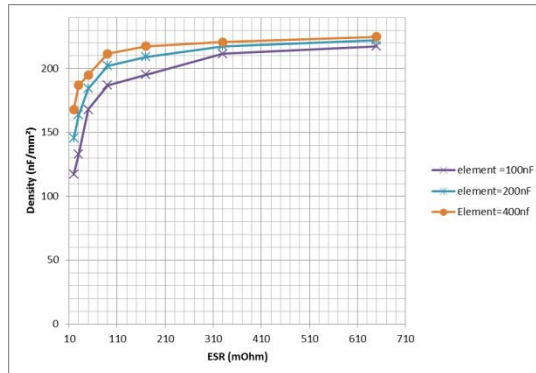

Figure 8: density/ESR trade-off for various PICS3 capacitors

We can therefore conclude that whilst offering 100 times more capacitance density (2000 nF/mm^3 vs 20 nF/mm^3), IPDiA 3D Silicon capacitors offer also ESR characteristics of 20 mΩ vs 100 mΩ when compared with Type I capacitors. For Type II, IPDiA offers unique capacitance stability performance with ultra low profile of 80 µm and ESR values at 20 mΩ when X7R & X5R offer a standard thickness of 300 µm at the same level of ESR and lower stability performance.

We have also seen in the introduction that a good decoupling capacitor must be efficient over a wide range of frequencies. The impedance magnitude for the IPDiA Mosaïc capacitor has therefore been compared with COG and X7R capacitors giving the graph on figure 9. We can see that no inductive transition is observed up to 10 GHz for the PICS capacitor and that it acts as a low-impedance element over a wide range of frequencies while X7R and COG capacitors act as low-impedance elements over a limited range of frequencies. IPDiA PICS capacitor provides the best result in terms of low impedance for frequencies higher than 20 MHz compared with COG and 35 MHz compared with X7R.
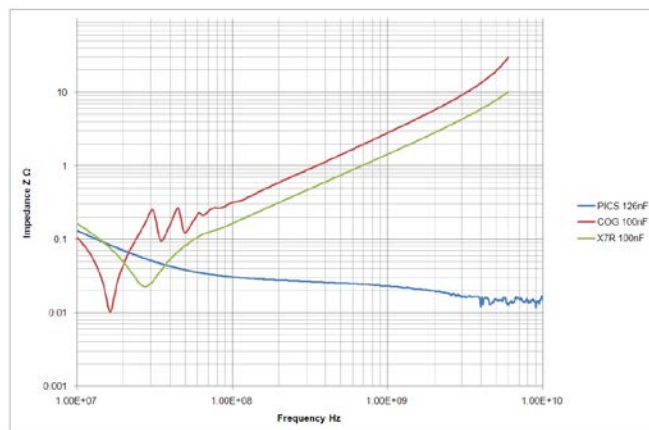

Figure 9: Impedance magnitude for 100 nF capacitor element. Comparison of PICS, COG and X7R

Improving decoupling performance has usually been based on the idea of reducing the ESR. Low ESR MLCCs have been widely used for this purpose. However, nowadays, in new DC/DC converters operating at much higher frequencies, a very low impedance device is required. A standard capacitor can in fact only be used up to the SRF. Above the SRF, the user essentially has a "DC blocking inductor". In order to extend the usable frequency range in such applications, IPDiA is offering ultra low ESL structures, which drastically decrease the overall impedance above the SRF and offer the best solution for decoupling performances in the 35 MHz to 10 GHz frequency range.

Conclusion

IPDiA PICS capacitors offer a combined solution of low profile, high capacitance and low ESR/ESL to meet the needs required in decoupling applications (high density SIM, smartcards, memory modules and other applications with space constraints). In addition to high performance results on low profile capacitors, a novel high density silicon capacitor design has been revealed with promising results on ESR and ESL, making PICS capacitors the best alternative for decoupling applications.

References

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