Copper Electroplating process for passive Si-based System in Package applications

L. Hamelin[1], S. Ledain[1], E. Dufour-Gergam[2] and C. Bunel[1]

[1] NXP Semiconductors Caen, 2, rue de la girafe, BP5120, 14079 Caen cedex 5, France
[2] IEF, institut d'électronique fondamentale Université Paris-Sud, 91405 Orsay, France

[1]Tel/Fax: +33 2 31 45 31 98, E-mail: laetitia.hamelin@nxp.com
[2]Tel/Fax: +33 1 69 15 77 23, E-mail: elisabeth.dufour-gergam@ief.u-psud.fr

Abstract

NXP has been involved these last years in PICS technology (Passive Integrated Connective Substrate) for passive components such as high-density capacitors, inductors and resistors. In order to improve the electrical characteristics of these devices and more particularly of inductors, top aluminum metal can be replaced by a thick copper layer. This paper will describe a study concerning a micromolding copper process for these PICS substrates. High deposition rate (1 µm/min), thickness distribution and uniform electrical characteristics (close to bulk values) are the main challenges for the industrial deposition process. We used two sets of electrolyte (sulphate bathes) with organic additives. Additives consumption and degradation have been carefully monitored using CVS (Cyclic Voltammetric Stripping) and TOC (Total Organic Compounds) analysis.
A wide range of current density (2 to 5 A/dm^2) was used to optimize the process. Copper deposition was performed on various pattern geometries representative of our products. For the two types of electrolyte, the wafer uniformity is as targeted (< 5%) but differences are observed for the within die uniformity (up to 1.5µm depending on the design). In the selected range of current density, the growth rate is below expectations. Both chemistries lead to low surface roughness (<25nm) for all current densities evaluated. Copper line profile is flat in one case and curved on the other one; this curved profile can have a negative impact for some applications. The electrical resistivity varies from 1.7 µΩ.cm to 2.3 µΩ.cm.
Finally, the process developed fulfills the main technical requirements (thickness uniformity, low roughness, good electrical performances…) but strong differences in bath management and additive consumptions have allowed to select one of the electrolyte for our applications.

Key words: Copper Electroplating, Patterned Copper, Passive components, Cu crystallization

1. Introduction

Electrochemical plating (ECP) is presently the most popular method used for Cu deposition in semiconductor fabrication processes. This process technology has been introduced by NXP 4 years ago to anticipate future needs of the passive substrate technology [1,2].
For these industrial applications, the copper deposition process must lead to reproducible results. High growth rate must be, low Cu roughness and a resistivity value close to the bulk are the main objectives. In this study, 2 electrolytes ("Electrobrite" and "Cabas") commercialized by Rockwood industry were evaluated.

2. Experimental set-up

The study presented in this paper was performed with the "Microform200" electroplating tool manufactured by Technotrans. The electroplating cell contains a high volume of electrolyte (65L) as requested in an industrial environment. Bath temperature is maintained at 24 °C and solution agitation is realized by the electrolyte flow (12l/min) and by sample rotation (66rpm).
Both baths are sulphate acid solution with different compositions. Electrobrite exhibits a lower copper concentration than Cabas. In both cases, 3 organic additives are present: brightener, suppressor, and leveler, but their nature and concentration are different. The Cu deposition was performed on silicon 6'' substrates (675 µm thick) coated with 500nm SiO2 / 50nmTi / 550nm PVD Cu. In this work, the electroplated copper is deposited through a photoresist mold (SPR 220, Shipley) or on blanket wafers (no mold). The different steps of the micromolding process are described figure 1.

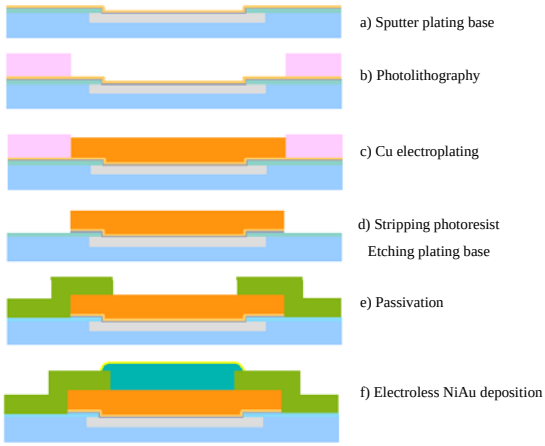


Figure 1. Schematic representation of the copper micromolding process.

3. Results and discussion

a) Growth rate

The evolution of the growth rate with the current density is shown on figure 2, for each electrolyte and for both kinds of substrate (Blanket and patterned wafers).

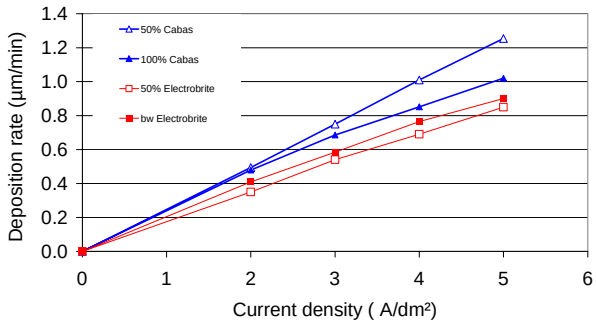


Figure 2. Deposition rate vs current density for the 2 electrolytes, for blanket wafers and patterned wafers

In all cases, the deposition rate increases linearly with the current density in agreement with the Faraday's law. For the 2 electrolytes, the growth rate is quite similar and can reach 1µm/min for the highest current density. This value is also depending on opened areas as patterned wafers always exhibit different deposition rates than blankets wafers for the same current density. This latter is a critical point for industrial applications: growth rate is depending on the pattern geometry and the spatial distribution.
For Cabas electrolyte, the growth rate on blanket wafers is slightly inferior to those obtained with patterned wafers. The opposite effect is observed for electrobrite. This could be due to the nature of the different additives.

The recommended current densities are 3 to 4A/dm² for these electrolytes. In this range, deposition rate is often lower to our target (1µm/min).

b) Thickness uniformity

The photolithographic mask design will affect strongly the distribution of the potential lines [3]. Thus, current distribution is influencing thickness uniformity in the Cu patterns. Cu thickness was measured at different points of the wafer on the same patterns for both electrolytes. A specific Cu design with several patterns sizes has been measured to characterize the within-die uniformity and the within-pattern uniformity.

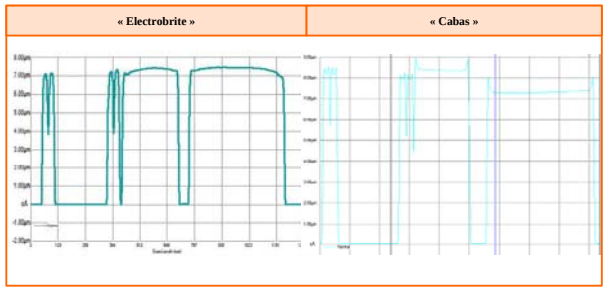


Figure 3. Copper profiles for different patterns sizes, for the both electrolytes

As seen on figure , no significant thickness variation is observed in our design with Electrobrite ; the within-die uniformity is below 5% (max-min/avg) for 2 to 5ASD. For Cabas, the pattern environment is leading to strong differences in Cu thickness (up to 1.5µm between large and small patterns). This effect is due to the current lines distribution on the wafer but also to the activation of the additives. For this electrolyte, the within-die uniformity is evaluated at 14% (max-min/avg), which is not compatible with industrial applications. Moreover, an edge effect is systematically observed ("rabbits ears").
To conclude, within-die uniformity seems to be governed mostly by the additives chemistry, as uniformity is not influenced by the current density.

c) Morphology

Optical observation shows that copper exhibits a shiny surface for both electrolytes.

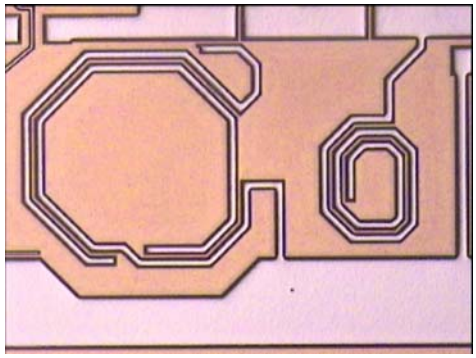


Figure 4 : Optical microscope view of Cu surface

As expected, low surface roughness is obtained whatever is the current density. Nevertheless, Cabas electrolyte leads to slighly smoother surfaces (rms roughness <10 nm) than Electrobrite electrolyte (rms roughness <16 nm). A typical AFM image can be seen on the figure 5 for Cabas electrolyte.

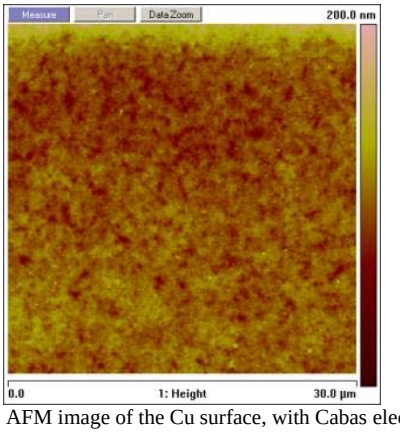


Figure 5. AFM image of the Cu surface, with Cabas electrolyte

d) Electrical properties

The electrical resistivity was measured using the 4 probes technique. for the 2 electrolytes and for all current densities evaluated, the material resistivity measured directly after copper-electroplating process is higher than for bulk material (1.7 µOhm.cm). This resistivity value is decreasing significantly with time, probably because of the Cu recristallization step at room temperature [4].

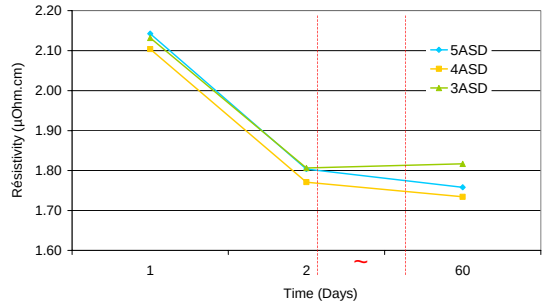


Figure 6. Effect of time on the Cu resistivity for the Electrobrite electrolyte

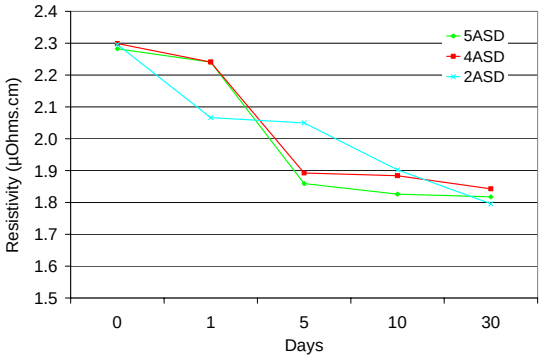
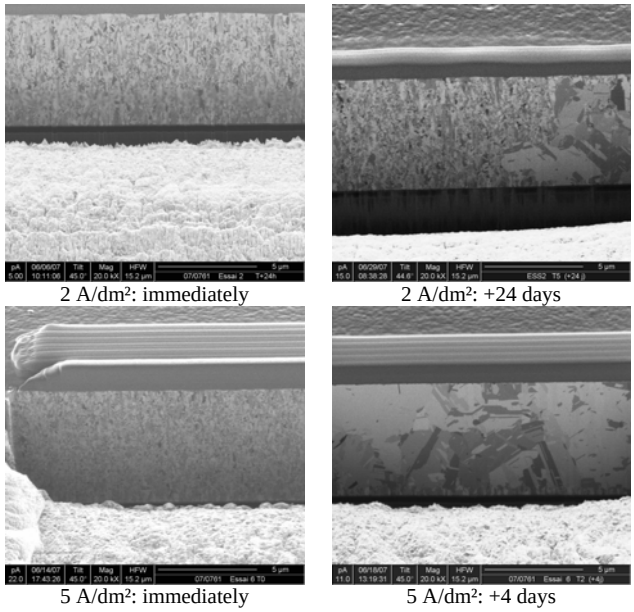


Figure 7. Effect of time on the Cu resistivity for the Electrobrite electrolyte

For cabas samples, the evolution of the Cu microstructure with time at room temperature was studied. For all current densities, Focused Ion Beam cross sections were performed immediately after plating and at regular intervals up to 24 days. SEM views of these cross-sections are seen on figure 5.



2 A/dm²: immediately | 2 A/dm²: +24 days

5 A/dm²: immediately | 5 A/dm²: +4 days

Figure 8. FIB cross sectional view of the Cu evolution with time, at 2 and 5 A/dm²

Immediately after plating, the Cu lines are always composed of fine grains for all current densities. However, at 4 and 5 A/dm², grains become even smaller. In metallic electrodeposition process, this evolution of the Cu texture with higher current density has already been reported [5].

One can observe after 4 days that samples processed with low current densities still exhibit rather fine texture whereas on other samples large grains are visible. For the low current density value (2ASD), 24 days are necessary to significantly increase the grain size. The decrease of the Cu resistivity is correlated with the microstructure of the Cu lines, as seen on figure. After 30 days at room temperature, all samples reach a quasi-bulk material resistivity value (~ 1.8µOhm.cm). Similar results are obtained using a thermal treatment at 350°C during 1h in a N2 flow oven.

Samples processed with Electrobrite copper grains are rather large and exhibit a quasi-colonar orientation immediately after plating (figure 9).

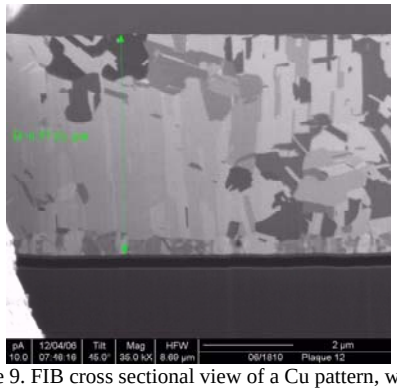


Figure 9. FIB cross sectional view of a Cu pattern, with Electrobrite electrolyte

In agreement with the microstructure, the electrical resistivity is decreasing more quickly and reaches the quasi-bulk value only after 2 days, for all current densities.

e) Mechanical properties

The differences of Coefficient of Thermal Expansion (CTE) between the layers at the wafer surface can lead to high wafer warpage.

The mechanical deformation of the substrate induced by stress, must be limited to avoid issues during further processing steps (passivation, wafer thinning, assembly...).

For Cabas electrolyte, the evolution of the bow value was measured using DFG840 equipment before and after the Cu electroplating steps, after the thermal treatment and finally after the thinning of the substrate. This thinning step is performed using successively a mechanical and chemical etching (for the last 20µm). The final thickness of the substrate is 300µm.

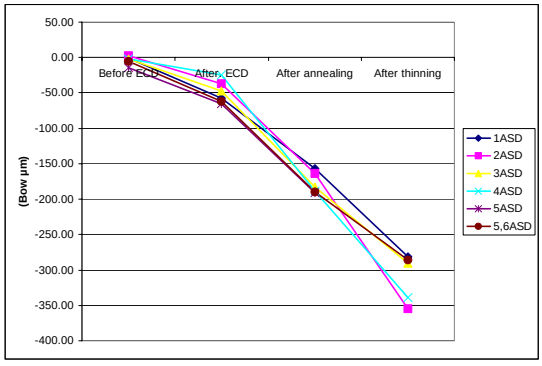


Figure 10. Evolution of the bow for the different steps of the process, with Cabas electrolyte

For all steps, the mechanical properties do not depend on the current density value. Measurements on figure clearly show that the Cu thermal treatment is a critical step for wafer deformation.
The use of lower temperatures for the Cu annealing could reduce the stress, nevertheless the passivation layer selected for our process requires an annealing step at 350°C during 1 hour.
After the thinning step, the bow value is important (350 µm) possibly generating difficulties for the industrialization of the process.

4. Conclusion

In this paper, we demonstrated that the two types of electrolyte could be used for passive components fabrication process using electroplating method. Satisfactory Cu properties are obtained: smooth surface and low resistivity.
Using the Cabas electrolyte, a slightly higher growth rate and the target value of 1µm/min are reached. However, rabbit ears profile and non-acceptable within-die uniformity kept us from selecting this electrolyte for our application.
Electrobrite electrolyte allows to get the targeted Cu profile and within-die uniformity but induced a difficult bath management and a high consumption of additives that makes its industrialization critical.

4. References

[1] D. Chevrie et al., A silicon based System in Package (SbSIP) technology, 15th European Microelectronics and Packaging Conference , Bruges, June 12-15, 2005.

[2] F. Roozeboom et al., Passive and heterogeneous integration towards a silicon-based System-in-Package concept, Thin Solid Films 504 (2006) 391-396.

[3] J. K. Luo et al. Uniformity Control of Ni Thin-Film Microstructures Deposited by Through-Mask Plating, Journal of The Electrochemical Society, **152,** C36-C41, 2005

[4] S. Lagrange, S.H. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, R. Palmans, K. Maex, Self annealing characterization of electroplated copper films, Microelectronic Engineering, **50**, pp 449-457, 2000.

[5] C. Fan, J.P. Celis, J. P. Roos, Surf. Coatings Technol., vol. 91, p. 220-224, 1997