Integrated Passive Devices and TSV, a disruptive technology for miniaturization.

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Abstract

The 3D Silicon technology of IPDiA is a disruptive technology for miniaturization adopted by the best players in the Medical and Industrial segments for its outstanding performance and reliability demonstrated in harsh environments. The high density capacitors with multiple metal-insulator-metal (MIM) layer stacks in 3D structures reaching 250nF/mm2 already in production for several years is at the forefront of the research program where CEA-Leti and IPDiA are jointly providing innovative platforms for customers who want to combine these capacitors with Through Silicon Vias in order to demonstrate new technological concepts . The via last approach selected by IPDIA allows large possibility of integration combining TSV with active or passive devices such as High-density trench capacitors, MIM capacitors, Resistors, High-Q inductors or Zener diodes . In this paper, the interaction between TSV and IPD will be studied. Emphasis will be placed on the robustness of the 3D trench capacitor technology .Examples of applications using chip-to-chip interconnections through a passive TSV interposer in a 3D IC integration system-in-package (SiP) will be illustrated .

Key words

3D trench capacitor, SiP, Interposer, Through Silicon Vias .

I. Introduction

IPDIA is supplying TSVs for interposers with or without IPDs, high quality passive components [1], [2], [3]. Main applications are high value added products. The targeted products and markets are medical devices, aerospace, professional electronics and telecom infrastructure. IPDIA has expanded its through-silicon via (TSV) capabilities with a 150mm mid-end manufacturing operation including micro bump technology down to 40µm, temporary bond/de-bonding, and backside via etching, isolation, and metallization.

II. 3D Trench Silicon Capacitors

IPDIA is offering a fully mature and reliable technology providing Capacitors with Oxide/Nitride /Oxide dielectric stacks and polysilicon top electrodes yielding a capacitance density of 250nF/mm² with a minimum electrical breakdown voltage of 11V ,very low leakage current (<1nA at the working voltage), extremely high reliability (FIT << 1) and high stability . Derivative options with higher breakdown voltage are also available and the 550nF/mm² was demonstrated in 2012 and characterized in 2013 with the same performances as the previous node (250nF/mm²). Obviously this huge capacitance density increase is achievable thanks to higher k-dielectric nanolaminates and to the ALD (atomic layer deposition) enabling excellent step coverage of the deposited layers .This new worldwide record on Silicon brings high capabilities in terms of integration.

A. Capacitor Structure

The capacitors are fabricated in reactive ion etching etched arrays of pillars with high aspect ratio and high density (Fig. 1). These 3D structures are combined with MIMIM architecture (Fig. 2) in order to double the capacitance value reachable by a single MIM (Metal Layer Dielectric Insulating layer Metal Layer). The Oxide/ Nitride /Oxide dielectric used in the previous nodes is replaced by higher k-dielectric nanolaminates deposited by ALD (atomic layer deposition) to reach the highest performance in term of coverage. (Fig. 3)

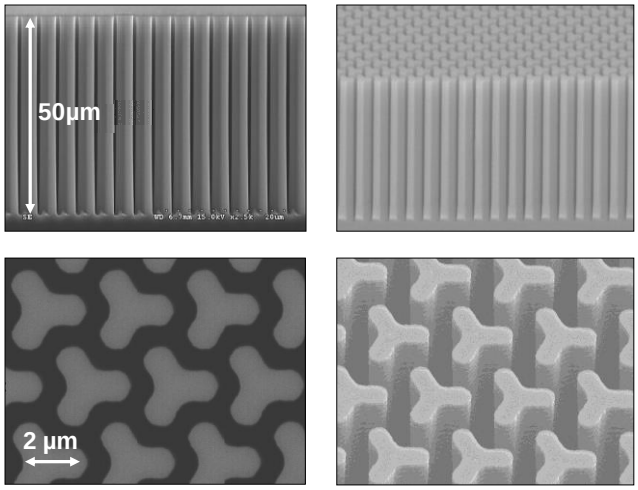

Figure 1: SEM pictures of the high aspect-ratio pillars etched in the silicon substrate (tripods of AR= 50:1)

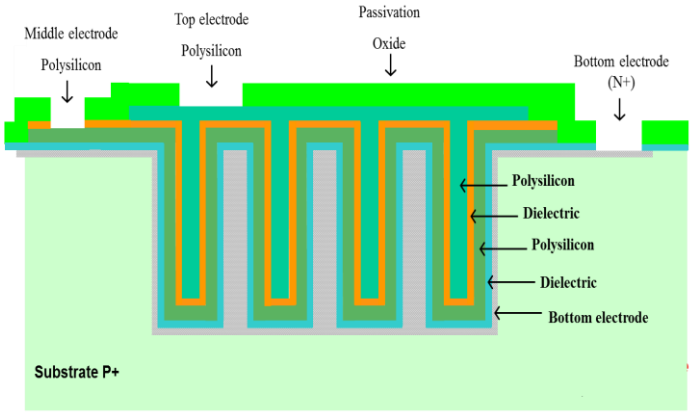

Figure 2: cross sectional view of the MIMIM architecture.

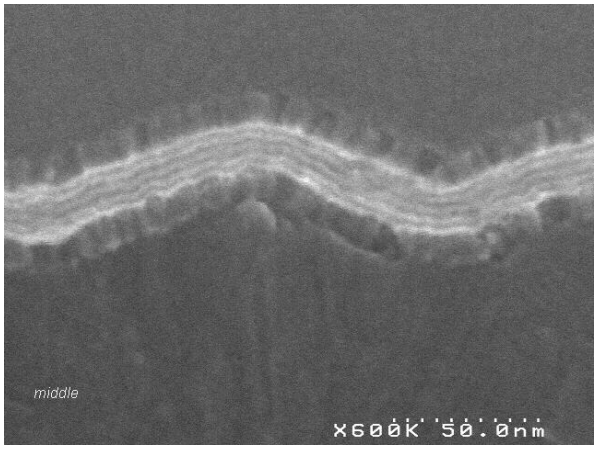

Figure 3: higher k-dielectric nanolaminates deposited in high aspect ratio 3D structures.

B. Lifetime

In constant-voltage tests the oxide is exposed to higher voltage (11.5, 12.5 and 13.5 v) than designed operating voltages (Fig. 4), and the time to breakdown is measured. To completely characterize dielectric life, TDDB tests are generally conducted to span a desired matrix of electric field and temperature values. The E-model is supported by published data and widely used down to 4nm, according to JEDEC standard (JP001.01 – May 2004).

The equation used to calculate the TTF is the following:

$$TTF = A_0 e^{Ea/kT} e^{-\gamma V}$$

With γ= field acceleration factor, Ea = activation energy , k=Boltzmann's constant.

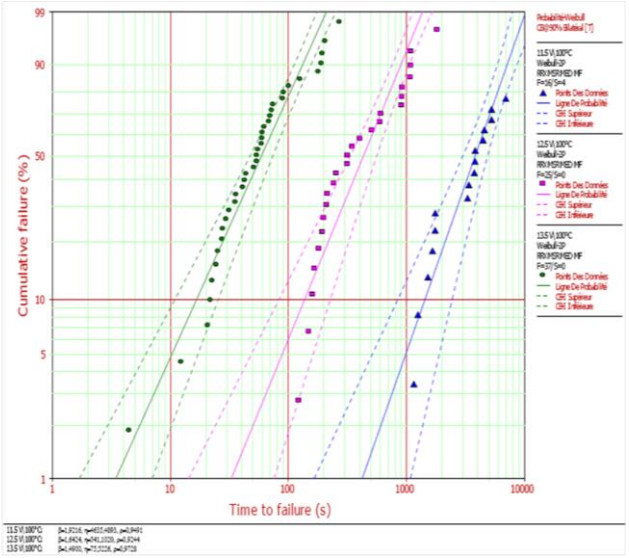

Figure 4: TTF when dielectric is exposed to 3 voltages: 11.5V, 12.5V, 13.5V

The extrapolation of the above data (Fig 4.) confirms the lifetime prediction of 10 years operating at 3.6V.

C. Key Differentiators

The key differentiators of this capacitor technology are the following:

- The capacitor density associated to the performances and the low profile capability with a thickness varying from 80µm down to 30µm.
- High temperature and voltage stability, the capacitance variation doesn't exceed 2% from room temperature to 250°C whereas the MLCC industry shows more than 60 % variation[3]
- High reliability with a FIT (Failure in Time) below 0.02 at room temperature and below 1 at 225°C.
- Ultra low leakage current: IPDIA dielectrics demonstrate a typical insulation resistance above 1 **ΩF** at 300°C whereas the class II dielectric insulation resistance drops significantly when the temperature exceeds 200°C [3]
- Extremely low ESL and customized ESR [6]
- 3D Silicon capacitors can be co-integrated with high Q factor inductors, Zener diodes for high efficiency ESD protection devices and Through Silicon Vias.

III. Examples of application

The TSV can be combined with the 3D high density Capacitors, Resistors and high Q inductors as described in Fig. 5. When combined with micro bump bonding and advanced flip chip technology, this technology enables a higher level of functional integration and performance in a smaller form factor [4]

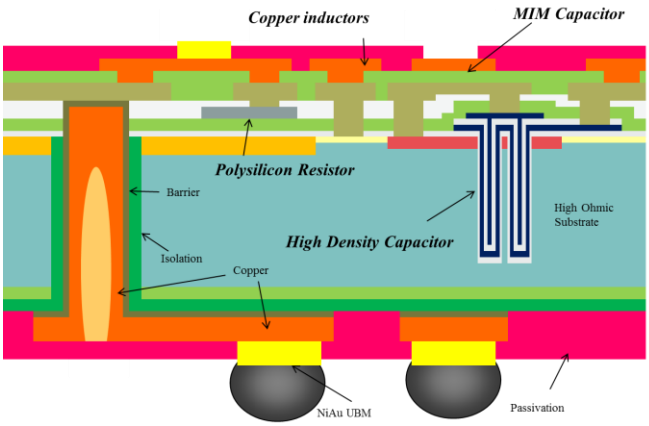

Figure 5: Silicon interposer with TSVs and High Density Capacitors, Polysilicon Resistors, MIM capacitor and Copper inductors .

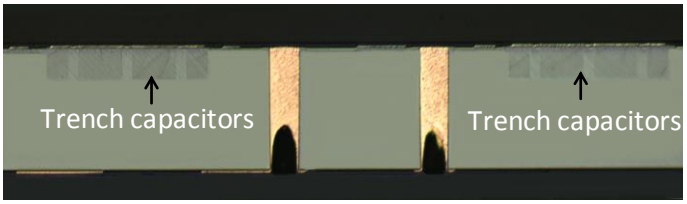

Figure 6: Cross sectional view of a silicon interposer with TSVs and High Density Capacitors (trench capacitors).

The TSV can be backside processed in pre-existing active CMOS wafers (Fig. 7). This solution, for example, brings indeed high value in the industry of advanced system-on-chip (SOC) probe cards, with technology leadership in both memory and SOC probe card markets. This solution addresses semiconductor test requirements and enhances the acceleration of the innovation in wafer test in position to meet the needs and roadmaps of logic and memory semiconductor device manufacturers.

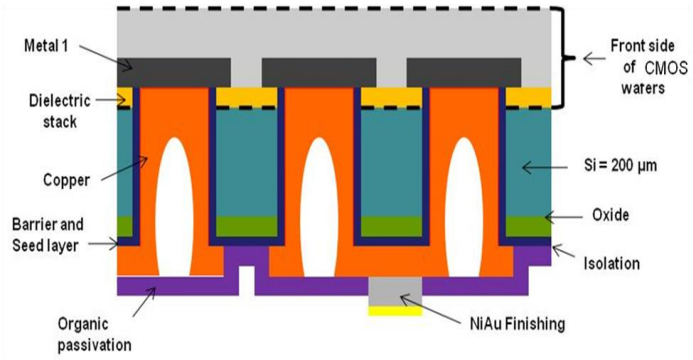

Figure 7: Drawing of TSVs on Actives

Table I: Key features of the basic TSV technology:

Item	Value
Die thickness	200µm
Via diameter	75µm
Via pitch	125µm
Keep out	15µm
Via density	64/mm²
Dielectric reliability	450v (V ramp)
Mechanical reliability (TMCL)	-40°C/+125°C 1000 cycles
Metal layers	Up to 3:AlSiCu or Cu
Isolation	Low T° oxide (<250°C)
Barrier layer	Ti/TiN
Via filling	Copper super filling by ECD
Passivation	Low K material (epoxy based)
Under Bump metallization	NiAu electroless

IV. Measurement Results and discussion

Electrical modeling of a TSV structure was carried out and the characterization was conducted at ambient temperature in a frequency range of 300 Khz up to 20Ghz. The TSV model was based on the physical structure of the TSV and was verified up to 20 GHz. The extracted RLC parameters reported in the table II show that the TSV structure can be used with good confidence in the DC to RF domains.

Table II: Equivalent Circuit Model Parameters of G-S-G TSV Structure.

Parameters	Rdc	L	Cox	Csi	G
Test structures	124 mΩ	35pH @10 GHz	From 3 to 1,25pF Tox=1,25um	From 100 to 45 fF	< 1mS up to 20 GHz

On top of these results, the insertion loss was remarkably low <0,5dB @ 20 GHz and the reflection to GND was also very good -12 dB with a good fit between simulation and measurements.

V. Design recommendation

High level of integration and high frequency (from 1 GHz to 20GHz) emphasizes the risk of interaction between the components. The degradation can manifest itself in several ways like for example interaction between the passive components through the common substrate, mutual inductance and capacitance between passives. Specific design rules were defined on the TSV pitch , the TSV keep out area and the GND vias insertion to prevent from these damaging effects. [5]

VI. Conclusion

Passive integration technologies coupled with 2,5D/3D-interposers bring differentiation and miniaturization. Main driver is the packaging integration density, with Integrated Passive Devices, Through Silicon Vias and external IC integration.

The TSV via last process developed by IPDIA can be co-integrated in a Silicon interposer with high value capacitors, resistors, RF MIM capacitors and copper inductors for RF applications .This TSV process can also be used on CMOS wafers.

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References

[1] Bunel, White paper Integrated Passive Devices Technology breakthrough by IPDIA France , “submitted for publication”.

[2] Gaborieau, Bunel and Murray ,3D passive integrated capacitors towards even higher integration, Device Packaging Conference 2009 , Phoenix , “submitted for publication”.

[3] Bunel , Lengignon ,Silicon Capacitors with extremely high stability and reliability ideal for high temperature applications, HITEC 2012 ,Albuquerque, "submitted for publication".

[4] Riou, Bailly, Bunel, Lenoir, Pommier, 3D TSV System in package (SIP) for aerospace applications, EMPC 2013 , Grenoble,"submitted for publication".

[5] Bunel , Tenailleau , Voiron, Brunet , Borel, TSV development, characterization and modeling for 2.5-D interposer applications , ECTC 2013 , Las Vegas , "submitted for publication".

[6] Lallemand, Voiron, Silicon interposers with integrated passive devices , an excellent alternative to discrete components , EMPC 2013, Grenoble,"submitted for publication".