

Silicon Based Integrated Capacitors: New Solutions for Combined Miniaturization and High Performance

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Abstract

The 3D Silicon technology of IPDiA is a disruptive capacitor and passive component technology for miniaturization adopted by the key players in the Medical domain for its very low leakage current, high stability and high reliability. It is also adopted by the Industrial market for its outstanding performance and reliability demonstrated in high temperature environment, up to 300°C. The high density Silicon capacitors with multiple metal-insulator-metal (MIM) layer stacks in 3D structures are reaching today 250nF/mm² in mass production and have been demonstrating densities of up to 1μF/mm², confirming the target of more than 4μF/mm² in the coming years. In this paper, the robustness of the IPDiA technology will be exposed, illustrated by reliability results obtained through innovative platforms and packaging configurations used in various fields like implantable medical devices, automotive electronics and down hole drilling equipment.

I. Introduction

The semi-conductor industry is now struggling with the increasing importance of the “More than Moore” trend , where added value to electronic devices is accommodated by incorporating functionalities .Given the advantages that IPDiA’s PICS (Passive Integration Connecting Substrate) technology has brought so far with integrate passive components such as high-Q inductors , resistors , accurate planar MIM capacitors and trench MOS capacitors with capacitance up to 250nF/mm² all in one piece of Silicon , providing a technology with outstanding performances , IPDiA will take benefits of its technological advance to address harsh environment products .

The PICS technology has been largely depicted in previous publications [1],[2],[3], showing very high aspect ratio 3D structures with amazing trench shapes and Oxide/nitride dielectric stacks [4]. The new generations called PICS4 and PICS5 still use high density 3D structures with ALD deposited high-k layers to reach respectively the 500nF/mm² and 1μF/mm² values .

Such improvements were obtained without any tradeoff with respect to lifetime, leakage or breakdown voltage. The robustness is key to success in the domains addressed by this technology: automotive, oil exploration and medical.

II. High Voltage and temperature applications

A. Automotive

Innovation in automotive electronics systems requires more power electronics with a demand for higher temperature driven by hybrid electrical vehicles and fuel cells vehicles whereas thermal management systems are not fitting with the extreme cost pressures. The number of sensors in vehicles is increasing and many of them like exhaust gas sensors, pressure or combustion sensors must operate in high-temperature environments. Most of the capacitors are limited to a maximum of 150°C whereas electronic devices require solutions operating at 175°C, with a trend to push the temperature envelope to 200°C, at high voltage and high current. Required features are very high reliability, low leakage current, good stability with voltage, time and humidity. IPDiA is addressing under-the-hood electronics and automotive sensors with its 3D Silicon Capacitor technology called PICS3HV offering miniaturized capacitors that withstand 200°C working at 16V.

The following chapters are evidencing the robustness of the technology through the test results on temperature, voltage, and thermal shock acceleration factor.

One of the primary limitations of these “high temperature products” at 200°C is the packaging because the glass transition temperature of common molding compounds is in the 180C to 200C range. The melting point of the solder pastes and the die surface have to be considered too..

Most of the tests have to be executed in a package according to the automotive rules .IPDiA selected the Cerdip package (Fig. 1) with Aluminum wire bonding on a 3μm Aluminum thick top die metallization for HTOL (High Temperature Operating Life) tests and Solder paste (Indalloy 95.0Pb5.0Sn Type 6) Soldering on board for TMCL tests (Fig. 2). Some tests such as TDDb (Time-Dependent Dielectric Breakdown) can be performed at die level (Fig. 3).

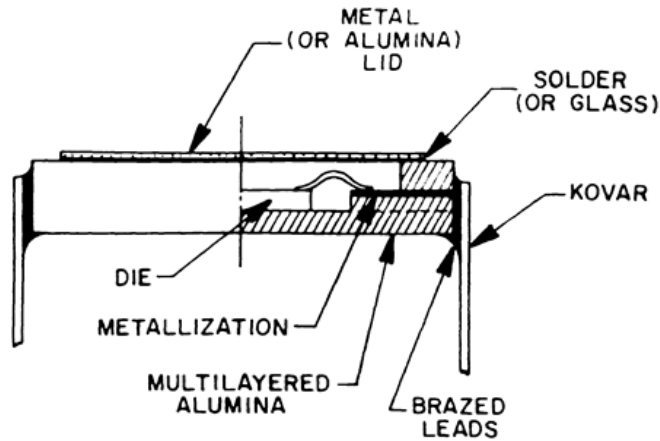


Figure 1: Cerdip package selected for the reliability tests

*Solder Paste with 95Pb/5Sn (Indalloy #171)
Liquidus at 312°C, Solidus at 308°C*

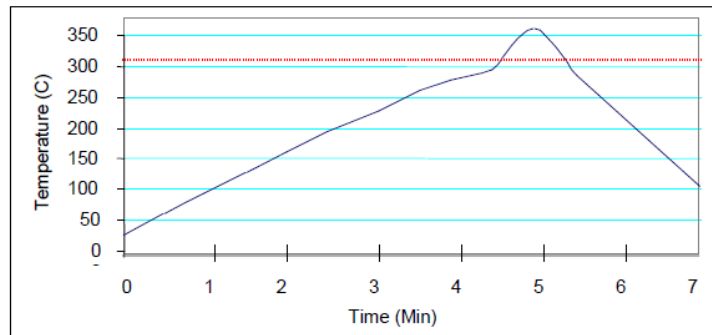


Figure 2: Solder paste reflow profile

1. Lifetime - Time to Failure at 200°C and 16V

The Time-Dependent Dielectric Breakdown (TDDB) measurements are used to model the intrinsic behavior of the capacitor dielectric under elevated temperature and strong electric field. The acceleration factors for temperature and electric field are used to extrapolate the capacitor lifetime under typical operating conditions. This Time-Dependent Dielectric Breakdown (TDDB) is a known failure mode in integrated circuits. Intrinsic breakdowns occur in oxides that are free of defects when the inherent, intrinsic tolerances of the dielectric material wear out. Wear out is accelerated under high voltage or high temperature conditions. In constant-voltage tests the oxide/nitride dielectric stacks were exposed to higher voltages (44, 41 and 38 v) than designed operating voltage (16v), and the time to breakdown was measured. To completely characterize dielectric life, TDDB tests were conducted to span a desired matrix of electric field and temperature values (200, 175 and 150°C). Raw data was statistically analyzed using a linearized Weibull plot to determine Time To Failure extrapolated down to 0.1% cumulative failures ($t_{0.1\%}$). The extrapolated $t_{0.1\%}$ is plotted against test voltage in Figure 3, with 60% Confidence Level (60% C.I.) intervals.

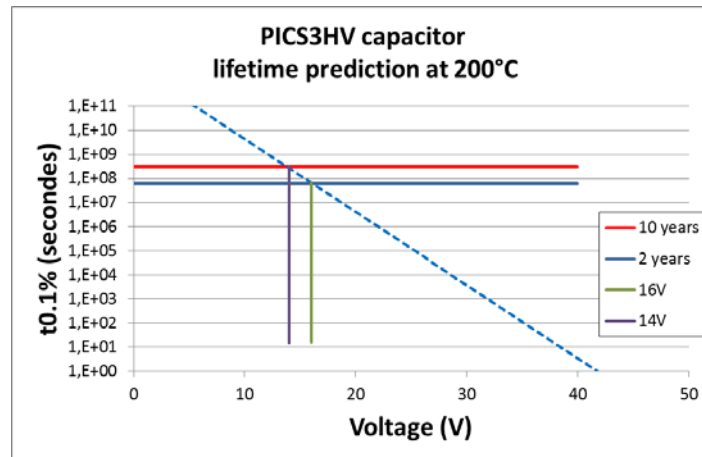


Figure 3: TDDDB measurements indicate that PICS3HV process has a 2 years lifetime @ 16V & 200°C and 10 years @ 14V & 200°C

As the temperature increases, the dissipation factor increases, and the breakdown strength decreases. Increasing the dielectric stack thickness to increase breakdown strength reduces the capacitance from 250nF/mm² (PICS3) down to 100nF/mm² (PICS3HV).

2. Stability over a large temperature range

Most of the capacitors commercially available for use at 220°C [6] show a significant change in capacitance above 150°C. In comparison, the PICS capacitor is extremely stable with a temperature coefficient of capacitance (TCC) below 80ppm from room temperature to 300°C (Fig.4).

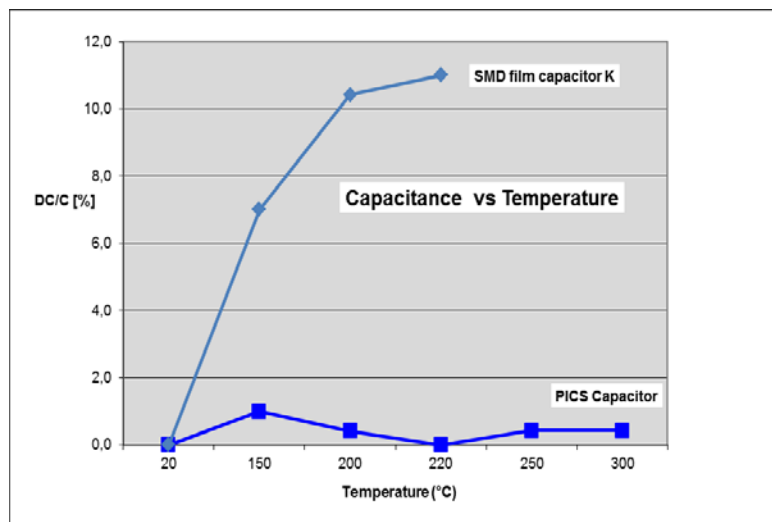


Figure 4: Capacitance stability of a PICS capacitor from room temperature to 300°C compared to a SMD film capacitor.

3. Leakage current

Increasing the temperature may conduct to the increase in leakage current.

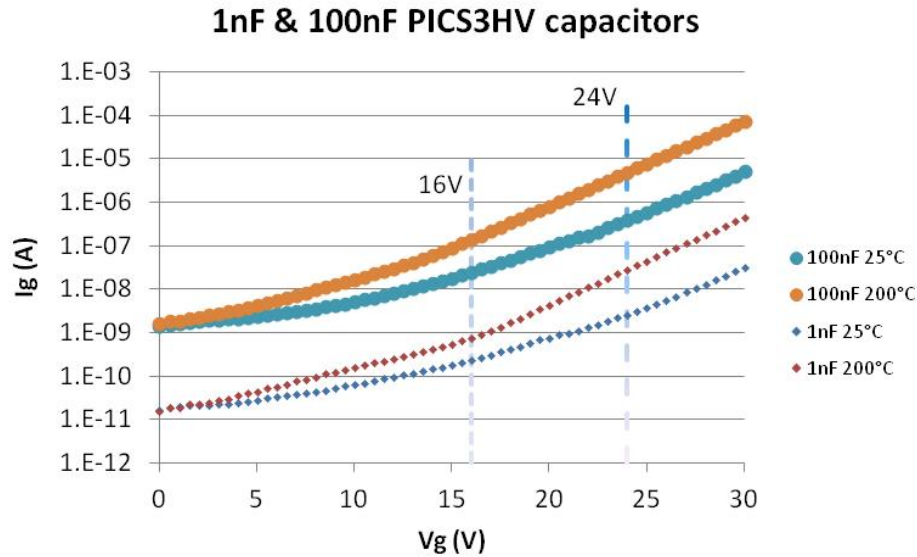


Figure 5: leakage current vs applied voltage and temperature measured on 2 IPDiA capacitors.

This graph shows that even if the leakage current is increasing when the temperature moves from room temperature to 200°C, the increase doesn't exceed one order of magnitude and the leakage measured at 200°C remains extremely low.

B. Down-hole drilling

The PICS3 technology is also addressing harsh environment conditions with temperature exceeding 250°C that require high reliability under mechanical shock and rapid changes in temperature. In order to verify this point, 50 cycles from +40°C to +250°C have been carried on parts soldered on a PCB. No failures have been observed after the electrical test.

	402		1206	
	33nF	100nF	100nF	1μF
Samples	135	130	112	144
nb of failures	0	0	0	0

Table 1: reliability results after 50cycles from +40°C to +250°C on boards.

Additional evaluations were based on extensive HTSL (High Temperature Storage Life) tests at 150°C through 4000h and at 250°C (Table 2) through 1000h without any parametric failures .These results demonstrate the robustness of the technology.

PICS3HV30 Finishing: TiCu (200/400nm)CuNiAu(3/2/1μm)		
	Duration	Defects
250°C	1000h (run1)	0/900
	1000h(run2)	0/900

Table 2: reliability results after 1000hrs at 250°C

C. Medical

Required features in Medical are very high reliability, low leakage current (high insulation resistance), small dimensions, good stability with voltage, temperature and time, and high peak withstanding voltage.

Reliability evaluations were performed on innovative platforms and packaging configuration depicted on figure 6, low profile [5] (130 μ m) stacked dies at 2 times V rate , 150°C and 1000 hours .

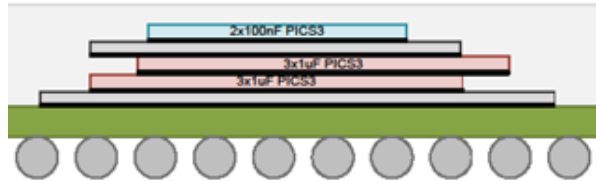


Figure 6: stacking of

multiple IPDiA dies

No shift was observed on
no failure on the capacitor leakage after 1000hrs.

the capacitance (Fig .7),

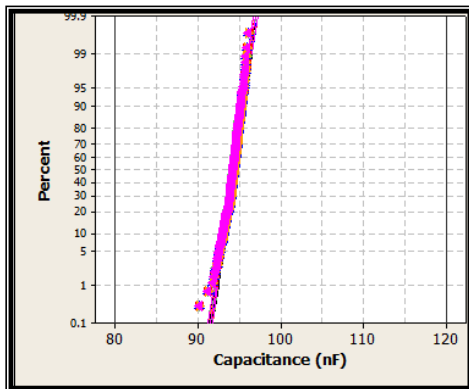


Figure 7: capacitance after 1000hrs
at 2*V Rate , 150°C

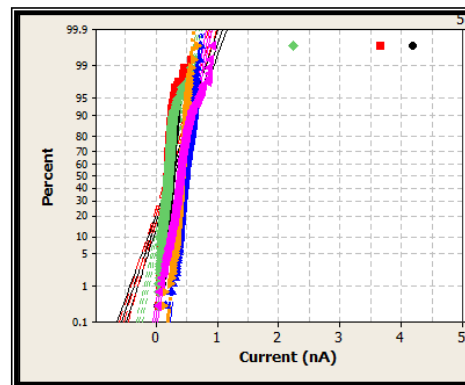


Figure 8 : Capacitor leakage after 1000hrs
at 2*V Rate , 150°C

These 2 graphs show that the capacitors can withstand 2X the rated voltage for more than 1000 hrs without failures occurring

III. Conclusion

IPDiA Capacitors are used for their outstanding performances at temperatures up to 250°C .In this paper some results (lifetime, stability, leakage, thermo mechanical), were depicted in order to prove that they are reliable for long term service. These results indicate that the IPDiA Silicon Capacitor offers great possibilities in applications such as automotive, down-hole drilling and medical.

IV. References

- [1] F. Murray 'Silicon Based System-in-Package: a passive integration technology combined with advanced packaging and system based design tools to allow a breakthrough in miniaturization', BCTM (2005).

- [2] F. Murray, F.LeCornec, S. Bardy, C. Bunel, Jan F.C. Verhoeven, F.C.M. van den Heuvel, J.H. Klootwijk, F. Roozeboom, 'Silicon Based System-in-Package : a new technology platform supported by very high quality passives and system level design tools', IEEE- SiRF2007
- [3] C.Bunel, J-R. Tenailleau,F.Voiron, S. Borel, A.Lefevre , "Integrated Passive devices and TSV , a disruptive technology for miniaturization " 46th Symposium *IMAPS* ,Orlando, 2013.
- [4] F.Lallemant, F.Voiron ,Silicon interposers with integrated passive devices, an excellent alternative to discrete components" EMPC 2013, Grenoble.
- [5] C.Bunel, S. Borel, M. Pommier and S. Jacqueline, "Low Profile Integrated Passive Devices with 3D High Density Capacitors," in *ESTC*, Amsterdam, 2012.
- [6] L.Caliari, et al."KEMET film capacitors for high temperature, high voltage and high current *CARTS*;Houston,2013