Silicon Based System-in-Package : a passive integration technology combined with advanced packaging and system based design tools to allow a breakthrough in miniaturization

F. Murray

Philips Semiconductors, 2, rue de la Girafe PO Box 5120, 14079 Caen, France
e-mail: franck.murray@philips.com

Abstract **— The very large development of home and domestic electronic appliances as well as portable device has led the microelectronics industry to evolve in two complimentary directions: "More Moore" with the continuous race towards extremely small dimensions hence the development of SoCs (System on Chip) and more recently a new direction that we could name "More than Moore" with the integration of devices that were laying outside the chips and thus the creation of SiPs (System in Package). Even though one can oppose SoCs to SiPs, one of the intentions of this paper is to demonstrate that these two approaches are not in competition one with the other. We will show some examples of systems that integrate several SoCs. The technology presented is called Silicon Based System in Package. This new technology is based upon the integration of passive devices into Silicon. The four critical elements of this technology will be discussed in detail: passive integration, advanced packaging, new IC design development tools, and innovative testing..**

Index Terms **— Passive circuits, System analysis and design, Reliability, Packaging, Interconnections, Energy management, Integrated circuit design.**

I. INTRODUCTION : FROM "MORE MOORE" TO "MORE THAN MOORE"

Looking for the lowest cost per digital function has led the Semiconductors industry to innovate in the field of miniaturization at the individual device level, like decreasing the length of individual transistors to less than 20 nm and the surface of memory cells to less than 1µm². Since these technologies are using more and more complex process steps, materials and lithography techniques, the initial investment costs to create a new product have increased tremendously. This leads to more and more generic and programmable chips. These products are usually called Systems on Chip (SoC). Whereas this approach seems to be economically efficient when dealing with data processors, this standardization or even commoditization does not allow any product differentiation except through their embedded software or through their operating software. In addition, this miniaturization requires the use of more and more passive components such as inductors and capacitors that currently take up most of the printed circuit board area in consumer products for instance [1]. As these passive devices do not scale following the Moore's law, their integration into the SoCs turn into a non cost-effective solution. Separate integration of those passive devices is an interesting alternative: it allows the optimization of both the passive and active devices on different technology platforms and the exploitation of this separate platform to integrate technologies that cannot be properly combined with advanced CMOS. For example, integration of MEMS or sensors becomes easier and cheaper [2]. One of the answers that we have brought to this paradigm is heterogeneous integration of multiple dies in a single package, also called System in Package (SiP). This multiple die integration is not new in itself but we have helped create a breakthrough thanks to efficient die to die interconnection processes as well as system level design that allow the integration of complex functions into standard miniature packages. This breakthrough was made possible thanks to the parallel development of the four following technology elements: passive integration, advanced packaging, advanced testing and system level multiple technology design. This is shown on Figure 1. The deployment of this program is what we have named "More than Moore".

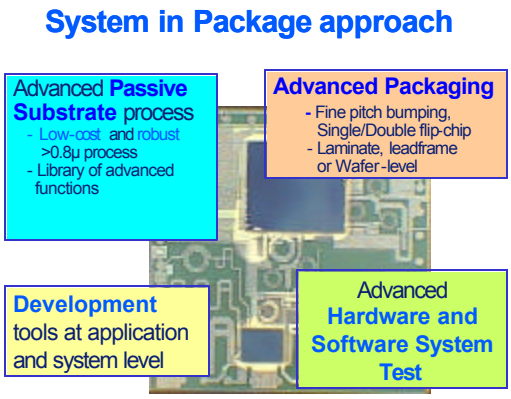


Fig. 1: The four elements of the Philips silicon based SiP approach

II. SIP VERSUS SOC

Many articles try to determine which solution is going to be the best between the SiP and SoC approaches. We prefer to present these two approaches as complementary ones. It is now clear that the SoC approach is the best suited one when we want to lower the cost per digital function. This is true for high volume products like microprocessors, standardized products like video or sound codecs, etc. The key challenge here is to manage the increased complexity caused by the wide variety of applications and emerging technical solutions. In addition, there is the innovator's dilemma: how to balance investments in a new application based on unproven technology against the next generation of a predictable technology? When we want to integrate more flexible responses to more specialized products and when we look at the highest value per total system, then the SiP approach seems to be the most efficient: it allows the integration of several either already existing and/or dedicated dies together to create a new function without having to pay for long product development times and very expensive masksets. In particular several SoCs can be integrated in a SiP to create a new system. Figure 2 shows the example of recent mobile phone platforms where the both kinds of products are present.

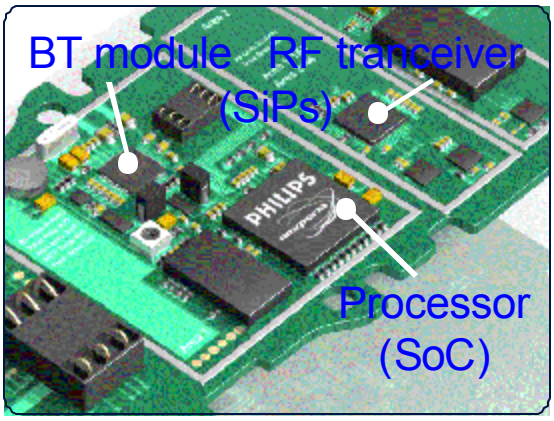


Fig. 2: mother board of a mobile phone with several SiPs (RF transmission/reception and Bluetooth communication module) and a SoC (Baseband processor)

Figure 3 is another example where three existing SoCs using advanced CMOS have been combined in a single package to create a breakthrough in the size of a Set Top Box by creating a One Chip Set Top Box. In summary, we think that, at least during the next five to ten years, the two approaches will be complementary.

As indicated in the introduction, this approach is based upon four balanced pillars that were developed in parallel.

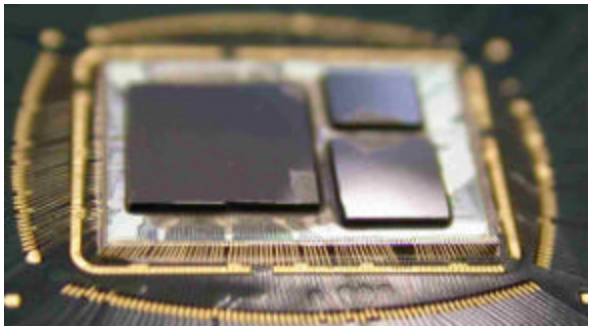


Fig. 3: Picture of a single package Set Top Box including three active dies from different technologies (CMOS090, CMOS18 and QUBiC4+ BiCMOS) and a passive die

III. PASSIVE INTEGRATION

Passive integration is the first piece of the puzzle. It is very interesting in terms of miniaturization, but also in terms of performance. Very efficient and high quality factor capacitors and inductors have been integrated, allowing the creation of complete modules including active devices, filters, and decoupling capacitors. Some examples will be shown, in particular in the field of connectivity and cellular phones.

The solution proposed is the use of a substrate or interconnection die carrying the passive devices. The technology use for the making of this die is called PICS (for Passive Integration Connecting Substrate).

A. Capacitors

High-density MOS capacitors with 1-1000 nF capacitance, and values as high as 25-200 nF/mm^2 specific capacitance have been integrated in macroporous Si-wafers containing over 1 billion macropores [3-5].

To reach these high values, we have made the choice to use the third dimension inside the silicon. The structure of the integrated capacitors is shown in Figure 4.

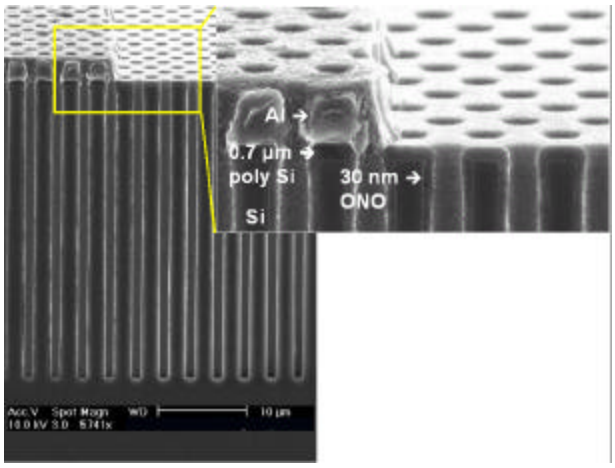


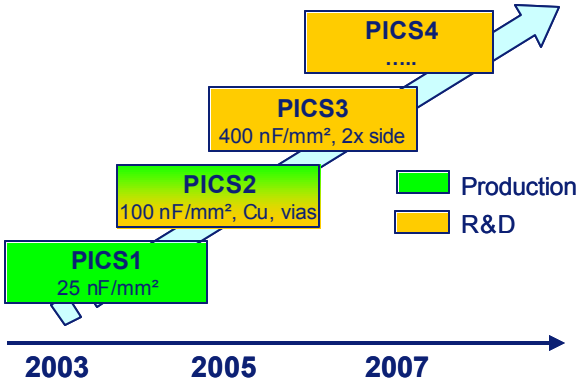
Fig. 4: Structure of 3D macro-pores in PICS capacitors

The use of the third dimension allows us to reach these values with dielectric layers manufactured using conventional front-end techniques like CVD and thermal processing, hence the very high quality of these layers. This was preferred to high k materials made with lower temperature processes leading to higher defect densities. These high k materials are also showing today some significantly lower quality factors than for MOS structures because of dielectric losses and piezoelectric relaxation phenomena inside the material.

Superior decoupling performances in the GHz range have been shown. Typically a series resistance of less than 100 mO and a parasitic inductance of less than 25 pH were found for capacitors over 10 nF. This novel concept can be an important step forward in improving the stability of power-amplifier modules by replacing conventional SMD technology.

Figure 5 shows the various nodes in the passive integration roadmap that we have built.

Fig. 5: Silicon based Passive Integration Roadmap



The generations with capacitor densities of up to 100 nF/mm² will be using "conventional" materials and processes. Values of up to 200 nF/mm² have been reached with these materials, thanks to the optimization of the developed surface. The next steps in the roadmap will call for new materials such as high-k dielectric layers and new process steps, in combination with 3D structures.

B. Inductors and Resistors

Resistors are simply made by using the poly-Si top electrode of the capacitors. This well controlled in-situ doped layer is well suited to the resistors values needed in the sub functions that we need to integrate.

Inductors are made by using the two metal layers also used for interconnects. Single turn coils are mainly made out of the thick (up to 5 µm) second metal and multiturn coils are made out of the two layers for crossover. All standard coil designs are compatible with this process.

Q factors of up to 40 (@ 1 GHz) have been demonstrated for several nH inductor values.

The combination of these three types of passives make possible the realization of multiple passive functions such as Baluns, PLL loop filters, decoupling capacitors, RC and low pass filters…All these functions, combined with one or several active dies have demonstrated their interest, not only in RF applications but also in many other applications where miniaturization counts. Figure 3 and Figure 7 show some examples of products that are manufactured today in large quantities. Several examples have also been recently announced or published.

C. Modeling

Bearing in mind that from the very beginning of this SiP R&D activity we had planned to develop these passive technologies together with IC-like design tools, we have made the choice to develop models that were compatible with this kind of design flow. Whereas models for capacitors and resistors are quite simple, we have used also compact and predictive models associated with scalable inductor layouts to simplify the design and make the simulations more accurate [6]. The combination of this approach with the use of IC-like design tools has led to the creation of passive devices libraries with many kinds of scalable devices (p-cells).

IV. Advanced Packaging and Size Reduction

The second element is advanced packaging. New technologies, such as the assembly of Silicon chips onto other Silicon chips, also referred to as "double flip chip" has been used [7-8]. This has been made possible thanks to the combination of the most advanced microbumping

and die placement techniques. Examples are shown in Figure 3 and Figure 6-7 where cross sections of products and top views are presented.

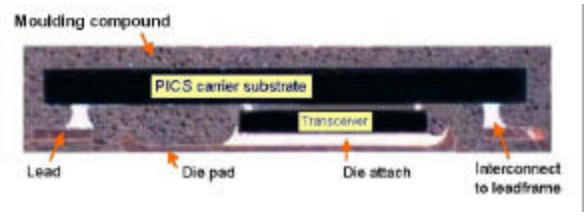
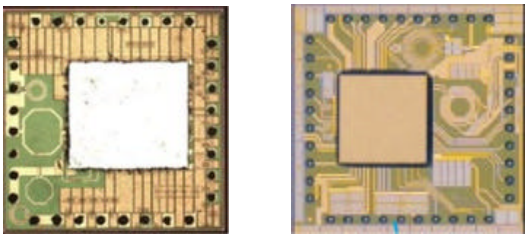


Fig. 6: Cross section of a fully integrated radio module in a molded leadframe



(a) (b)

Fig. 7: Examples of sbSiP products : (a) Bluetooth communication module, (b) GSM transceiver,

In addition to a tremendous reduction of size (up to a factor of 10 as shown on some examples in Table I) these techniques have also brought a better repeatability of system performance, thanks to a well-controlled placement of passive functions and to the possibility to tune the passive components to the real needed value.

TABLE I
EXAMPLES OF SIZE REDUCTION FACTORS OR ENABLING POSSIBILITIES OFFERED BY THE SBSIP TECHNOLOGY

Application	**Size of the application** (sizes in mm²)		
	without	with passive integration	Reduction factor
GSM transceiver	100	35	3x
Bluetooth module	-	36	enabling
DECT radio module	400	42	10x
TV on mobile	-	64	enabling
Set top Box	250	64	4x
NFC solution	70	35	2x

Same as for passive integration, we have built a SiP packaging roadmap shown in Figure 8.

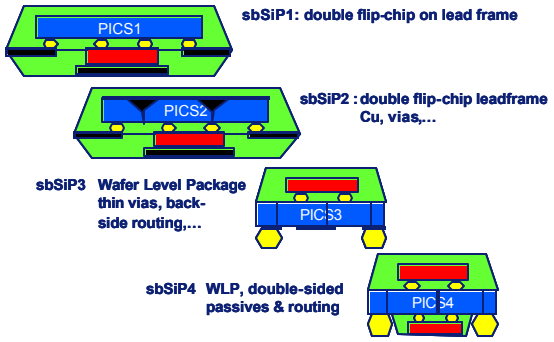


Fig. 8: Packaging roadmap

V. SYSTEM DESIGN AND SIMULATION

The third element has been the development of design tools that allow a seamless system design for engineers used to IC design tools and flows.

Our Design Environment allows co-design of chips in multiple technologies and their integration in a single system. The first level is at the individual passive device level: like in the usual IC technologies, compact models, elementary libraries and libraries of more complex functions have been developed. The second level is at physical level: packaging and interconnections between the dies are part of the design flow. The third level deals with the electromagnetic, thermal and mechanical behaviors of the different dies inside the package. An example of thermal-mechanical simulation is shown in figure 9.

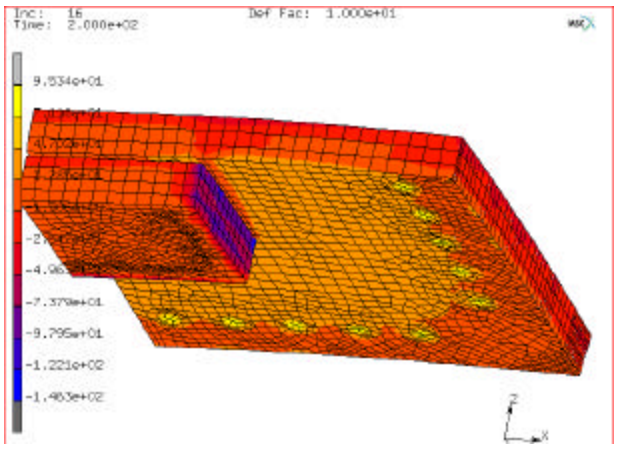


Fig. 9: Examples of a thermo-mechanical simulation (representation of z axis shear stress) to identify the critical areas in the products design

The complete approach is called Multi Technology Design Environment. It uses dynamic links between the various product databases and allows software based verification and error checks.

Finally, this IC-like Design Environment has contributed a lot to the adoption of the technology.

V. INNOVATIVE TESTING SOLUTIONS

Testing is the fourth element and is one of the economical enablers of the technology. The key words are: "known good die", RF test, system test, etc. Some innovative RF probing and full-on wafer subsystem testing has been developed. Even though efficient test is not vital for the technical feasibility of this system integration, it becomes very quickly one of the most important enablers, especially when we deal with very high volumes of production.

VI. COMPETITIVE ANALYSIS

The field of SiP has shown some very intense activity in the last few years. As the technologies are not yet standardized and the solutions less unified than the ones we see in the Moore's law race, several approaches compete with each other. Some have started from packaging and assembly technologies. They, of course, use the most advanced individual packaging techniques but do not bring the link to system level design. Some other approaches come from the discrete and passive device side. These bring some interesting technical solutions but again, no real link to a system level approach. Some examples will be shown during the presentation.

VII. CONCLUSION

In this paper, we have presented our approach to the integration of multiple technology dies inside a single package to create miniaturized integrated systems. This technology, called Silicon Based System in Package has demonstrated its potentialities thanks to the successful launch of several products representing a breakthrough in size and performance. The innovation relies not only in the individual technologies used, but rather in the parallel development and links that we have created between these elements to build this integral approach.

ACKNOWLEDGEMENT

These R&D activities are supported by the French Public Authorities as well as by the European Community through Eureka Program.

REFERENCES

[1] P. Philippe, and A. Oruk, "A highly miniaturized 2.4 GHz Bluetooth radio utilizing an advanced System-in-Package technology," *European Microwave Week.,* Amsterdam, October 2004.

[2] J.T.M. van Beek, M. van Delden, A. van Dijken, P. van Eerd, A.B.M. Jansman, A.L.A.M. Kemmeren, T.G.S.M. Rijks, P.G. Steeneken, J. den Toonder, M.J.E. Ulenaers, A. den Dekker, P. Lok, N. Pulsford, F. van Straten, L. van Teeffelen, J. de Coster and R. Puers, "*High-Q integrated passives and RF-MEMS on silicon*", *Mater. Res. Soc. Symp. Proc.* **783** (2003) pp. 97-108

[3] F. Roozeboom, R. Elfrink, T.G.S.M. Rijks, J. Verhoeven, A. Kemmeren and J. van den Meerakker, "*High-Density, Low-Loss MOS Capacitors for Integrated RF Decoupling*", *Int. J. Microcircuits and Electronic Packaging*, **24** (3) (2001) pp. 182-196, and refs. therein.

[4] F. Roozeboom, A. Kemmeren, J. Verhoeven, F. van den Heuvel, H. Kretschman and T. Fric, "*High-Density, Low-loss MOS Decoupling Capacitors integrated in a GSM Power Amplifier*", *Mat. Res. Soc. Symp. Proc*. **783** (2003) pp. 157-162.

[5] F. Roozeboom, A. Kammeren, J. Veroeven, F van der Heuvel, J. Klootwijk, H. Kretschmann, T. Fric, E van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, *"More than Moore: Towards Passive and Si Based System-in-Package integration*", *ISB Micro Conference,* Florianopolis, Brazil, Sept 4-7, 2005, Invited Paper

[6] L. Tiemeijer, R Havens, R. de Kort, Y. Bouttement, P. Deixler and M. Ryczek, "*Predictive spiral inductor compact model for frequency and time domain", IEDM,* Washington DC, USA, Dec 8-10, 2003

[7] D. Chevrie, C. Bunel, Y. Bouttement, S. Bardy, L. Hamelin, E. van Grunsven, M. Burghoorn and M. de Samber, "*A Silicon-based System in Package Technology*", IMAPS Conf., Bruges, Belgium, June 12-15, 2005.

[8] P. Deixler, T. Letavic, T. Madhadejkul, Y. Bouttement, R. Brock, P.C. Tan, V. Saikumar, A. Rodriguez, R. Colclaser, P. Kellowan, H. Sun, N. Bell, A. Yao, R. van Langevelde, T. Vanhoucke, W.D. van Noort, G.A.M. Hurkx, D. Crespo, C. Biard, S. Bardy and J.W. Slotboom, "*A cost-effective Power-on-Board BiCMOS Manufacturing Technology with Elite Passive Enhancements Optimized for 'Silicon-based RF System-in-Package Environment*", 2005 IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM 2005), Santa Barbara (USA), Oct. 10-11, 2005