Assembly of Broadband Silicon Capacitors: Guidelines for improved Impedance Matching

Rev.1.0

Introduction

This application note provides guidelines to design transmission lines in order to obtain the best performances from Murata Broadband Silicon Capacitors. These recommendations are applicable to: XBSC, UBSC, BBSC and ULSC ranges in 0201 (800µm x 600µm), 0201M (600µm x 300µm) and 0402 (1200µm x 700µm) sizes.

Three types of transmission lines are presented, for single-ended and differential modes:

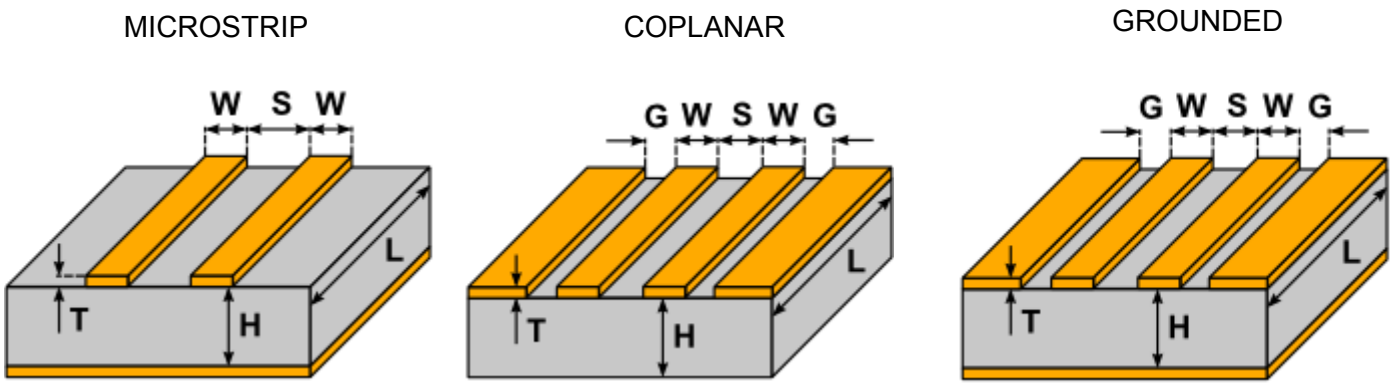


Figure 1: Differential Transmission Lines Structures

The application note details some examples of substrate materials, line width and gaps in order to achieve a 100Ω differential characteristic impedance or a 50Ω single-ended impedance.

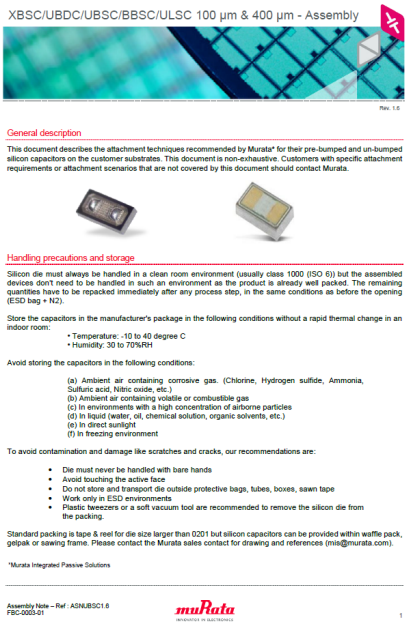
The dimensions given in this application note are for information only. They are to be considered as a starting point for the PCB layout optimization. Full 3D electromagnetic simulations are needed. Please contact our sales representative for 3D HFSS models of our Silicon Capacitors

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Please also refer to the following application notes regarding assembly and electromagnetic models:

- "Assembly Note_XBSC-UBDC-UBSC-BBSC-ULSC 100 µm & 400 µm - NiAu finishing Assembly by soldering"
- "MIS broadband silicon capacitor electromagnetic simulation setup"



XBSC/UBDC/UBSC/BBSC/ULSC 100 µm & 400 µm - Assembly

Rev. 1.6

General description

This document describes the attachment techniques recommended by Murata* for their pre-bumped and un-bumped silicon capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact Murata.

Handling precautions and storage

Silicon die must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices don't need to be handled in such an environment as the product is already well packed. The remaining quantities have to be repacked immediately after any process step, in the same conditions as before the opening (ESD bag + N2).

Store the capacitors in the manufacturer's package in the following conditions without a rapid thermal change in an indoor room:

- Temperature: -10 to 40 degree C
- Humidity: 30 to 70%RH

Avoid storing the capacitors in the following conditions:

(a) Ambient air containing corrosive gas. (Chlorine, Hydrogen sulfide, Ammonia, Sulfuric acid, Nitric oxide, etc.)
(b) Ambient air containing volatile or combustible gas
(c) In environments with a high concentration of airborne particles
(d) In liquid (water, oil, chemical solution, organic solvents, etc.)
(e) In direct sunlight
(f) In freezing environment

To avoid contamination and damage like scratches and cracks, our recommendations are:

- Die must never be handled with bare hands
- Avoid touching the active face
- Do not store and transport die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD environments
- Plastic tweezers or a soft vacuum tool are recommended to remove the silicon die from the packing.

Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided within waffle pack, gelpak or sawing frame. Please contact the Murata sales contact for drawing and references (mis@murata.com).

*Murata Integrated Passive Solutions

Assembly Note – Ref : ASNUBSC1.6
FBC-0003-01

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Design Guidelines

Line Width:

The key point is to match the width of the transmission lines on the PCB to the width of the capacitors while keeping the impedance value. The capacitors in series should be considered as a part of the transmission line, targeting a thru.

In the drawing below, the “active” (or “conductive”) part (inner electrode) of the Silicon Capacitor is represented by the dotted line. The capacitor package is the bold black rectangle. The pads are the orange rectangles.

The optimum line width on the PCB is the width of the “active” part, but it is most of the times difficult to match it because of the constraints of the assembly and of the substrate’s characteristics. In some cases the transmission line width can be smaller than WMIN (the pad width) and it might be necessary to use tapers. The design of the tapers is not in the scope of this application note. However, be aware that, in the case of microstrip transmission lines with tapers, there will be an impedance drop at pad level. Coplanar waveguides may give better results.

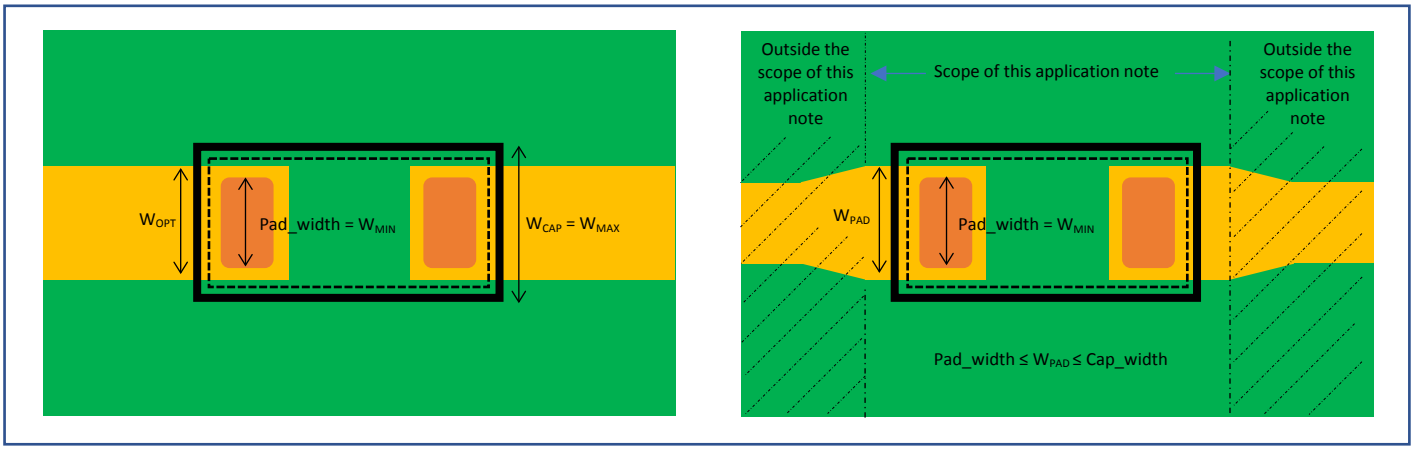


Figure 2: Transmission Line and Capacitor Width

The following table shows the optimum and acceptable min/max line width for each capacitor size:

Capacitor case	Cap Dimensions	Pad dimensions	Wmin	Wmax	Wopt
0201M	600x300	100x150	150	300	200~250
0201	800x600	150x400	400	600	500
0402	1200x700	300x500	500	700	600

Table 1: Line Width (µm)

Keep-Outs:

There are a few important things to consider in order to obtain good RF performances of your system. One is the minimum keep-out distance between two Silicon Capacitors side-by-side:

Capacitor case	Distance (µm)
0201M	100
0201	100
0402	100

Table 2: Keep-Outs

These distances are also depending upon the capability of the assembly tools.

Another important parameter is the distance between the capacitor's edge and the ground plane, in the cases of coplanar and grounded coplanar waveguides.

If the ground plane is too close from the capacitor's edge, there is a high risk of impedance mismatch that can degrade the Return Loss of the transmission line. There is also a risk that the capacitor touches the ground plane if the capacitor is tilted, which would lead to a greater degradation of the performances.

Again, 3D EM simulations are needed to ensure the best RF performances.

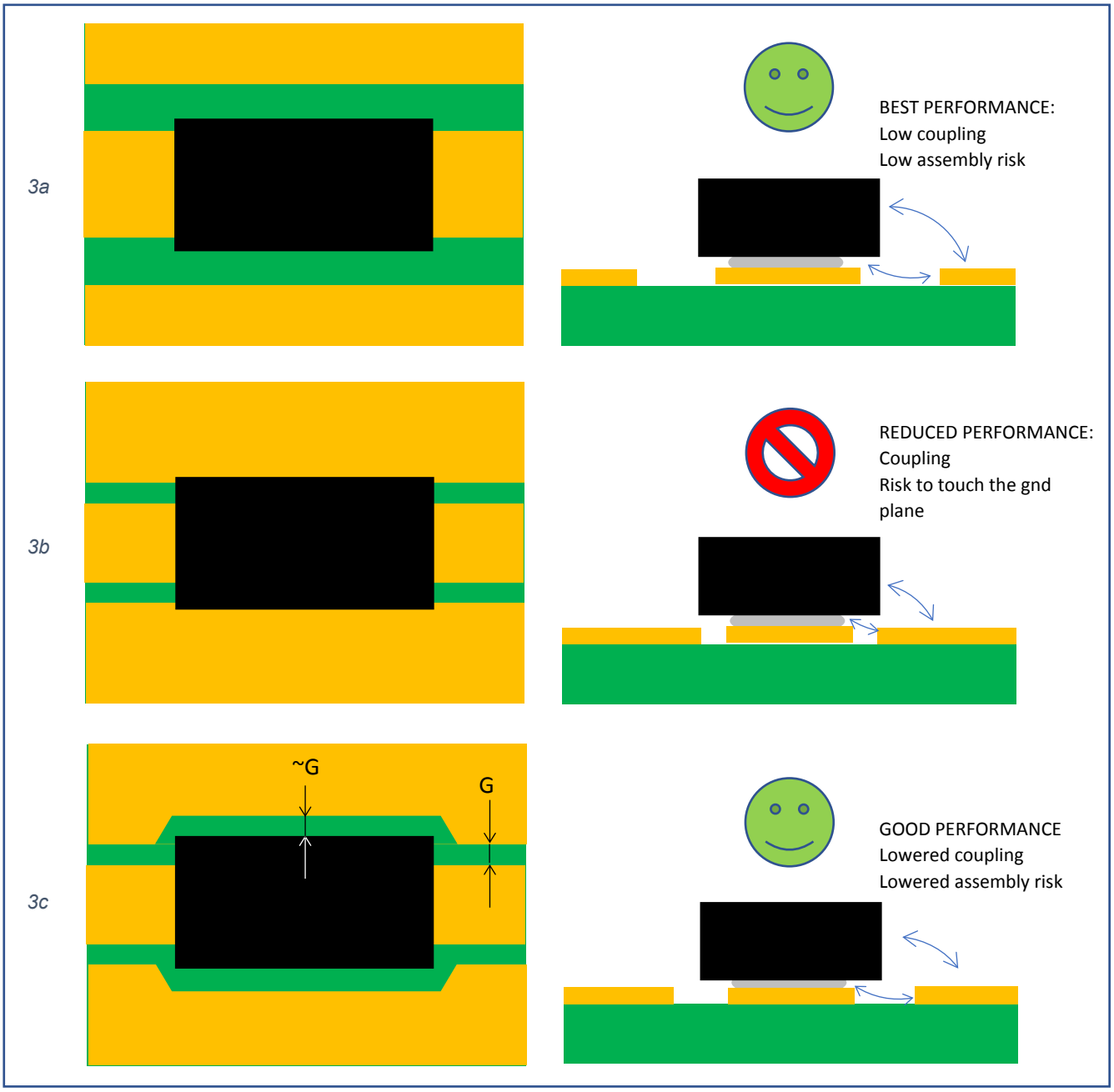


Figure 3: Ground Keep-Outs

In Figure 3c, the shape of the ground plane around the capacitor has two effects: it avoids coupling and touching risks but it can also help to ensure a good matching when there is an important difference between the line width and the capacitor width.

Basic guidelines to follow in order to design coplanar transmission lines such as shown in Figure 3a:

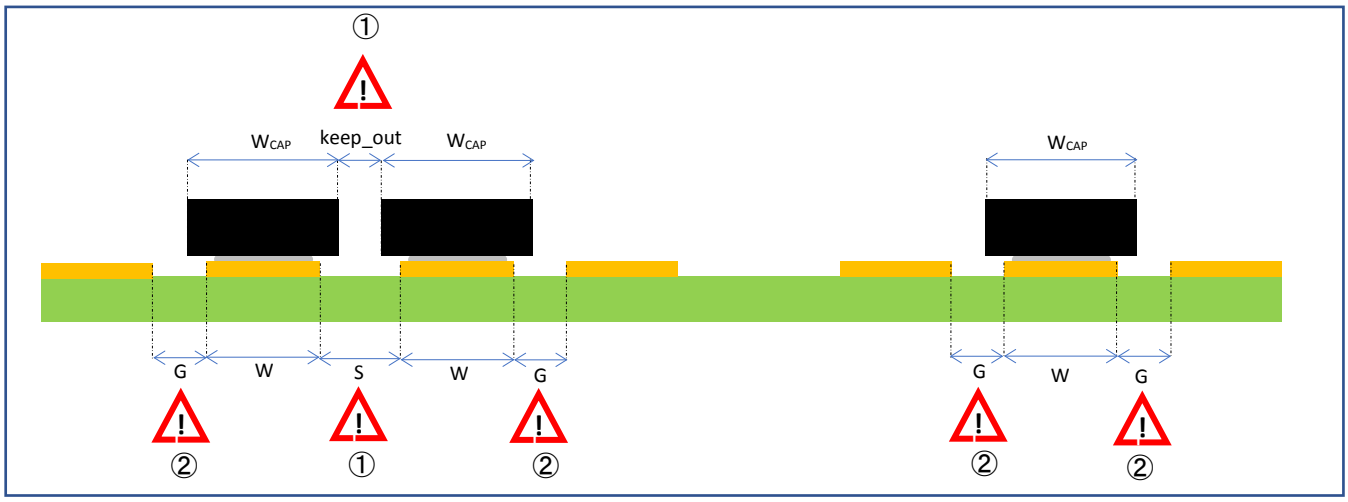


Figure 4 – Basic Guidelines to ensure proper Keep-Out Distances

① : W + S ≥ WCAP + keep_out (see Table 1 & Table 2)
② : W/2 + G > WCAP/2 + ~20µm (see Table 1)

Vias:

Last important consideration is the number and location of the vias between inner and top gnd planes. Their number and location will have a major impact on performances, and the risk to have resonances is quite high if the design is not properly done.
Again, 3D EM simulations are a needed to ensure the best RF performances.

Design examples for 100Ω differential lines

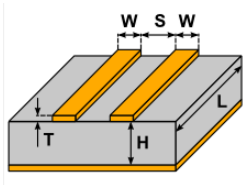
Here is a selection of substrates that are widely used for RF designs, proposing various dielectric constants and thicknesses. Using these parameters, the width and gaps were computed in order to obtain a 100Ω differential impedance.

The εr stated in the following tables are given by the manufacturers. “design” εr has been chosen wherever available (Rogers substrates).

There is no soldermask and no underfill.

0201M (600µm x 300µm x 100µm) capacitor size:

Basic design rule to follow:
W + S ≥ 400µm

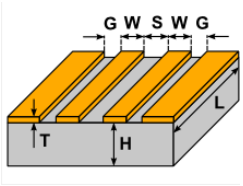


Substrate	Manufacturer	Er	H	T	W	S
RO4003C	Rogers	3.55	101	18	202	250
MEGTRON R-G545L	Panasonic	3.5	125	25	260	200
HS100(D)	Hitachi	3.62	136	14	250	200
RO4350D	Rogers	3.66	101	18	200	260
MEGTRON R-G525	Panasonic	4.5	100	25	170	280
Taconic TLY-5A	Taconic	2.17	130	18	300	100

Table 1 - Examples of Dimensions for 0201M Silicon Capacitors: Microstrip Waveguide (µm)

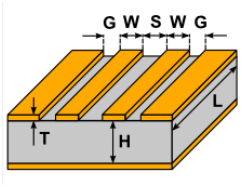
Basic design rules to follow:

1) W + S ≥ 400µm
2) W/2 + G > 170µm



Substrate	Manufacturer	Er	H	T	W	S	G
RO4003C	Rogers	3.55	101	18	280	150	80
MEGTRON R-G545L	Panasonic	3.5	125	25	250	170	85
HS100(D)	Hitachi	3.62	136	14	280	150	80
RO4350D	Rogers	3.66	101	18	280	150	85
MEGTRON R-G525	Panasonic	4.5	100	10	270	155	90
Taconic TLY-5A	Taconic	2.17	130	18	280	150	50

Table 2 - Examples of Dimensions for 0201M Silicon Capacitors: Coplanar Waveguide (µm)

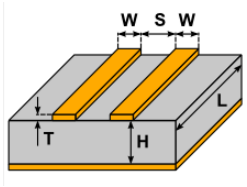


Substrate	Manufacturer	Er	H	T	W	S	G
RO4003C	Rogers	3.55	101	18	190	260	190
MEGTRON R-G545L	Panasonic	3.5	125	25	210	265	130
HS100(D)	Hitachi	3.62	136	14	225	195	180
RO4350D	Rogers	3.66	101	18	180	220	200
MEGTRON R-G525	Panasonic	4.5	100	10	160	240	180
Taconic TLY-5A	Taconic	2.17	130	18	270	150	80

Table 3 - Example of Dimensions for 0201M Silicon Capacitors: Grounded Coplanar Waveguide (µm)

<u>0201 (800µm x 600µm x 100µm) capacitor size:</u>

Basic design rules to follow:
W + S ≥ 700µm



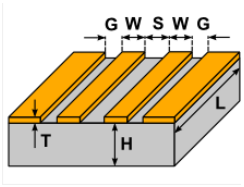
Substrate	Manufacturer	Er	H	T	W	S
RO4003C	Rogers	3.55	2x101	*25*	400	450
MEGTRON R-G545L	Panasonic	3.5	200	*25*	400	450
HS100(D)	Hitachi	3.62	*2x136*	14	450	300
RO4350D	Rogers	3.66	*2x101*	18	400	380
MEGTRON R-G525	Panasonic	4.5	*3x100*	10	410	300
Taconic TLY-5A	Taconic	2.17	*2x130*	18	600	195

Table 4 - Examples of Dimensions for 0201 Silicon Capacitors: Microstrip Waveguide (µm)

Note: It is difficult to get 100Ω differential impedance with low substrate thickness. The proposed solution is to double or even triple the layers of substrate (for example 2x136µm) and/or increase the metal thickness (for example 18µm to 25µm).

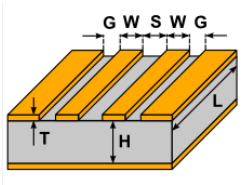
Basic design rules to follow:

W + S ≥ 700µm
W/2 + G > 320µm



Substrate	Manufacturer	Er	H	T	W	S	G
RO4003C	Rogers	3.55	2x101	18	520	200	100
MEGTRON R-G545L	Panasonic	3.5	200	14	540	200	95
HS100(D)	Hitachi	3.62	136	14	540	200	85
RO4350D	Rogers	3.66	2x101	18	520	200	105
MEGTRON R-G525	Panasonic	4.5	2x100	10	550	205	150
Taconic TLY-5A	Taconic	2.17	130	18	600	120	85

Table 5 - Examples of Dimensions for 0201 Silicon Capacitors: Coplanar Waveguide (µm)



Substrate	Manufacturer	Er	H	T	W	S	G
RO4003C	Rogers	3.55	*254*	18	450	380	300
MEGTRON R-G545L	Panasonic	3.5	200	14	400	400	400
HS100(D)	Hitachi	3.62	*2x136*	14	450	300	300
RO4350D	Rogers	3.66	*2x101*	18	400	500	400
MEGTRON R-G525	Panasonic	4.5	*3x100*	10	400	330	200
Taconic TLY-5A	Taconic	2.17	*2x130*	18	500	200	120

Table 6 - Example of Dimensions for 0201 Silicon Capacitors: Grounded Coplanar Waveguide (µm)

Note: It is difficult to get 100Ω differential impedance with low substrate thickness. The proposed solution is to double or even triple the layers of substrate (for example 2x136µm)

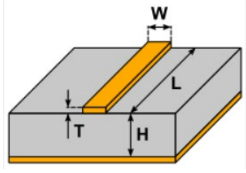
Design examples for 50Ω single-ended lines

Here is a selection of substrates that are widely used for RF designs, proposing various dielectric constants and thicknesses. Using these parameters, the width and gaps were computed in order to obtain a 50 Ω single-ended impedance.

The εr stated in the following tables are given by the manufacturers. “design” εr has been chosen wherever available (Rogers substrates)

There is no soldermask and no underfill.

0201M (600µm x 300µm x 100µm) capacitor size:

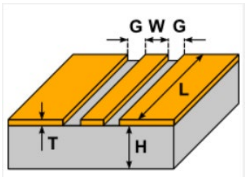


Substrate	Manufacturer	Er	H	T	W
RO4003C	Rogers	3.55	101	18	210
MEGTRON R-G545L	Panasonic	3.5	130	14	280
HS100(D)	Hitachi	3.62	136	14	290
RO4350D	Rogers	3.66	101	18	208
MEGTRON R-G525	Panasonic	4.5	100	10	180
Taconic TLY-5A	Taconic	2.17	100	18	300

Table 7 - Examples of Dimensions for 0201M Silicon Capacitors: Microstrip Waveguide (µm)

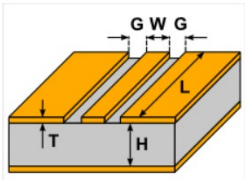
Basic design rule to follow:

W/2 + G > 170µm



Substrate	Manufacturer	Er	H	T	W	G
RO4003C	Rogers	3.55	101	18	240	58
MEGTRON R-G545L	Panasonic	3.5	200	14	275	55
HS100(D)	Hitachi	3.62	136	14	275	55
RO4350D	Rogers	3.66	101	18	290	62
MEGTRON R-G525	Panasonic	4.5	100	10	280	50
Taconic TLY-5A	Taconic	2.17	100	18	280	53

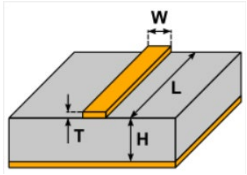
Table 8 - Examples of Dimensions for 0201M Silicon Capacitors: Coplanar Waveguide (µm)



Substrate	Manufacturer	Er	H	T	W	G
RO4003C	Rogers	3.55	101	18	185	80
MEGTRON R-G545L	Panasonic	3.5	200	14	280	65
HS100(D)	Hitachi	3.62	136	14	235	80
RO4350D	Rogers	3.66	101	18	190	90
MEGTRON R-G525	Panasonic	4.5	100	10	170	100
Taconic TLY-5A	Taconic	2.17	130	18	230	50

Table 9 - Example of Dimensions for 0201M Silicon Capacitors: Grounded Coplanar Waveguide (µm)

0201 (800µm x 600µm x 100µm) capacitor size:

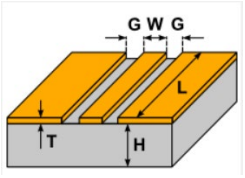


Substrate	Manufacturer	Er	H	T	W
RO4003C	Rogers	3.55	2x101	18	440
MEGTRON R-G545L	Panasonic	3.5	200	14	440
HS100(D)	Hitachi	3.62	*2x136*	14	580
RO4350D	Rogers	3.66	*2x101*	18	430
MEGTRON R-G525	Panasonic	4.5	*2x100*	10	400
Taconic TLY-5A	Taconic	2.17	130	10	400

Table 10 - Examples of Dimensions for 0201 Silicon Capacitors: Microstrip Waveguide (µm)

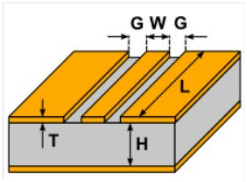
Basic design rule to follow:

W/2 + G > 320µm



Substrate	Manufacturer	Er	H	T	W	G
RO4003C	Rogers	3.55	101	18	600	80
MEGTRON R-G545L	Panasonic	3.5	200	14	600	80
HS100(D)	Hitachi	3.62	136	14	600	77
RO4350D	Rogers	3.66	101	18	600	80
MEGTRON R-G525	Panasonic	4.5	100	10	600	70
Taconic TLY-5A	Taconic	2.17	130	18	600	67

Table 11 - Examples of Dimensions for 0201 Silicon Capacitors: Coplanar Waveguide (µm)



Substrate	Manufacturer	Er	H	T	W	G
RO4003C	Rogers	3.55	3x101	18	*440*	*115*
MEGTRON R-G545L	Panasonic	3.5	200	14	400	180
HS100(D)	Hitachi	3.62	2x136	14	*500*	*180*
RO4350D	Rogers	3.66	3x101	18	*440*	*115*
MEGTRON R-G525	Panasonic	4.5	3x100	10	*490*	*250*
Taconic TLY-5A	Taconic	2.17	2x130	18	600	115

Table 12 - Example of Dimensions for 0201 Silicon Capacitors: Grounded Coplanar Waveguide (µm)

Note: It is difficult to get 100Ω differential impedance with low substrate thickness. The proposed solution is to double or even triple the layers of substrate (for example 2x136µm)

Conclusion

The proposed dimensions will allow a quick start of the design, however it is mandatory to perform 3D electromagnetic simulations of the board layout including the capacitors models. Some adjustments may be needed to enhance the RF performances.

The 0201M capacitors offer more possibilities than the 0201 to get the proper matching without tapers.

Key guidelines:

- keep the line width as close as possible to the capacitor width
- keep the ground plane away from the capacitor's edges for the coplanar and grounded coplanar modes

Tools

For reference, please find below some Transmission Line Impedance Calculation tools:

- Qucs: "Qucs Transcalc 0.0.119"
- QucsStudio: "QucsStudio Transmission Line Calculator 2.5.7"
- EEWeb tools: https://www.eeweb.com/tools/microstrip-impedance

The data provided in this application note can also be found in the following Web-Tool:

sicapmatchedline.com

These data are based on substrates and parameters commonly used in existing applications but it may not correspond to your needs. However, it is possible to make a request for specific cases using the WEB Tool.

Revision history

Revision	Date	Description	Author
0.1	06/09/2019	Draft	LLR
1.0	10/01/2020	Release	LLR

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

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