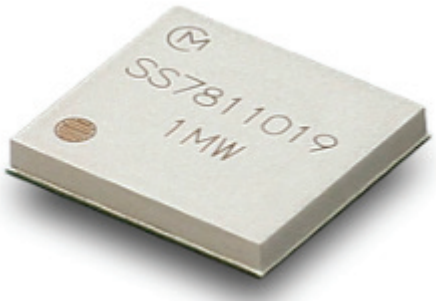
Hardware Application Note

Wi-Fi® + Bluetooth® Combo Module

Infineon CYW43455 Chipset for 802.11a/b/g/n/ac + Bluetooth 5.0

Hardware Application Note - Rev. 4.0

- Design Name: Type 1MW
- Module P/N: LBEE5HY1MW



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About This Document

This application note provides the hardware development guidelines for Type 1MW (CYW43455) and guidelines for the design of schematic, layout, and reference RF performance. For detailed module specification, refer to Type 1MW Datasheet for module specification.

Audience & Purpose

This document is targeted towards system integrators for Wi-Fi/Bluetooth solutions using Murata Type 1MW module, based on Infineon CYW43455 chipset.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	**Warning Note** Indicates very important note. Users are strongly recommended to review.
	**Info Note** Intended for informational purposes. Users should review.
	**Menu Reference** Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	**External Hyperlink** This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	**Internal Hyperlink** This symbol indicates a hyperlink within the document. **Example**: Module Introduction Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Module Introduction

Type 1MW is a small and high-performance module based on Infineon CYW43455 combo chipset which supports Wi-Fi 802.11a/b/g/n/ac + Bluetooth 5.0 BR/EDR/LE up to 433Mbps PHY data rate on Wi-Fi and 3Mbps PHY data rate on Bluetooth. The WLAN section supports SDIO v3.0 DDR50 interface and the Bluetooth section supports high-speed 4-wire UART interface and PCM for audio data.

The CYW43455 implements sophisticated and enhanced collaborative hardware mechanisms coexistence and algorithms. This ensures that WLAN and Bluetooth collaboration is optimized for maximum performance.

In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0 - MSC9 (up to 256 QAM) in 20MHz, 40MHz and 80MHz channels for data rate up to 433Mbps.

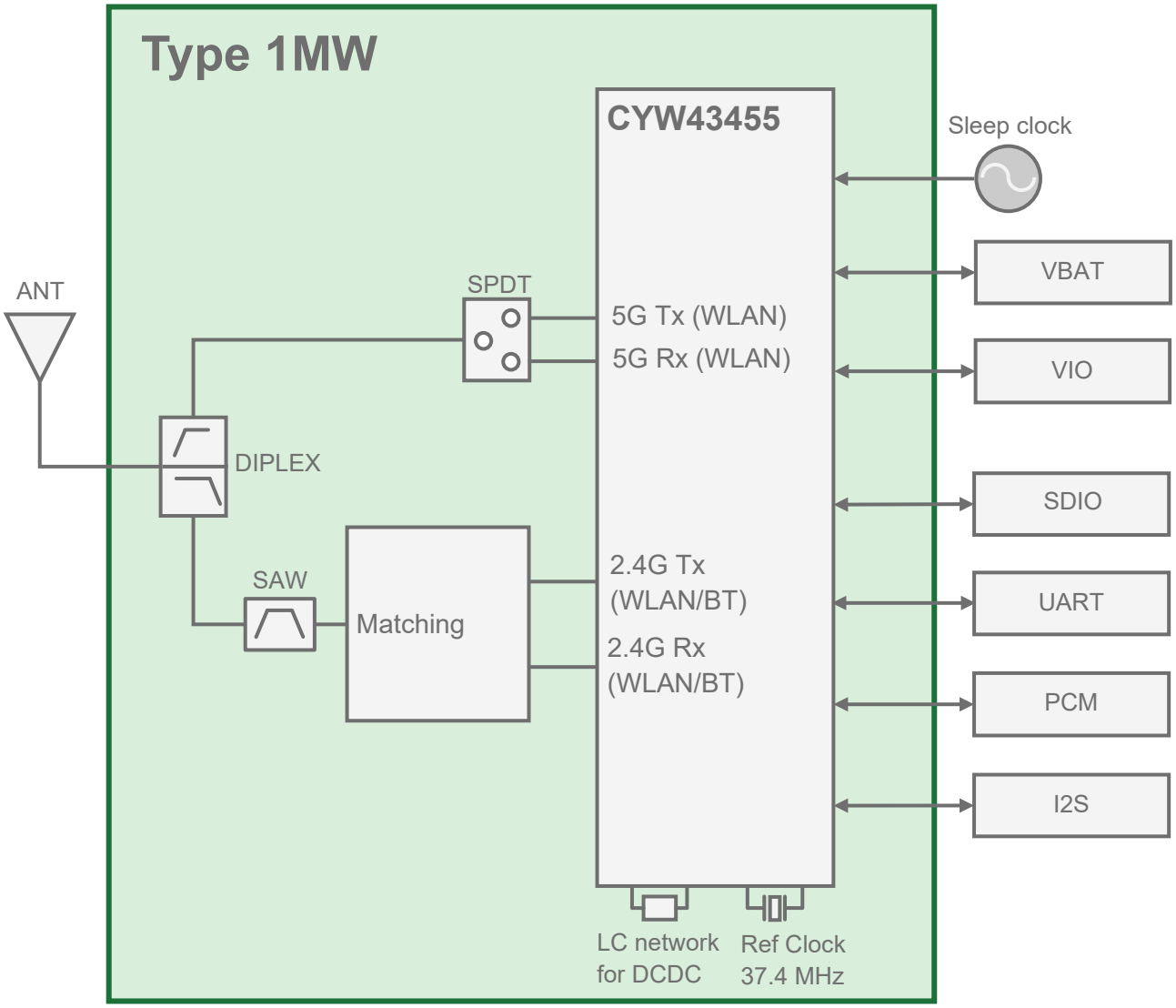
1.1 Features

- WLAN (11a/b/g/n/ac) + BT/BLE (BT5.0) combo SIP module with Infineon CYW43455
- The package type is LGA (SM type)
- This module is covered with resin molding and fully shielded with metal.
- MAC and BD address are embedded in OTP.

1.2 Hardware Block Diagram

The Type 1MW module's internal block diagram is shown in **Figure 1**.

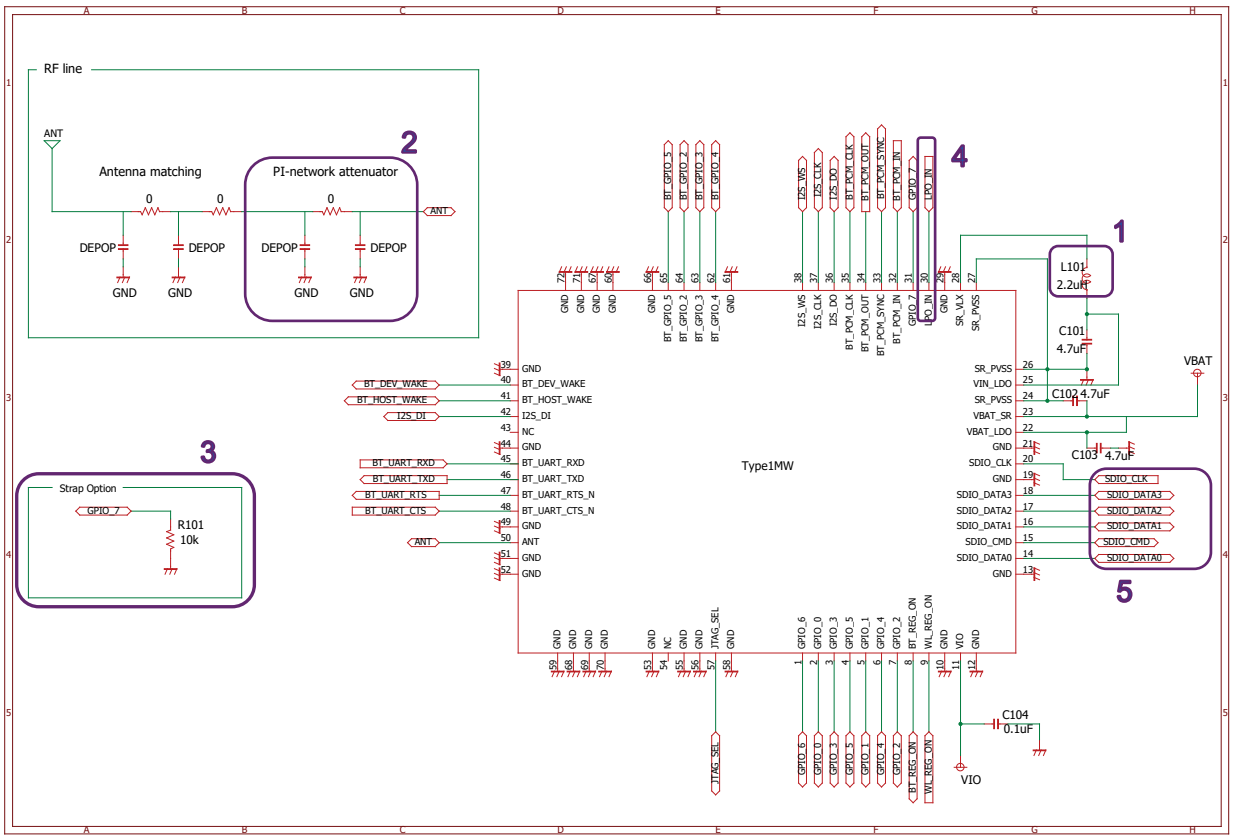
Figure 1: Block Diagram



1.3 Reference Circuitry Design

This section describes reference circuit design for Type 1MW module. **Figure 2** shows the reference circuit.

Figure 2: Reference Circuit



1. BOM list (Recommended P/N) - 2.2uH: LQM18PN2R2M
2. Attenuator circuit - Please add attenuator circuit between Type1MW and antenna matching if you use Murata Radio certification. If your antenna peak gain is higher than Murata application one, please reduce antenna gain by this pi-type attenuator.
3. Strap Option of SDIO interface voltage:
   - R101: Open SDIO interface voltage = 1.8V
   - R101: 10k Ω PD SDIO interface voltage = 3.3V

4. SDIO

Please arrange SDIO lines with 50 Ω and put series-R, shunt-C parts to reject the noise if needed.10k~100k Ω pull-ups are required on the four DATA lines and the COMD line. This requirement must be met during all operating states by using external pull-ups. This module does not have internal pull-ups on these lines. Please confirm the performance on your board.

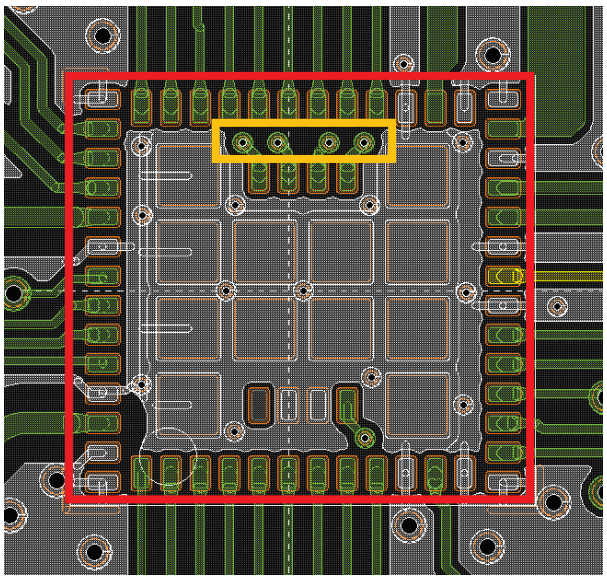
2 Hardware Design Guideline

This section describes the hardware design procedure.

2.1 Underneath of Module

Figure 3 shows the structure of the module from underneath.

Figure 3: Underneath of Module



Please refer to Type 1MW Datasheet regarding dimensions.

Murata is preparing DXF file (type1mw_module_footprint_topview.dxf)that is module footprint.

Via design between outside and inside module pad:

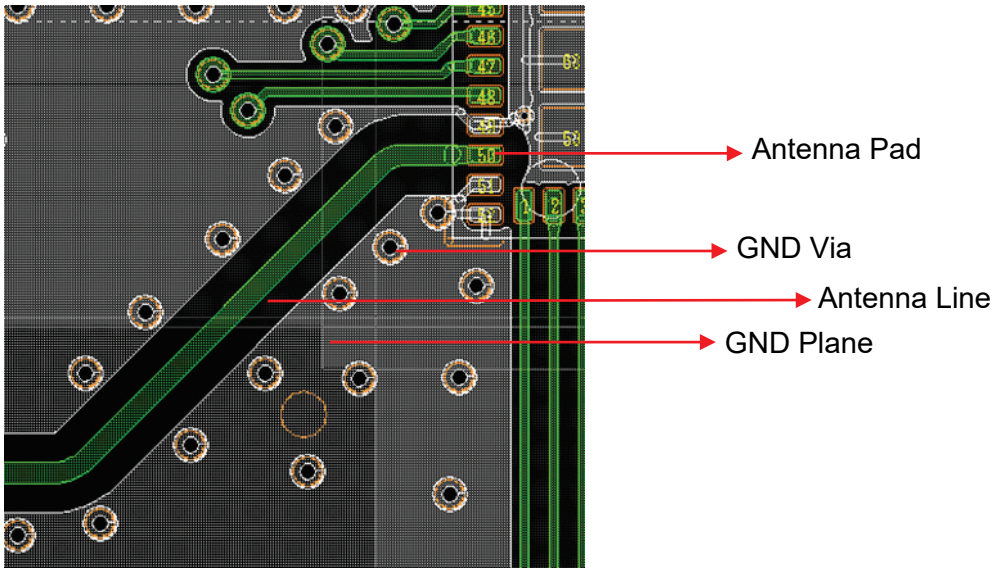
- Via Hole Φ150um
- Via Land Φ350um

2.2 Antenna Line

Antenna line should be 50 Ω. There should be enough GND via along with Antenna line. Make sure that pi matching circuit is located right before the Wi-Fi antenna on the main board.

The antenna for 1MW is shown in **Figure 4**.

Figure 4: Type 1MW Antenna

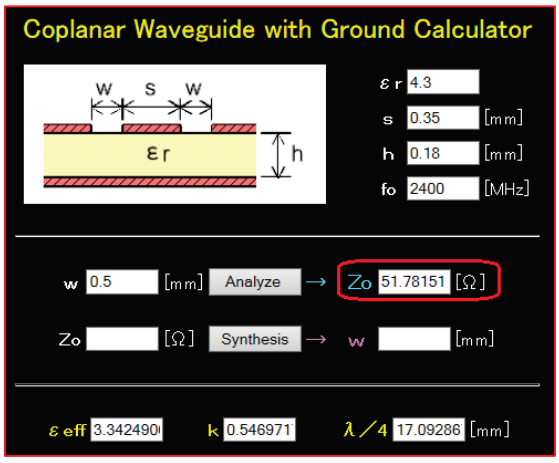


To know how to make 50 Ω line, refer to: I-Laboratory.

An example of the conditions of 50 Ω lines of evaluation board is as below:

- Epsilon: 4.3
- RF trace width(s)**:** 0.35mm
- GND gap(h)**:** 0.18mm
- GND gap(w): 0.5mm
- The line impedance is Z0 = 51.8 Ω.

Figure 5: Coplanar Waveguide



2.3 VBAT/CBUCK Line

Make the line from SR_VLX to VIN_LDO as short as possible. C1:4.7uF capacitor should be as close to VIN_LDO as possible.

If the main board is multilayer PCB type, it is better to separate the GND place for this area on the top later, then connect it to the main GND through the via hole on the lower layer.

On VBAT_SR line, C2:4.7uF bypass capacitor should be located as close to the module as possible. C2:4.7uF bypass capacitor should connect to SR_PVSS.

Figure 6 shows the GND placement for layer 1.

Figure 6: Layer 1

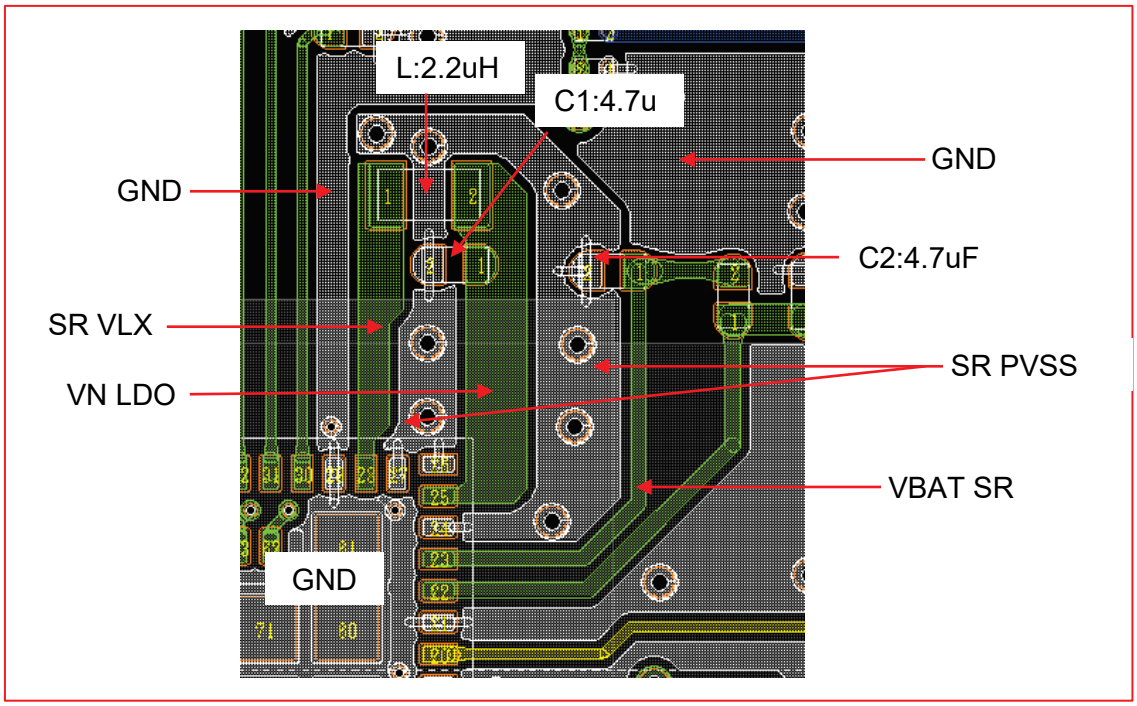
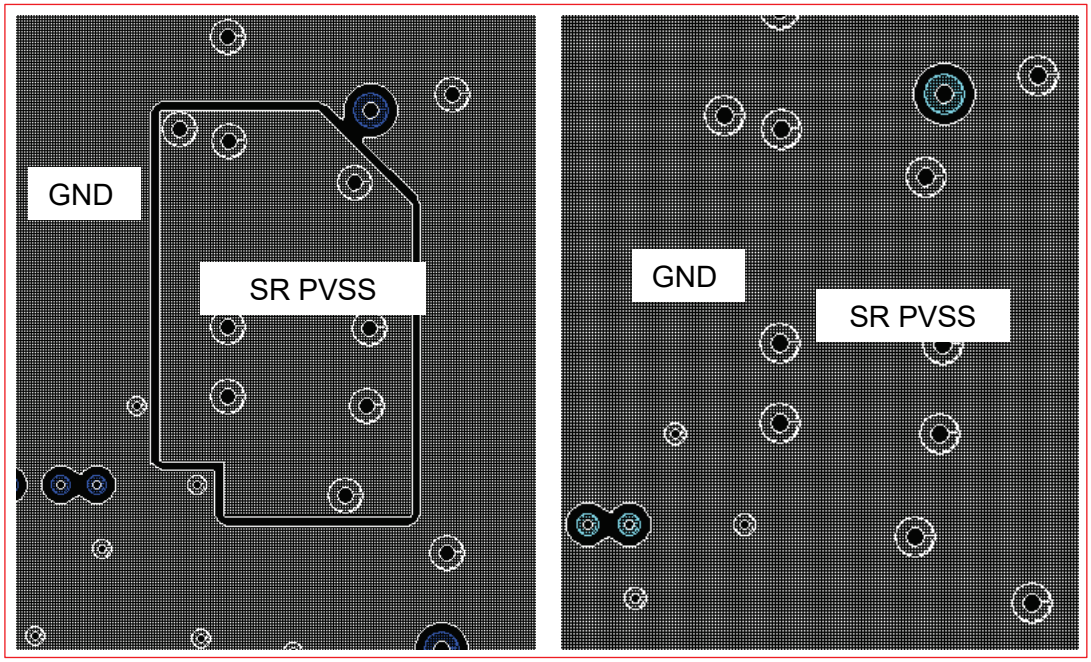


Figure 7 shows the GND placement for layer 2 and layer 3.

Figure 7: Layer 2 and Layer 3



2.4 Antenna Information

This section describes the antenna information for Type 1MW module.

2.4.1 Appearance of the Antenna

The antenna design measurements and specifications are shown in **Figure 8** and **Figure 9**.

Figure 8: Antenna Design Measurements

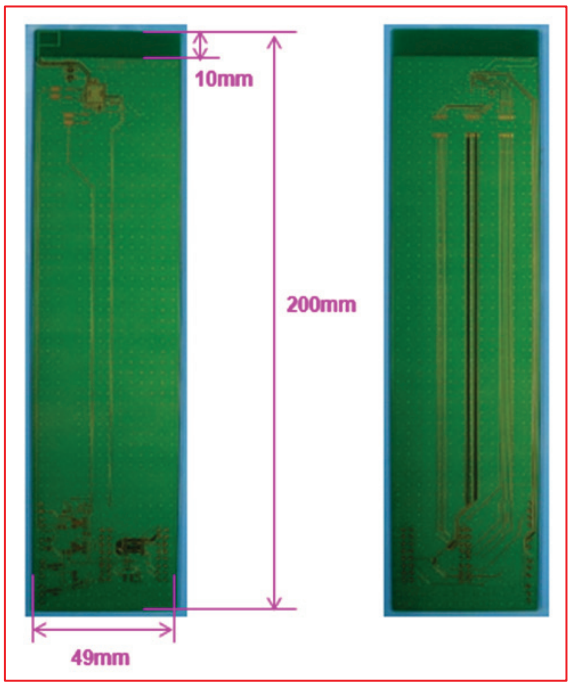


Figure 9: Antenna Design Specifications

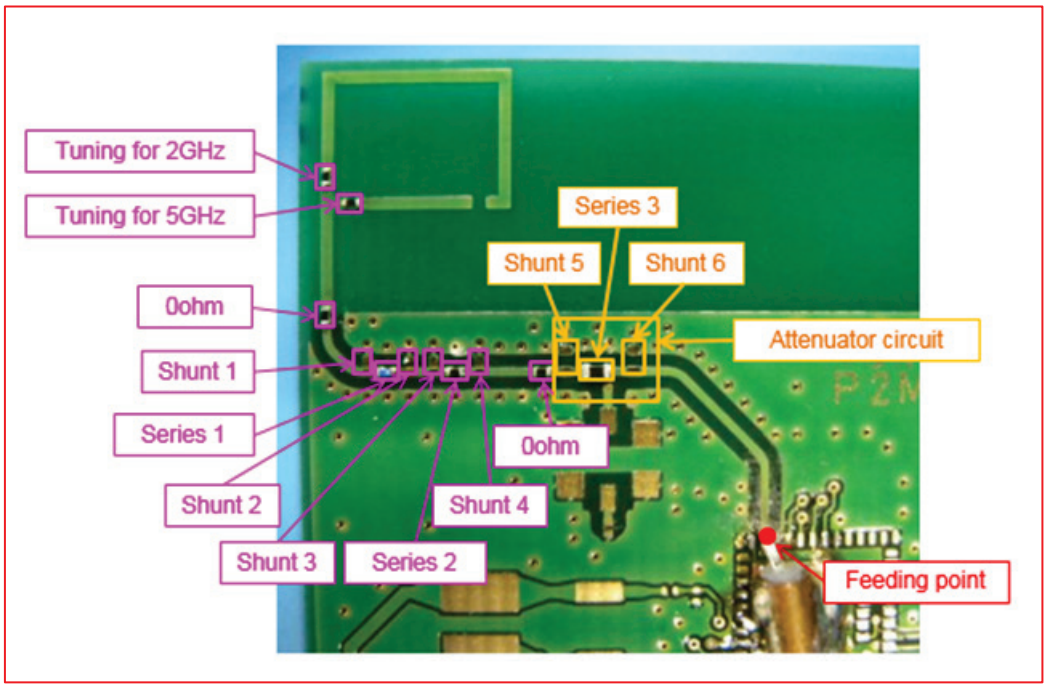


Table 2 describes antenna design specifications.

Table 2: Antenna Design Descriptions

Tuning for 2 GHz	Tuning for 5 GHz-1	Matching Circuit	Attenuator Circuit
0 Ω	0 Ω	Shunt 1: None, Series 1: 1.4 nH, Shunt 2: None,	Shunt 5: 270 Ω, Series 3: 20 Ω, Shunt 6: 270 Ω
		Shunt 3: None, Series 2: 0 Ω, Shunt 4: None	

1005 size component is applied to attenuator circuit

2.4.2 Antenna Measurement Directions

Antenna measurement directions for XY plane, YZ plane, and ZX plane is shown in **Figure 10**.

Figure 10: Antenna Measurement Directions

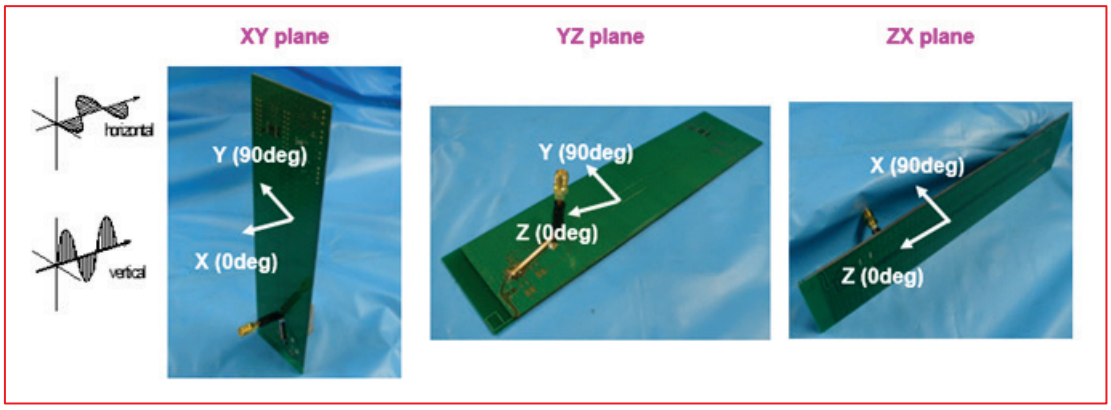


Figure 11: Antenna Layout

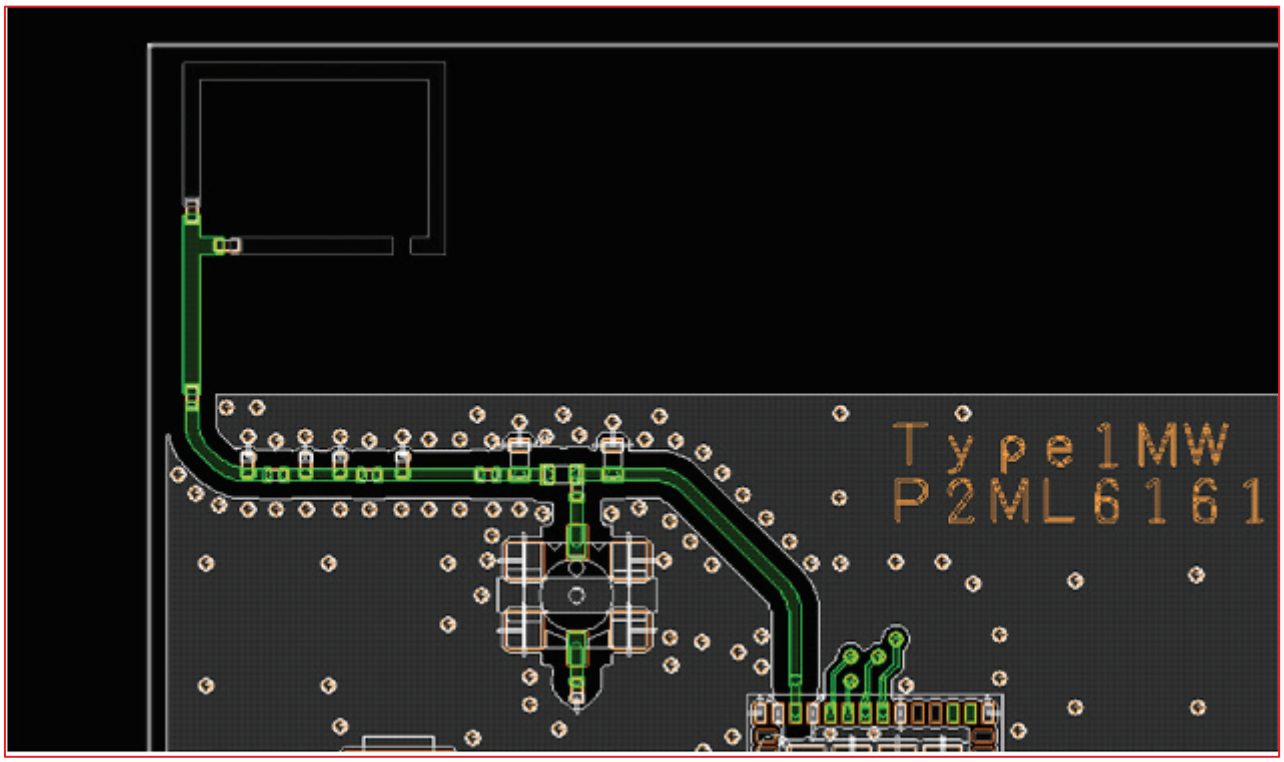
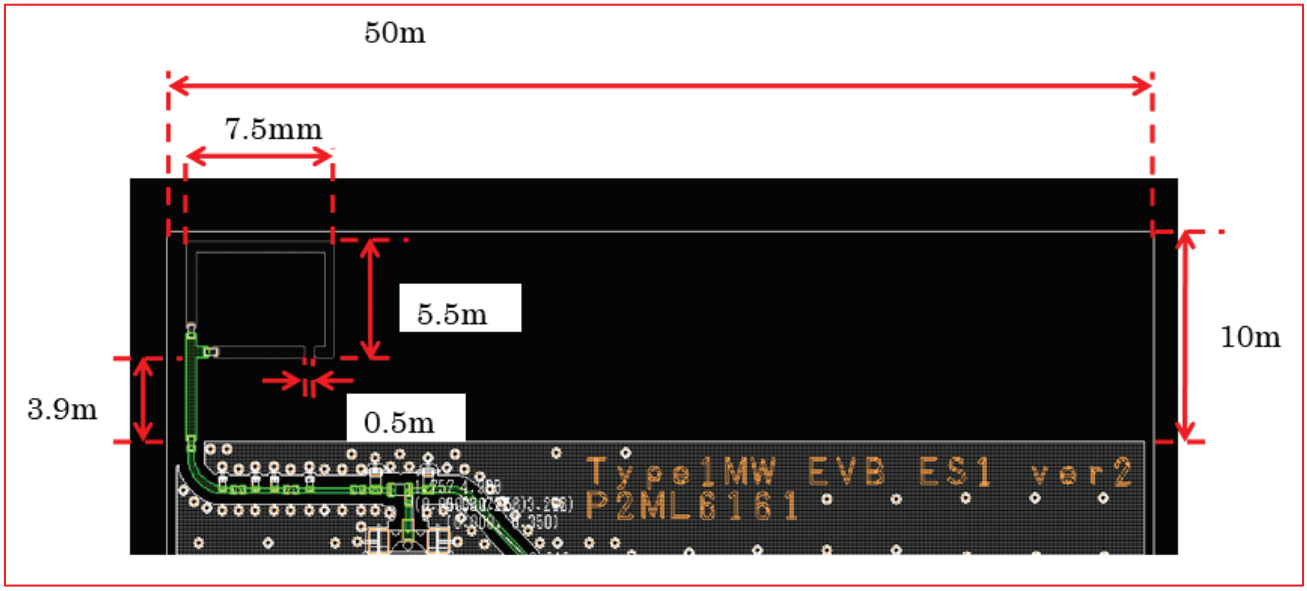


Figure 12: Antenna Layout Measurements



Antenna trace width 0.5 mm

2.4.3 Antenna Performance

Table 3 and **Figure 13** describe the antenna performances for 2.4 GHz.

Table 3: Antenna Gain and Efficiency - 2.4 GHz

Linear Polarization		XY-Plane (dBi)		YZ-Plane (dBi)		ZX-Plane (dBi)		Total Efficiency (dB)
		Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	
2400 MHz	Maximum	-3.8	-4.0	-0.1	-18.5	-6.0	-1.2	-4.3
	Average	-8.1	-7.7	-5.1	-24.0	-13.3	-3.6	
2442 MHz	**Maximum**	**-3.6**	**-3.7**	**0.1**	**-17.0**	**-5.5**	**-0.8**	**-3.9**
	Average	**-7.9**	**-7.3**	**-4.7**	**-22.9**	**-13.0**	**-3.3**	
2484 MHz	Maximum	-3.3	-3.6	0.0	-16.5	-5.5	-0.6	-3.8
	Average	-7.8	-7.1	-4.6	-22.8	-12.8	-3.1	

Figure 13: Antenna Directivity - 2.4 GHz

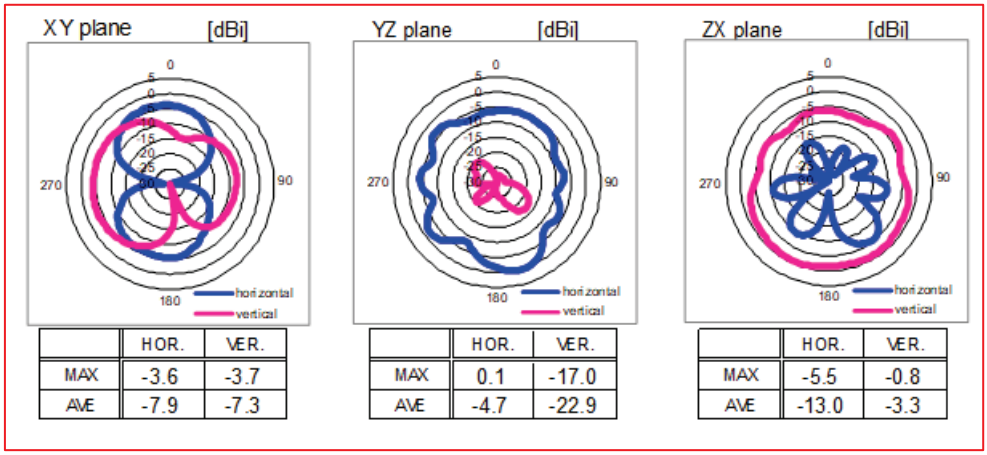
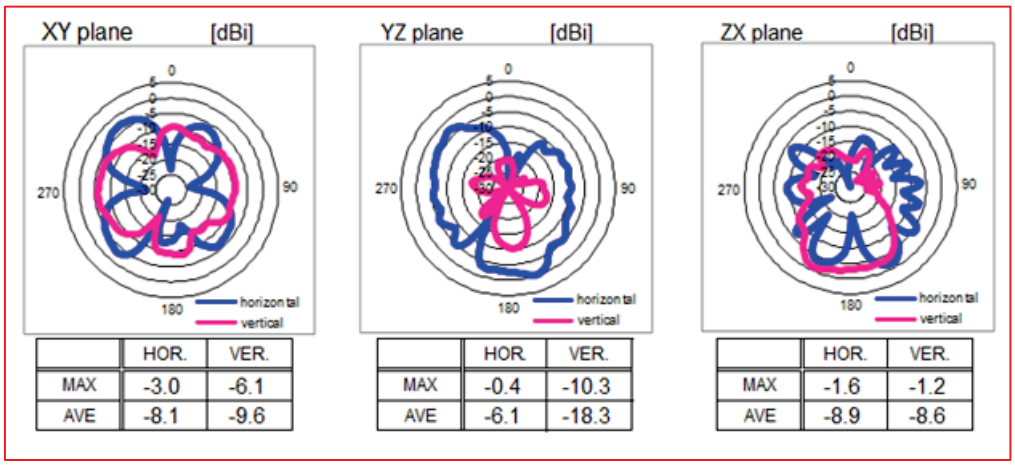


Table 4 and **Figure 14** describe the antenna performances for 5 GHz.

Table 4: Antenna Gain and Efficiency - 5 GHz

Linear Polarization		XY-Plane (dBi)		YZ-Plane (dBi)		ZX-Plane (dBi)		Total Efficiency (dB)
		Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	
5150 MHz	Maximum	-3.0	-6.1	-0.4	-10.3	-1.6	-1.2	-5.6
	Average	-8.1	-9.6	-6.1	-18.3	-8.9	-8.6	
5500 MHz	**Maximum**	**-2.4**	**-4.9**	**-0.6**	**-10.8**	**-0.7**	**-2.9**	**-5.2**
	Average	**-7.6**	**-8.6**	**-5.7**	**-19.0**	**-9.0**	**-10.0**	
5850 MHz	Maximum	-1.8	-4.0	-1.3	-10.7	-0.9	-5.1	-5.4
	Average	-7.6	-8.0	-6.2	-18.4	-8.6	-11.8	

Figure 14: Antenna Directivity - 5 GHz



	HOR.	VER.
MAX	-3.0	-6.1
AVE	-8.1	-9.6

	HOR.	VER.
MAX	-0.4	-10.3
AVE	-6.1	-18.3

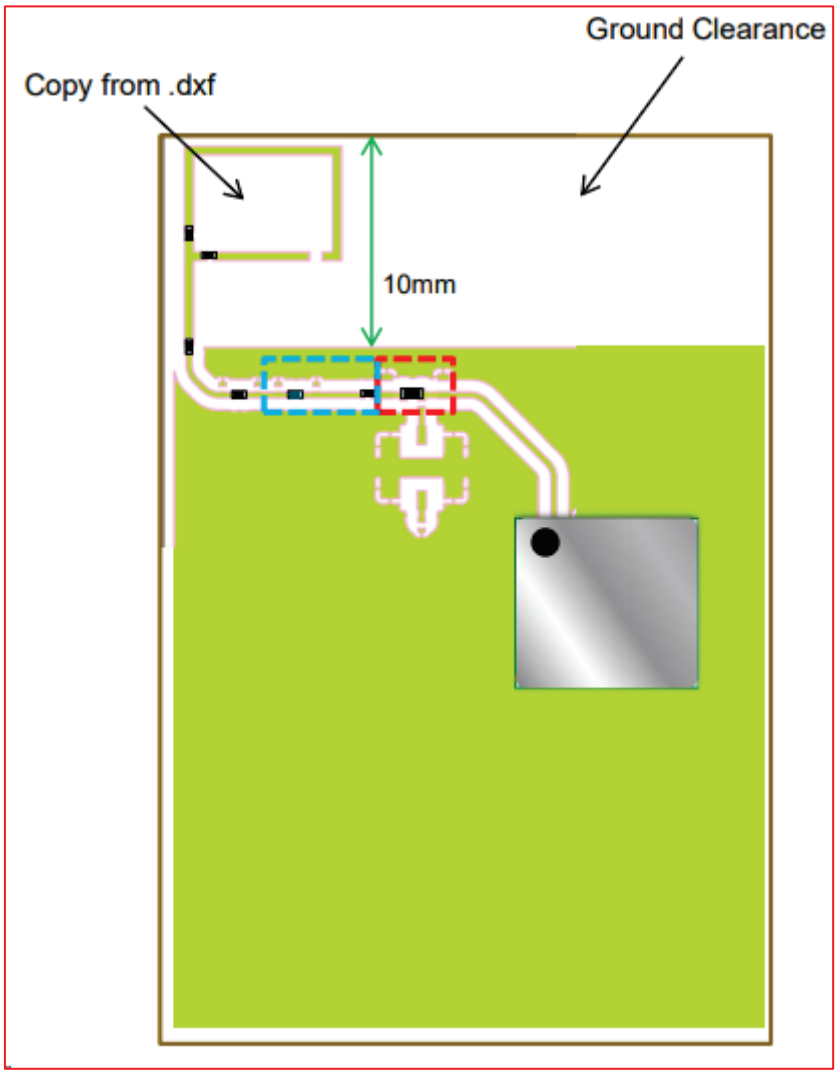
	HOR.	VER.
MAX	-1.6	-1.2
AVE	-8.9	-8.6

2.4.4 Layout Guide for Good Antenna Performance

- Place the antenna on top-left (or right) corner.
- Keep GND clearance all long the top edge.
- Place metal stuff as far as possible.
- Place pi-network + one component on series for matching.
  - Put 0 Ω in series and no load in parallel on the initial design.
  - Put appropriate value of C/L/R depends on actual performance.
- Place pi-network for attenuating.
  - Put 0 Ω in series and no load in parallel on the initial design.
  - Put appropriate value of R depends on actual performance.

Figure 15 shows the antenna layout guide.

Figure 15: Antenna Layout Guide



2.4.5 Antenna Design

Please perform the antenna design that followed the specifications of the antenna.

The following provide information about the signal line between an antenna and a module.

- It is a 50 Ω line design.
- Fine tuning of return loss etc. can be performed using a matching network. However, it is required to check "Class1 change" and "Class2 change" which the authorities define then.

The concrete contents of a check are the following three points:

- It is the same type as the antenna type of antenna specifications.
- An antenna gain is lower than a gain given in antenna specifications.
- The emission level is not getting worse.

Table 5: 50 Ω Line Testing

	Antenna
Antenna type	Monopole pattern antenna
50 Ω feed line length	We test it at 0 mm as a representative

“Attenuator” part should be pi-network as above.

Appropriate value of R depends on the design of the product. Put 0 Ω in series and no load in parallel on the initial design.

“Matching1” part should be pi-network + 1 series component as above. Appropriate value of L/C/R depends on the design of the product.

Put 0 Ω in series and no load in parallel on the initial design.

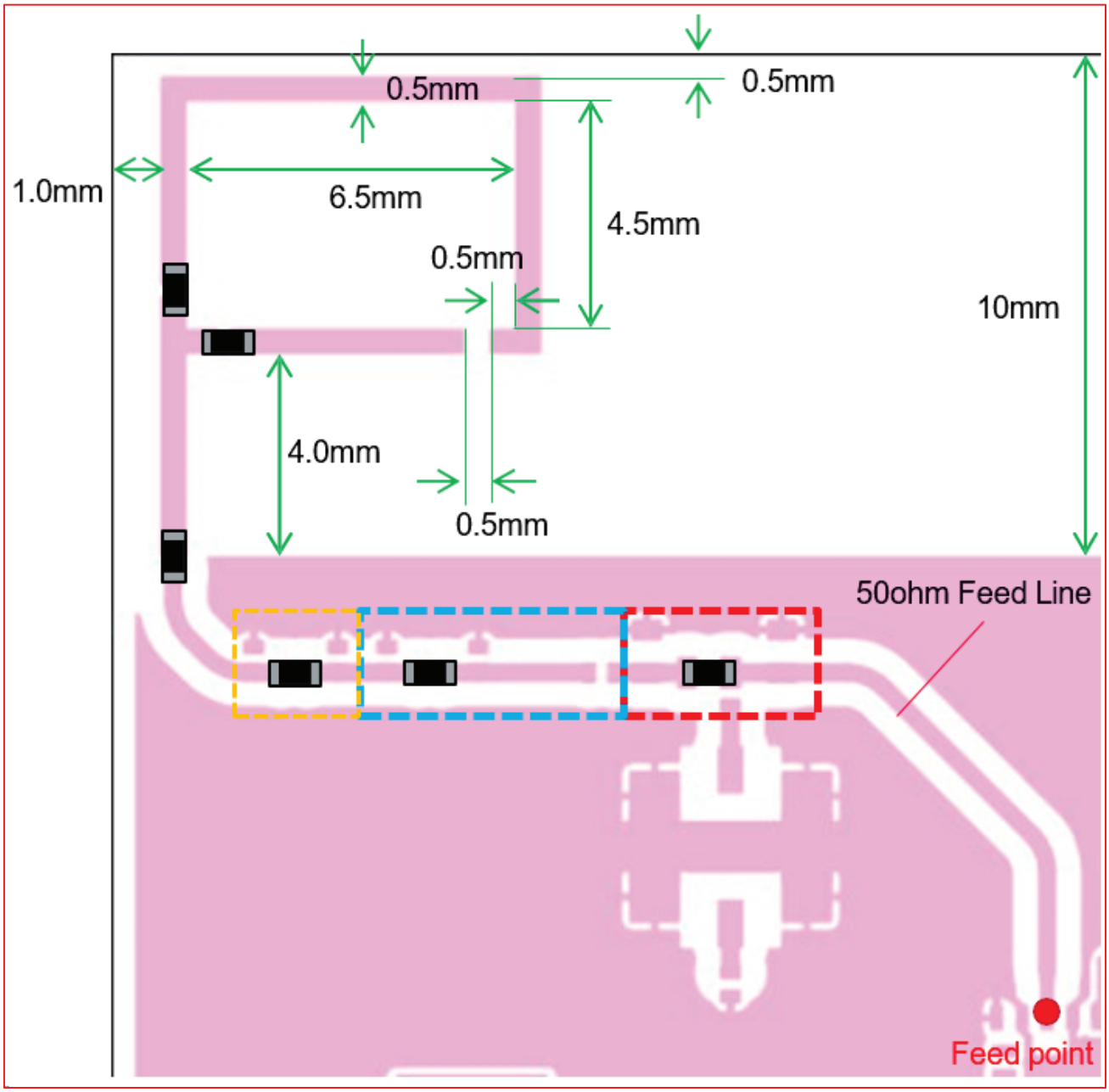
“Matching2” part should be pi-network as above.

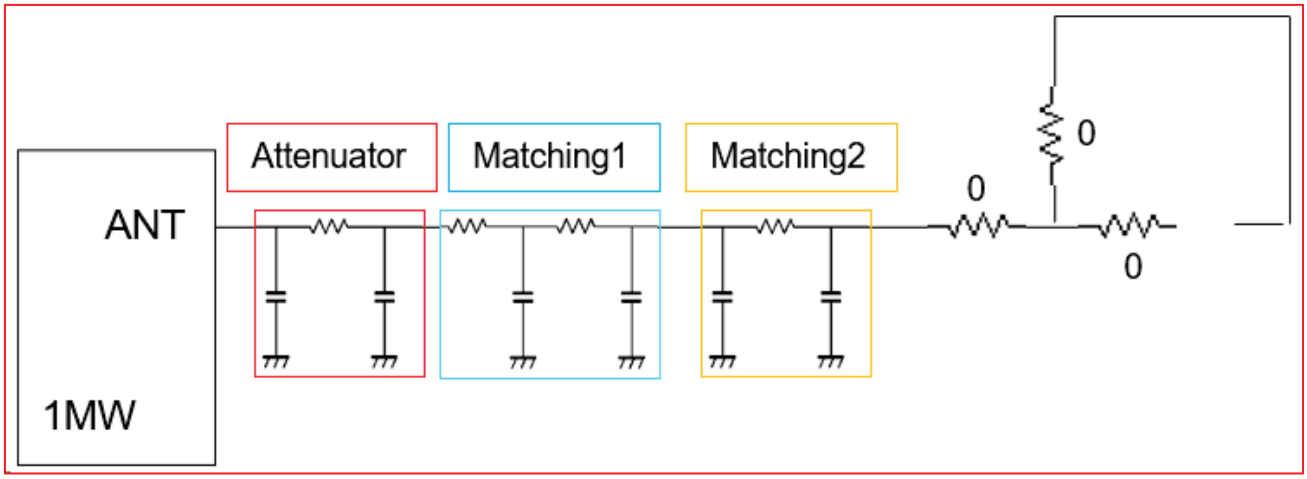
Only matching1 might achieve the antenna tuning, but if you have a place to have this part, please add it.

Appropriate value of L/C/R depends on the design of the product. Put 0 Ω in series and no load in parallel on the initial design.

Figure 16 shows the antenna design. Please follow type1mw_antenna_p2ml6161.dxf file.

Figure 16: Antenna Design





3 RF Measurement Results

This section describes Tx output power level and Rx minimum sensitivity level (at module antenna port)

3.1 TX Output Power Level (at Module Antenna Port)

The transmit output power levels for Wi-Fi and Bluetooth for the module are described in the 1MW datasheet.

3.2 Rx Minimum Sensitivity Level (at Module Antenna Port)

This section describes the power levels for Wi-Fi and Bluetooth.

3.2.1 Rx Minimum Sensitivity Level - Wi-Fi

Conditions:

- VBAT = 3.3V, VIO = 1.8V
- FW version**:** version 7_45_86

Table 6: Rx Minimum Sensitivity Level - WLAN at 2.4 GHz

Frequency [MHz]	Rx Minimum Sensitivity Level [dBm]					
	11b		11g		11n	
	1Mbps	11Mbps	6Mbps	54Mbps	MCS0	MCS7
2412	-98.5	-89.3	-94.0	-76.8	-94.0	-75.0
2442	-98.8	-89.7	-94.1	-77.0	-94.1	-75.0
2472	-98.0	-88.8	-93.4	-76.3	-93.4	-74.4

Table 7: Rx Minimum Sensitivity Level - WLAN at 5 GHz (20 MHz)

Frequency [MHz]	Rx Minimum Sensitivity Level [dBm]					
	11a		11n (HT20)		11ac (VHT20)	
	6Mbps	54Mbps	MCS0	MCS7	MCS0	MCS8
5180	-93.2	-76.1	-93.2	-74.2	-93.1	-69.9
5500	-93.2	-76.1	-93.1	-74.1	-92.9	-69.9
5825	-93.4	-76.3	-93.3	-74.3	-93.1	-70.1

Table 8: Rx Minimum Sensitivity Level - WLAN at 5 GHz (40 MHz)

Frequency [MHz]	Rx Minimum Sensitivity Level [dBm]			
	11n(HT40)		11ac (VHT40)	
	MCS0	MCS7	MCS0	MCS9
5190	-89.9	-70.4	-90.2	-65.2
5510	-90.1	-70.4	-90.4	-65.3
5795	-90.2	-70.5	-90.6	-65.5

Table 9: Rx Minimum Sensitivity Level - WLAN at 5GHz (80 MHz)

Frequency [MHz]	Rx Minimum Sensitivity Level [dBm]	
	11ac (VHT80)	
	MCS0	MCS9
5210	-87.5	-62.5
5530	-87.8	-62.6
5775	-87.7	-62.6

3.2.2 Rx Minimum Sensitivity Level - Bluetooth

Conditions:

- VBAT = 3.3V, VIO = 1.8V
- Hcd file version: BCM4345C0_003.001.025.0139.0234.hcd

Table 10: Rx Minimum Sensitivity Level – Bluetooth

Frequency [MHz]	Rx Minimum Sensitivity Level [dBm]		
	DH5	3DH5	BLE
2402	-91.0	-90.1	-95.5
2440	-91.9	-91.3	-95.5
2480	-90.6	-90.6	-95.1

4 Current Consumption

This section describes the current consumption conditions and parameters for Wi-Fi and Bluetooth.

4.1 Current Consumption - Wi-Fi

This section describes the Tx/Rx current consumption for Wi-Fi.

4.1.1 Tx/Rx Current Consumption

Table 11 shows the Tx/Rx current consumption for Wi-Fi at 2.4 GHz.

Table 11: Tx/Rx Current Consumption - WLAN at 2.4 GHz

Mode	Rate	Tx Current		Rx current [mA][1]
		Setting Power	Tx Current [mA][2]	
11b	1 Mbps	17	301	58
11g	6 Mbps	16	320	58
11n	MCS0	14	328	58

Table 12 shows the Tx/Rx current consumption for Wi-Fi at 5 GHz.

Table 12: Tx/Rx Current Consumption - WLAN at 5 GHz

Mode	Rate	Tx Current		Rx current[mA][1]
		Setting Power	Tx Current [mA][2]	
11a	6Mbps	15	301	75
11n (HT40)	MCS0	15	320	85
11ac (VHT80)	MCS0	12	328	110

4.1.2 Sleep Current Consumption

Conditions:

- VBAT = 3.3V, VIO = 1.8V
- WL_REG_ON: ON, BT_REG_ON: OFF
- FW version: 7.45.59.4

Table 13 describes the sleep current consumption.

Table 13: Sleep Current Consumption

Band	Mode	VBAT (3.3V)	VDDIO (1.8V)
		mA	uA
	IEEE Power save, Inter Beacon[3]	0.09	180
2.4GHz	IEEE Power Save: DTIM1[4]	1.77	180
	IEEE Power Save: DTIM3	0.62	180
	IEEE Power Save: DTIM5	0.43	180
5 GHz	IEEE Power Save: DTIM1	0.91	180
	IEEE Power Save: DTIM3	0.40	180
	IEEE Power Save: DTIM5	0.30	180

4.2 Bluetooth Low Energy Current Consumption

Conditions:

- VBAT = 3.3V, VIO = 1.8V
- WL_REG_ON: OFF, BT_REG_ON: ON

[1] Carrier sense when no carrier present
[2] Setting values: 1024byte, 20usec interval
[3] Idle, not associated, or inter-beacon.
[4] Beacon Interval = 100 ms

- Hcd file version: BCM4345C0_003.001.025.0139.0234.hcd

Table 14 describes the BLE current consumption.

Table 14: BLE Current Consumption

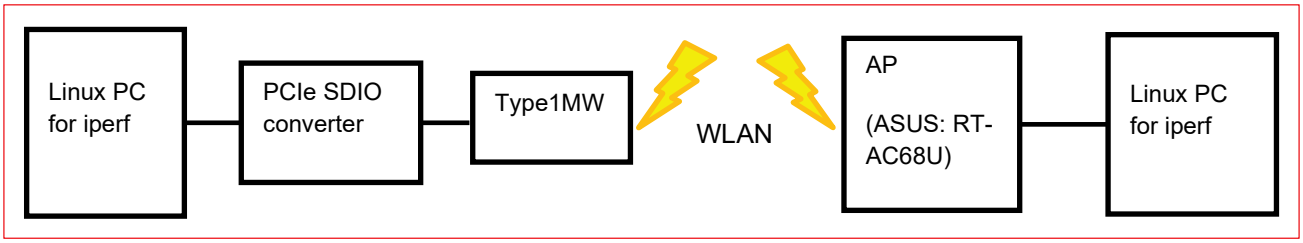
Mode	VBAT (3.3V)	VDDIO (1.8V)
	uA	uA
BLE Scan	213	155
BLE Adv-Unconnectable 1.00sec	98	155
BLE connected 1sec	42	159

BLE Scan - No devices present. A 1.28 second interval with a scan window of 11.25ms.

5 Throughput Performance

The test environment is shown in **Figure 17**.

Figure 17: Test Environment



Throughput measurement tool: iperf

Type1MW Configuration

- WLAN Driver version: 1.141.67.11
- FW version: 7.45.189
- NVRAM: bcm943455wlsagb_Type1MW_3.3v_180112.txt
- VBAT = 3.3V, VIO = 1.8V
- WL_REG_ON: ON, BT_REG_ON: ON

The WLAN throughput data for 2.4 GHz are shown in **Table 15**.

Table 15: WLAN Throughput Data - 2.4 GHz

11n_HT20_MCS7	Tx [Mbps]	Rx [Mbps]
TCP	52	58
UDP	55	57

The WLAN throughput data for 5 GHz are shown in **Table 16**.

Table 16: WLAN Throughput Data – 5 GHz

11ac_VHT80_MCS9	Tx [Mbps]	Rx [Mbps]
TCP	228	231
UDP	316	278

6 References

Table 17 reviews all the key reference documents that the user may like to refer to.

Table 17: Reference Table

Support Site	Notes
Murata Type 1MW Module Datasheet	Murata Type 1MW module datasheet (type1mw.pdf)
Murata Type 1MW Module Footprint	Murata Type 1MW module footprint (type1mw_module_footprint_topview.dxf)
Murata Type 1MW Antenna	Murata Type 1MW module trace antenna (type1mw_antenna_p2ml6161.dxf)
Linux WLAN Configuration	Murata GitHub link for Linux NVRAM file for 1MW
Linux WLAN Regulatory Configuration	Murata GitHub link for Linux CLM_BLOB file for 1MW
Linux User Guide	Murata Linux User Guide for Infineon modules (Murata Wi-Fi & BT (IFX) Solution for i.MX Linux User Guide.pdf).

7 Technical Support Contacts

Table 18 lists all the support resources available for the Murata Wi-Fi/BT solution.

Table 18: List of Support Resources

Support Site	Notes
Murata Community Forum	**Primary support point for technical queries.** This is an open forum for all customers. Registration is required.
Murata i.MX Landing Page	No login credentials required. Murata documentation covering hardware, software, testing, etc. is provided here.
Murata uSD-M.2 Adapter Landing Page	Landing page for uSD-M.2 Adapter. In conjunction with Murata i.MX Landing Page, this should provide the user with comprehensive getting started documentation.
Murata Module Landing Page	No login credentials required. Murata documentation covering all Infineon-based Wi-Fi/BT modules is provided here.

Revision History

Revision	Date	Section	Change Description
1.0	Apr 16, 2018		First Issue
2.0	Dec 28, 2018	1.3 Reference circuit 5.0 Throughput performance	Revised BOM list. Added test environment of throughput test.
3.0	Oct 28, 2019	1.0 Module Introduction 4.2 BT current consumption	Updated BT version (4.2 to 5.0) Corrected condition (VIO = 3.3V->1.8V)
4.0	June 13, 2022		Converted to new format.