Hardware Application Note

Type 1WL-633 LoRa + Wi-Fi® + Bluetooth® + GNSS Module Rev.E

Semtech LR1110 Chipset for LoRa, Wi-Fi Scan, GNSS Scan
STMicro STM32WB55 Chipset for MCU and Bluetooth LE
Airoha MT3333 Chipset for High-Performance GNSS

- Design Name: Type 1WL-633
- P/N: LBEU5ZZ1WL-633

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About This Document

Murata's Type 1WL-633 is a small and high-performance module based on Semtech LR1110 + STMicro STM32WB55 + Airoha MT3333 chipset, supporting LoRa + IEEE 802.11 b/g/n Wi-Fi Passive Scanner + Bluetooth 5.2 LE + GNSS. This application note provides RF and hardware design guidance. Refer to Type 1WL-633 Datasheet for module specification.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product. In particular RF, hardware, system, and software engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Embedded Artists AB Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This application note provides detailed information on schematic/layout design, and references RF performance benchmarks. Refer to for Type 1WL-633 Datasheet for module specification.

2 Module Introduction

Type 1WL-633 Module is a multi-technology fused location LPWAN module designed as the ideal platform to develop a wide range of IoT tracking solutions, minimizing the Total Cost of Ownership (TCO) of IoT geolocation use cases. It allows your engineering to focus on the use case, to optimize time-to-market and cost by using less complex PCBs (all high-density devices being encapsulated), to reduce certification risk and budget, as well as testing time and cost for mass production.

This LoRaWAN® fused location module is a cost effective, ultra-low power and small footprint SiP (System in Package) integrating the high performance STM32WB micro-controller (MCU) with integrated Bluetooth 5.x Low Energy transceiver, the latest LoRaWAN® radio transceiver from Semtech, and an optimized arrangement of multi-technology RF engines for indoor and outdoor positioning.

The module contains 3 main chips: a high end MCU STM32WB55 associated with BLE radio, a high-performance multi-constellation GNSS receiver MT3333 (GPS, GLONASS, Beidou, and Galileo) and the Semtech transceiver LR1110 to provide LoRa & FSK sub-GHz radio, low power Wi-Fi and GNSS RX.

2.1 Features

- STM32WB MCU wireless microcontroller
  - Cortet-M4, RAM: 256KB, Flash: 1MB
  - Bluetooth Low Energy transceiver
- SEMTECH LR1110 RF IC
  - LoRa Transceiver
  - Wi-Fi Passive Scanner
  - Multi-Constellation GNSS Scanner (GPS & BeiDou)
- Airoha MT3333 GNSS chipset
  - High-performance, multi-Constellation GNSS solution
- Low power consumption
- TCXO for maximum frequency accuracy

- Structure: Metal case + PCB (Lead Free Module)
- Weight: 1200 mg
- MSL: 3
- LGA Surface-mount type
- RoHS compliant

Product name	LBEU5ZZ1WL-633
Technology	LoRa, BLE, Wi-Fi Scanner, GNSS
Peripheral I/F	UART, USB, SPI, I2C, ADC, GPIOs
Dimensions	17.50 x 17.00 x 2.15 mm (max)
Operating Temperature	- 30 °C to 85 °C
Regulatory certification	FCC, ISED, CE, JRL

2.2 Block Diagram

Figure 1 shows the block diagram of Type 1WL-633 module. “ANT_2.4G is shared between Wi-Fi Passive Scan and Bluetooth LE.

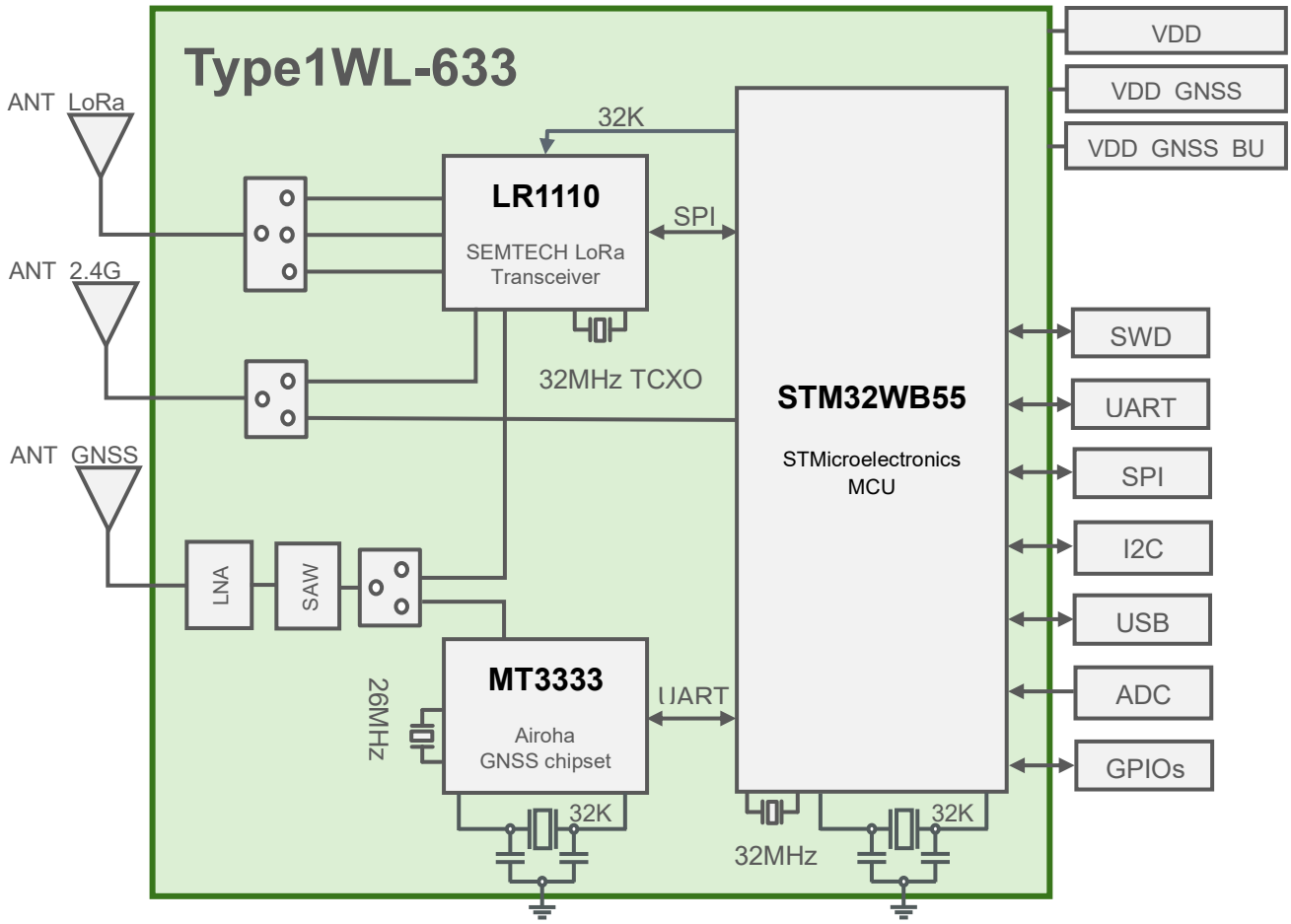


Figure 1: Block Diagram

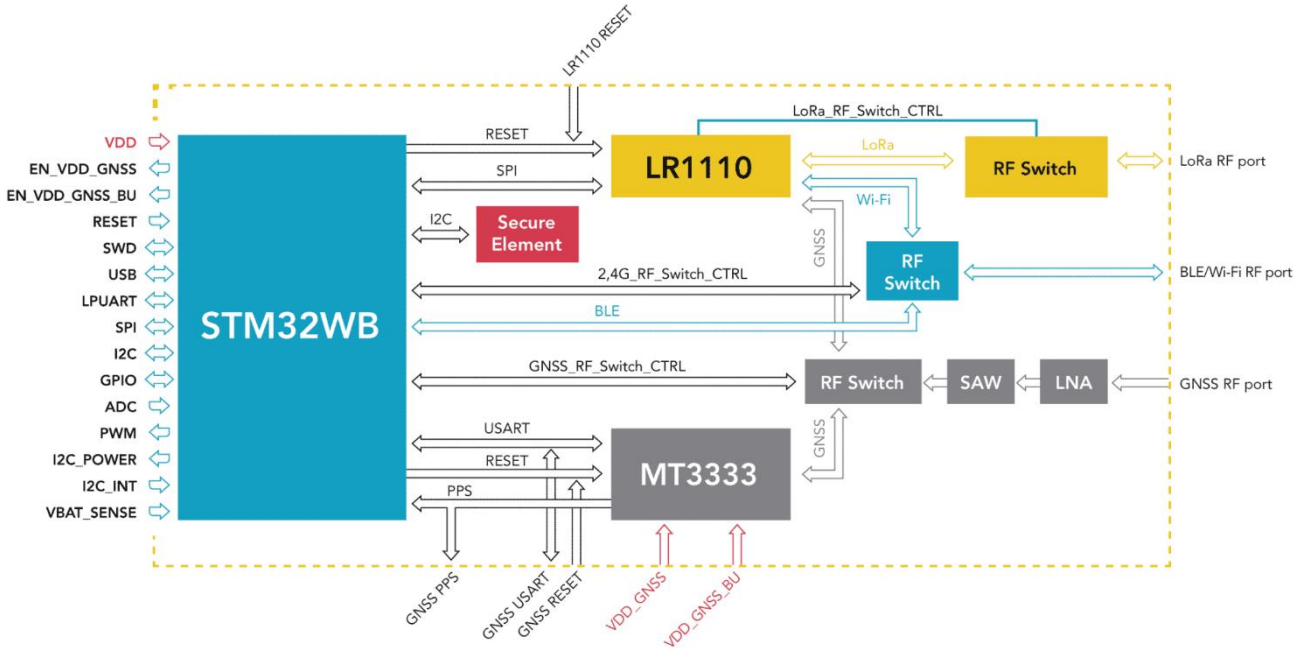


Figure 2: Module Internal Detail Connection

3 Clock Circuit

3.1 LR1110 Clock Circuit

The LoRa Edge system uses two primary clocks: a high-frequency clock running at 32MHz (referred to as 32MHz HF Clock), and a low-frequency clock running at 32.768kHz (32.768kHz LF clock):

- The 32MHz HF clock is the reference frequency for the Phase Locked Loop (PLL) and is therefore required for all the RF blocks: PLL, Radio RX/TX, Wi-Fi, and GNSS.
- The 32.768kHz LF clock is the real-time clock (RTC). This clock is necessary for keeping an accurate time base while putting the device in the lowest power consumption modes. It is used to wake-up the device from sleep mode for radio duty-cycled operations, for example for the LoRaWAN standard. It is also used by GNSS to enter advanced scan mode and for dual constellation configuration.

The 32MHz signal is derived from a 32MHZ TCXO inside of module and supplied by LR1110 via VTCXO.

The 32.768kHz signal is fed by the LSCO (low-speed clock output) of STM32WB55 inside of module.

Sending and/or receiving data packets requires a 32MHz reference clock for the radio subsystem. Although a 32.768kHz Real Time Clock (RTC) is not mandatory for the transmission and reception

of radio packets, some radio functions rely on this clock. These functions include automatic wake-up from sleep mode and duty-cycled Receive or Transmit modes, among others.

In LoRa packet transmission or reception, the 32.768kHz LF clock is used to wake up the transceiver from sleep mode when performing periodic or duty-cycled operations, such as duty-cycled RX or TX operations.

3.2 MT3333 Clock Circuit

MT3333 requires a TCXO for main clock source. Two frequencies are supported, 16.386MHz and 26MHz. The module is hardware configured to use 26MHz source. There is a 26MHz TCXO inside of module for MT3333 main clock and supplied by MT3333 via AVDD_TCXO_SW pin which powered by the AVDD28_TLDO of MT3333.

MT3333 requires a 32.768KHz clock for built-in RTC block. There is a 32.768KHz crystal inside of module for MT3333 RTC clock. The RTC clock is needed at the MT3333 power-on stage. The power domain of RTC block is 1.2V.

3.3 STM32WB55 Clock Circuit

The STM32WB55 chip integrate many sources of clocks:

- LSE: 32.768KHz external oscillator, for accurate RTC and calibration with other embedded RC oscillators
- LSI1: 32KHz on-chip low-consumption RC oscillator
- LSI2: almost 32KHz on-chip high-stability RC oscillator, used by the RF subsystem
- HSE: high quality 32MHz external oscillator with trimming, needed by the RF subsystem
- HSI16: 16 MHz high accuracy on-chip RC oscillator
- MSI: 100KHz to 48MHz multiple speed on-chip low power oscillator, can be trimmed using the LSE signal
- HSI48: 48MHz on-chip RC oscillator, for USB crystal-less purpose

There is a 32MHz crystal inside of module for the STM32WB55 HSE (high-speed-external) clock source. And this 32MHz crystal has been fine-tuned by adjusting the STM32WB55 internal load capacitance at crystal terminals.

There is a 32.768KHz crystal inside of module for the STM32WB55 LSE (low-speed-external) clock source. And this LSE clock is clocked-out to LR1110 as for LR1110's real-time clock.

4 Power Supply of Module

4.1 VDD

The VDD is the main power supply for STM32WB55 ranging from 2.8(1) to 3.3V. And through a ferrite bead connected to LR1110 power supply. The 3.3V is limited by the GNSS LNA inside of module because the GNSS LNA is power and controlled by STM32WB55 GPIO.

The VDD power supply decoupling capacitors should follow to Figure 3: Decoupling of VDD. The capacitors should be placed as close as to the module pins. **Figure 4**: Placement of VDD decoupling capacitors.

1. When use USB function, the minimum VDD should be 3.0V. The STM32WB55xx USB functionality is ensured down to 2.7 V, but the full USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.

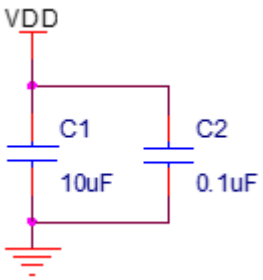


Figure 3: Decoupling of VDD

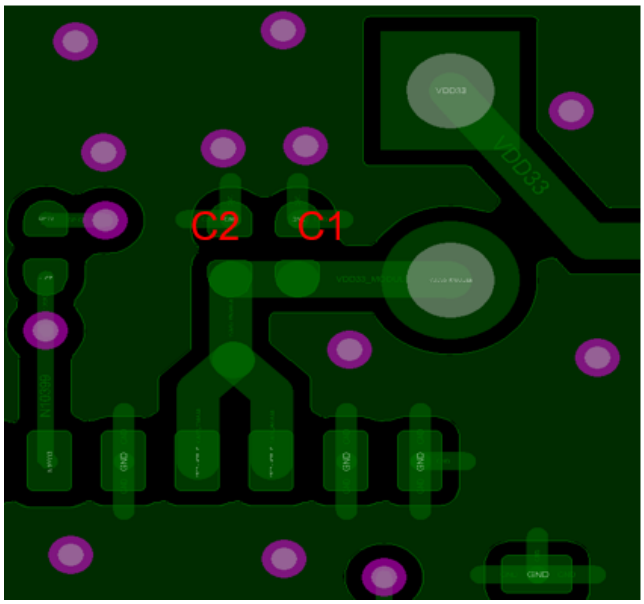


Figure 4: Placement of VDD decoupling capacitors

4.2 VDD_GNSS

The VDD_GNSS is the main power supply for MT3333 ranging from 2.8V to 4.3V. When you use battery for module power supply. It is recommended to use an external LDO to convert the battery to a 3.0~3.3V voltage source for this VDD_GNSS.

- The module pin35 EN_ VDD_GNSS can be used for the LDO enable control.

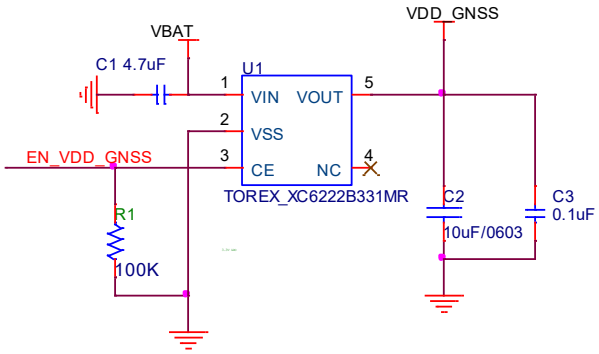


Figure 5: VDD_GNSS power supply Option 1

- The module pin35 EN_ VDD_GNSS can be used for load switch control.

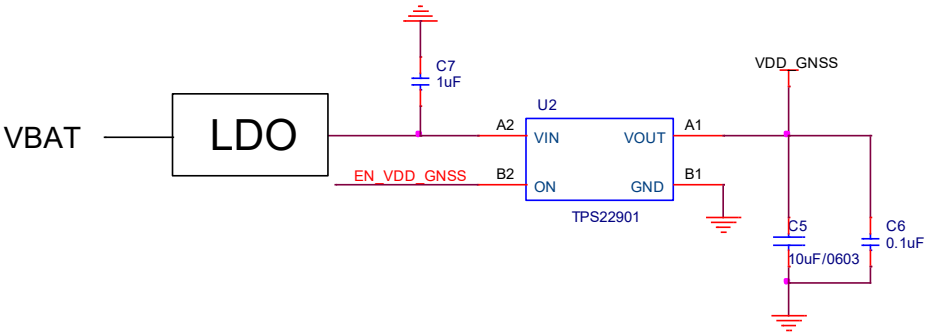


Figure 6: VDD_GNSS power supply Option 2

4.3 VDD_GNSS_BU

The VDD_GNSS_BU is the RTC power supply for MT3333 ranging from 2.0V to 4.3V. You can connect it to the module pin36 EN_VDD_GNSS_BU or an always-on source, like the battery. MT3333 RTC power and RTC clock should be kept on while the main power is closed for saving the aiding data and configuration data in RTC RAM. Thus, TTFF can be shorten at the next startup with these data.

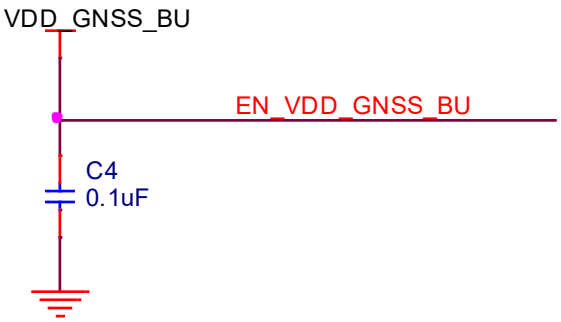


Figure 7: VDD_GNSS_BU power supply

5 NRST_MCU

This section describes the MCU reset function for Type 1WL-633.

NRST_MCU pin has a 0.1uF capacitor inside of module. No need external capacitor outside module. There are three types of MCU reset, namely:

- a system reset
- a power reset
- a backup domain reset

5.1 Power reset

A power reset is generated when one of the following events occurs:

1. a brown-out reset (BOR)
2. when exiting from Standby mode
3. when exiting from Shutdown mode

A brown-out reset, including power-on or power-down reset (POR/PDR), sets all registers to their reset values except the Backup domain.

When exiting Standby mode, all registers in the VCORE domain are set to their reset value. Registers outside the VCORE domain (RTC, WKUP, IWDG, and Standby/Shutdown modes control) are not impacted.

When exiting Shutdown mode, a Brown-out reset is generated, resetting all registers except those in the Backup domain.

5.2 System reset

A system reset sets all registers to their reset values except register (RCC_CSR) and the registers in the Backup domain.

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. Window watchdog event (WWDG reset)
3. Independent watchdog event (IWDG reset)
4. A software reset (SW reset)
5. Low-power mode security reset
6. Option byte loader reset
7. A brown-out reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

These sources act on the NRST pin and it is always kept low during the delay phase. The Cortex-M4 RESET service routine vector is selected via the BOOT0 and BOOT1.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

In case on an internal reset, the internal pull-up RPU is deactivated in order to save the power consumption through the pull-up resistor.

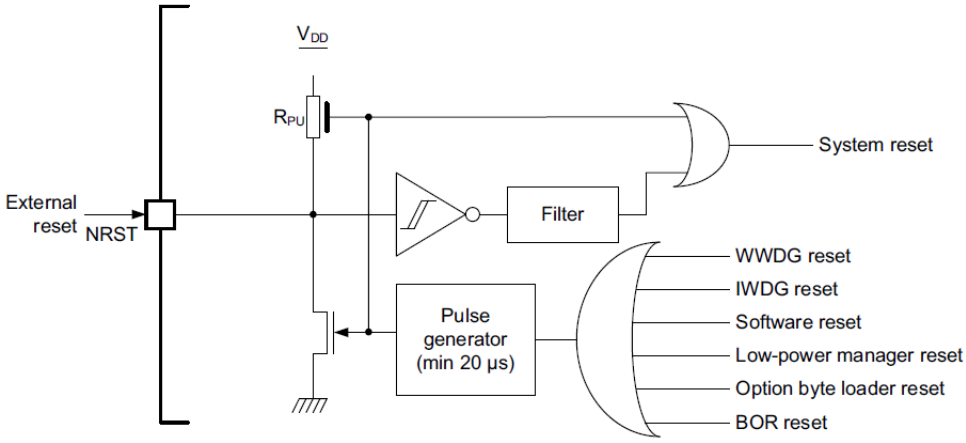


Figure 8 Simplified diagram of the STM32WB55 internal reset circuit

5.3 Backup domain reset

The backup domain has two specific resets.

A backup domain reset is generated when one of the following events occurs:

1. Software reset, triggered by setting the BDRST bit in the RCC backup domain control register (RCC_BDCR).

2. STM32WB55 VDD or VBAT power on, if both supplies have previously been powered off.

A backup domain reset only affects the LSE oscillator, the RTC, the Backup registers and the RCC Backup domain control register.

For more details, please refer to STM32WB55 data sheet and STMICRO RM0434 Reference manual.

6 GPIOs

This section describes the GPIOs function and features for Type 1WL-633.

6.1 GPIO Introduction

1WL-633 module has 10 GPIOs for general purpose use. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

Some interfaces like SWD, SPI can also be used as GPIOs depends on your design. Because all of them are duplicate usage. For example, if you do not use the SWCLK and SWDIO function for debug or download firmware, you can configure them to GPIOs or other function.

Each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR) and a 32-bit set/reset register (GPIOx_BSRR). In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL).

6.2 GPIO Main Features

- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O

- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_ BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers
- Fast toggle capable of changing every two clock cycles
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several
- peripheral functions

6.3 GPIO Functional Description

Subject to the specific hardware characteristics of each I/O port listed in the datasheet, each port bit of the general-purpose I/O (GPIO) ports can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain with pull-up or pull-down capability
- Output push-pull with pull-up or pull-down capability
- Alternate function push-pull with pull-up or pull-down capability
- Alternate function open-drain with pull-up or pull-down capability

Each I/O port bit is freely programmable; however, the I/O port registers must be accessed as 32-bit words, half-words or bytes. The purpose of the GPIOx_BSRR and GPIOx_BRR registers is to allow atomic read/modify accesses to any of the GPIOx_ODR registers. In this way, there is no risk of an IRQ occurring between the read and the modify access.

For more details, please refer to STM32WB55 data sheet and STMICRO RM0434 Reference manual.

Note: GPIO pins are to be left OPEN if not used.

6.4 GNSS_PPS

GNSS_PPS (Pulse Per Second) signal generated by the MT3333 GPS receiver provide an excellent relative accuracy clock which can be useful for synchronization between separate stations in the communications system or the measurement system.

7 Configuration Pins

This section describes the boot modes configuration for Type 1WL-633.

At start up, BOOT0 pin and BOOT1 option bit are used to select one of three boot options.

Table 2: Boot modes configuration

BOOT0 pin	BOOT1(1) option bit	BOOT modes
0	x	Boot from user flash
1	0	Boot from system memory
1	1	Boot from embedded SRAM

1. The BOOT1 value is the inverse value of the nBOOT1 User option

The values on both BOOT0 and BOOT1 are latched after a reset. It is up to the user to provide the correct value for the required boot mode.
The BOOT0 and BOOT1 are also re-sampled when exiting Standby mode. Consequently, they must be kept in the required boot mode. After the startup delay, the Cortex-M4 fetches the top-of-stack from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.
Depending on the selected boot mode, main Flash, system Flash, or SRAM1 memories are accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the Cortex-M4 boot memory space at address 0x0000 0000, and is also still accessible from its physical address 0x0800 0000. In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from System Flash memory: the system Flash memory is aliased in the Cortex-M4 boot memory space at address 0x0000 0000, and is also still accessible from its physical address 0x1FFF 0000.
- Boot from SRAM memory: the SRAM memory is aliased in the Cortex-M4 boot memory space at address 0x0000 0000, and is also still accessible from its physical address 0x2000 0000.

Embedded boot loader

The embedded boot loader is located in the system Flash memory, programmed by ST during production. It is used to program the Flash memory using one of the following device interfaces:

- USART1 on pins PA9 and PA10
- I2C1 on pins PB6 and PB7.
- I2C3 on pins PC0 and PC1

- SPI1 on pins PA4, PA5, PA6 and PA7
- SPI2 on pinsPB12, PB13, PB14 and PB15
- USB FS on pins PA11 and PA12.

For more details, please refer to STM32WB55 data sheet and STMICRO RM0434 Reference manual.

Note: Some interface GPIOs are internal used by module. You can refer to the module pin description in data sheet.

8 Power Sequence

This section describes the power sequences along with their parameters.

8.1 Power-On Sequence

- VDD must be good (90%) before assert NRST_MCU (= 0 to 1).

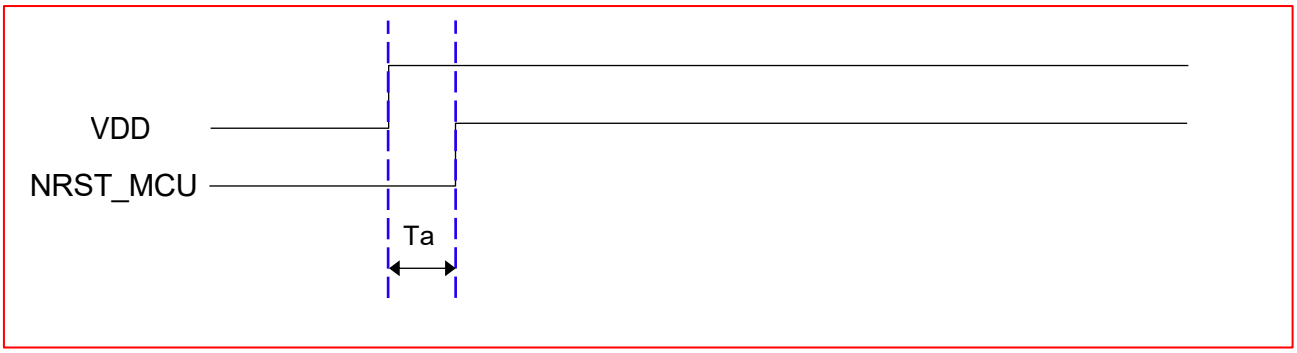


Figure 9: Power-On Sequence Graph

Table 3: Parameters for Power-On Sequence Graph

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Ta	VDD to NRST_MCU time	3.0			ms

8.2 Power-Off Sequence

- VDD should be off (10%) after assert NRST_MCU (= 1 to 0).

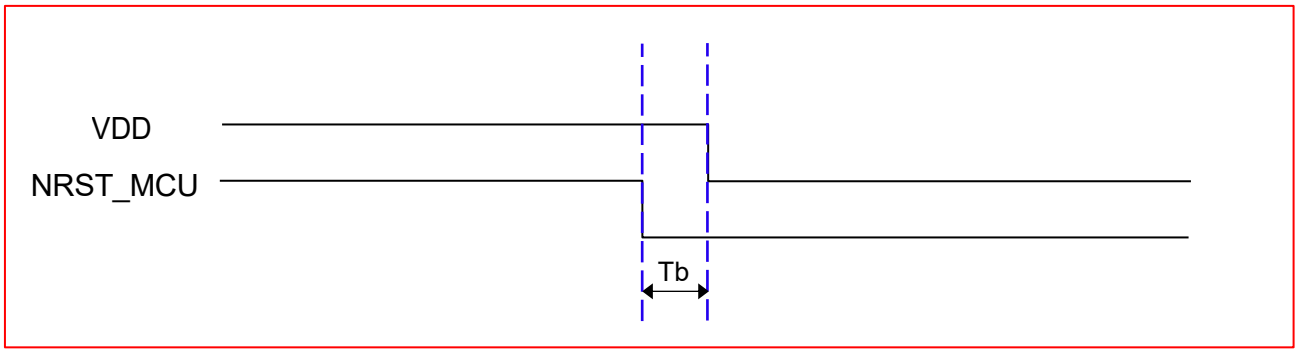


Figure 10: Power-Off Sequence Graph

Table 4: Parameters for Power-Off Sequence Graph

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Tb	NRST_MCU to VDD time	0			ms

9 Reference Design

This section describes the reference design for Type 1WL-633.

9.1 Reference Circuit

NRST_MCU pin has a 0.1uF capacitor inside of module. No need external capacitor outside module.

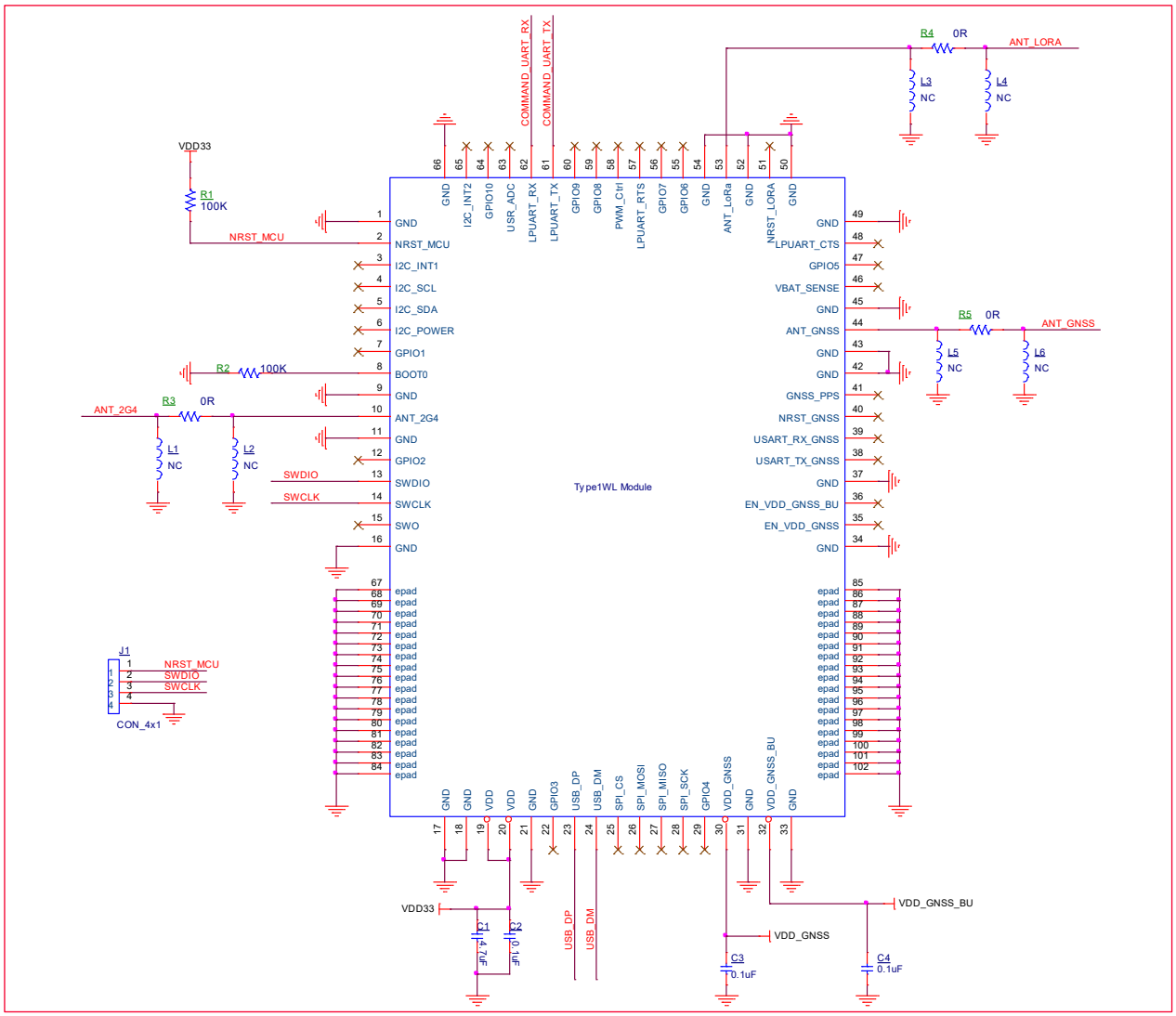


Figure 11: Reference Circuit

9.2 General Layout Guidelines

9.2.1 Power

Power traces do not produce any cycle for EMI consideration, even for different or the same layers.

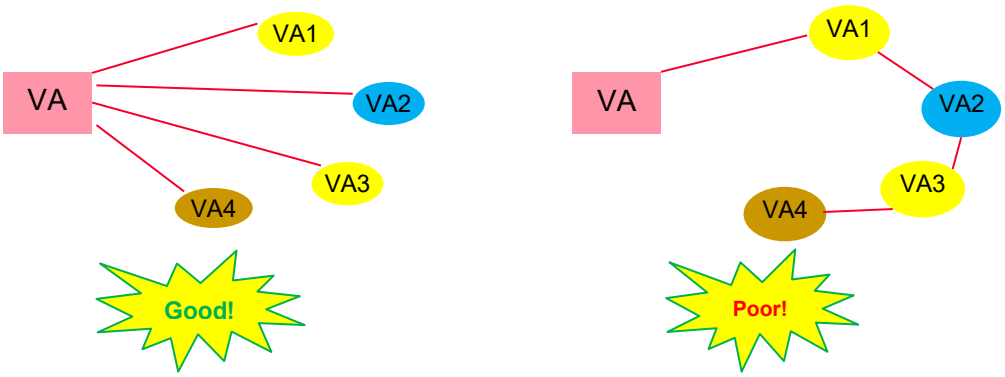


Figure 12: Power Supply Layout Topology

- The decoupling capacitors shall be placed close to the power pin.
- Make sure the power trace routes through the decoupling capacitor before being connected to power pins.
- Power traces shall be kept at low impedance and adequately added to the decoupling capacitor for noise filtering.
    - Add enough vias or larger vias for power connection when the power trace changes layer.
    - Keep the power trace as wide/short as possible.
- Make sure the width of power trace is proportional to the maximum current carried.
- When power traces overlap signal traces on adjacent layer beyond avoidance, the use of orthogonal cross is recommended.

9.2.2 Impedance

All RF traces have to execute the 50ohm impedance control and excellent GND shielding for good sensitivity.

9.2.3 RF

Set the RF path as short as possible to reduce the loss in RF signal transmission. Keep enough asymmetric GND vias around the RF trace and keep the antenna as far from the interference source as possible.

Reserve pi matching pads on RF trace in front of the antenna for matching tuning.

Routing RF traces on the surface layer which is far away from other high-speed signals trace is recommended. Any right-angle turn-in trace routing should be accomplished with an arc turn.

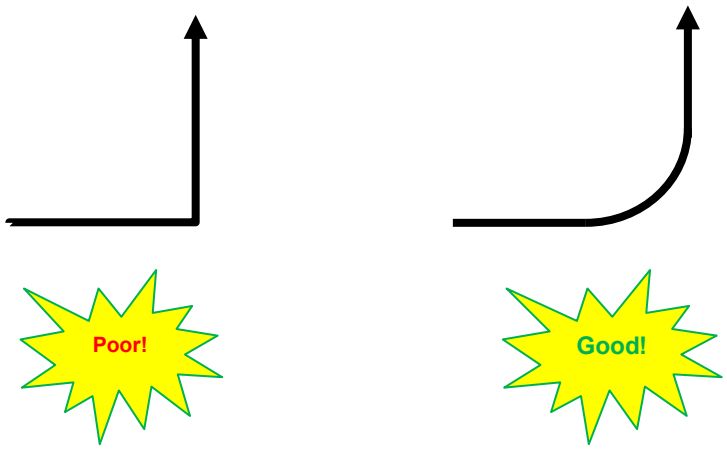


Figure 13: RF trace route principle

Avoid parallel inductor condition when impedance matching is done. Remove the crosshatched area of the GND plane underneath the matching component area to reduce the parasitic capacitance to easily meet 50ohm impedance control if necessary. If the RF connector or RF test point is used, remember to keep the impedance of its footprint at 50ohm.

9.2.4 High-Speed Digital Signals

- **USB:** DP/DM should be differential 90 Ω impedance. Keep USB trace as far from the interference source as possible.

9.3 Requirements for Unused Signals

No pull-up/down is necessary (floating) for these signals not used.

9.4 Module Footprint Design

Refer to dimensions in the Type 1WL-633 Datasheet. The DXF File of module footprint “type1wl_module_footprint_topview.dxf” is provided on the website.

9.5 Recommended Antennas

This module is certified with three types of antenna solution by regulatory certification body. To use Murata’s regulatory certification, any user must follow below instructions.

- Users should use recommended antennas only. However, any equivalent type of antenna with less antenna gains than the antenna gain of recommended antennas by Murata can also be used.

The recommended antennas with gains are described in **Table 5**.

Table 5: Recommended Antennas

P/N	Vendor	Form Factor	Frequency	Type	Gain	Actual Test Gain
ANT-SS900	LPRS	SMA, Whip/Stubby	868-915MHz	Omni-directional	2 dBi	0.4dBi@868MHz, 0.0dBi@915MHz
W1010	Pulse	SMA, Whip	2.4-2.5GHz	Omni-directional	2 dBi	1.7dBi@2484MHz
ABW007W10 (1)	Abeeway	SMA, Patch	1575.42MHz, 1598-1606MHz	RHCP	0.8 dBi	0.4dBi@1584.5MHz

2. The ABW007W10 is INPAQ ceramic antenna P/N:PA1590MS4G-102-1S (18x18x4mm) mounted in the middle of the ground plane PCB of 69.85mmx69.85mmx1.2mm. For detail, please refer to *ABW007W10_passive_GNSS_antenna.pdf*.

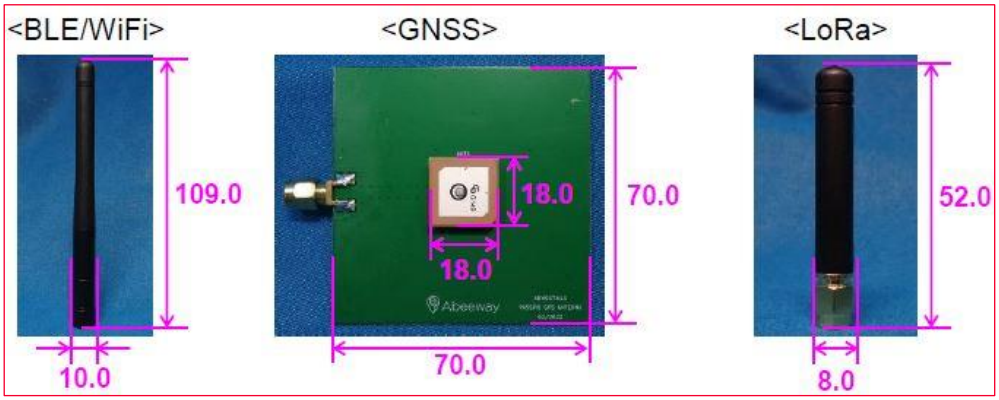


Figure 14: Murata Recommended Antennas

Figure 15: ***Antenna Performance Measurement Condition*** shows the Murata recommended antennas performance measurement condition.

Figure 14: shows the Murata recommended antennas performance measurement direction.

The antennas are connected to 1WL-633 Geolocation Module discovery kit via SMA connector.

Condition	Memo	Matching circuit		
		Shunt 1	Series	Shunt 2
Condition 1	LoRa	None	0ohm	None
	GNSS	None	0ohm	None
	BLE/WiFi	None	0ohm	None

Size:1005 LQG15HS / GRM15 / Resistor

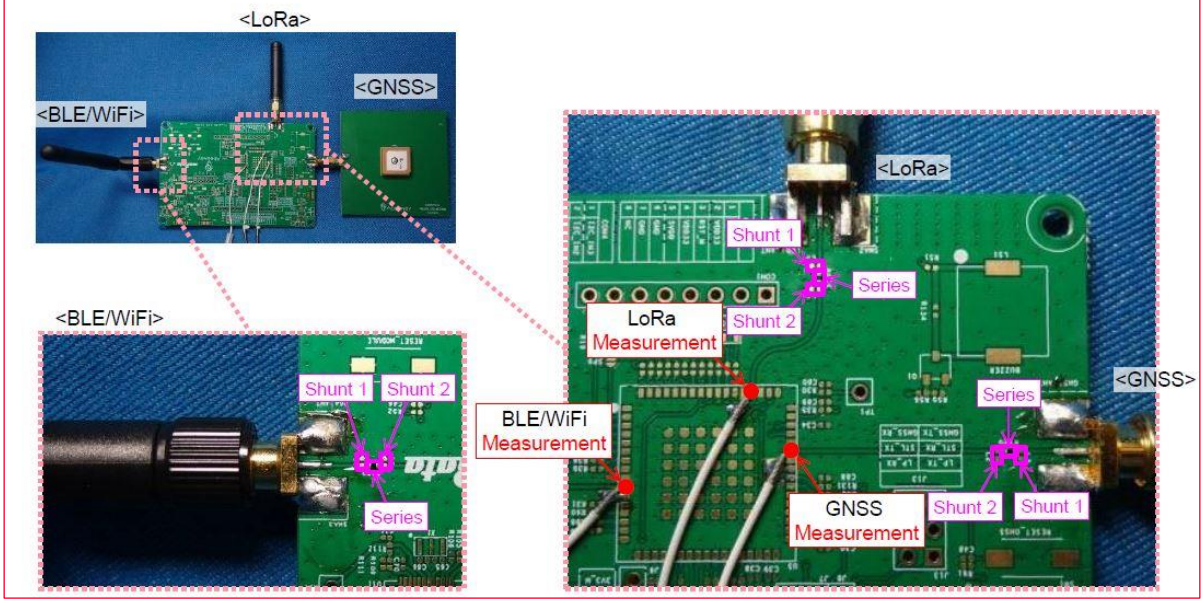


Figure 15: Antenna Performance Measurement Condition

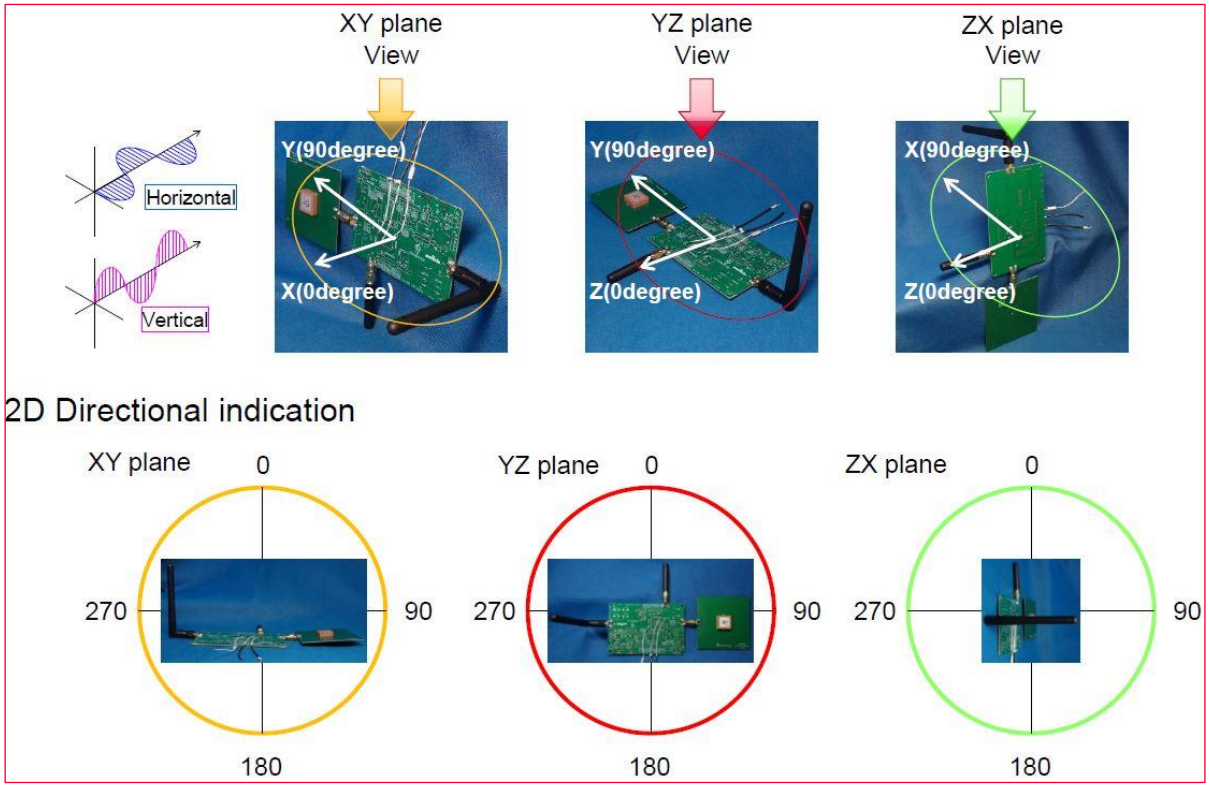
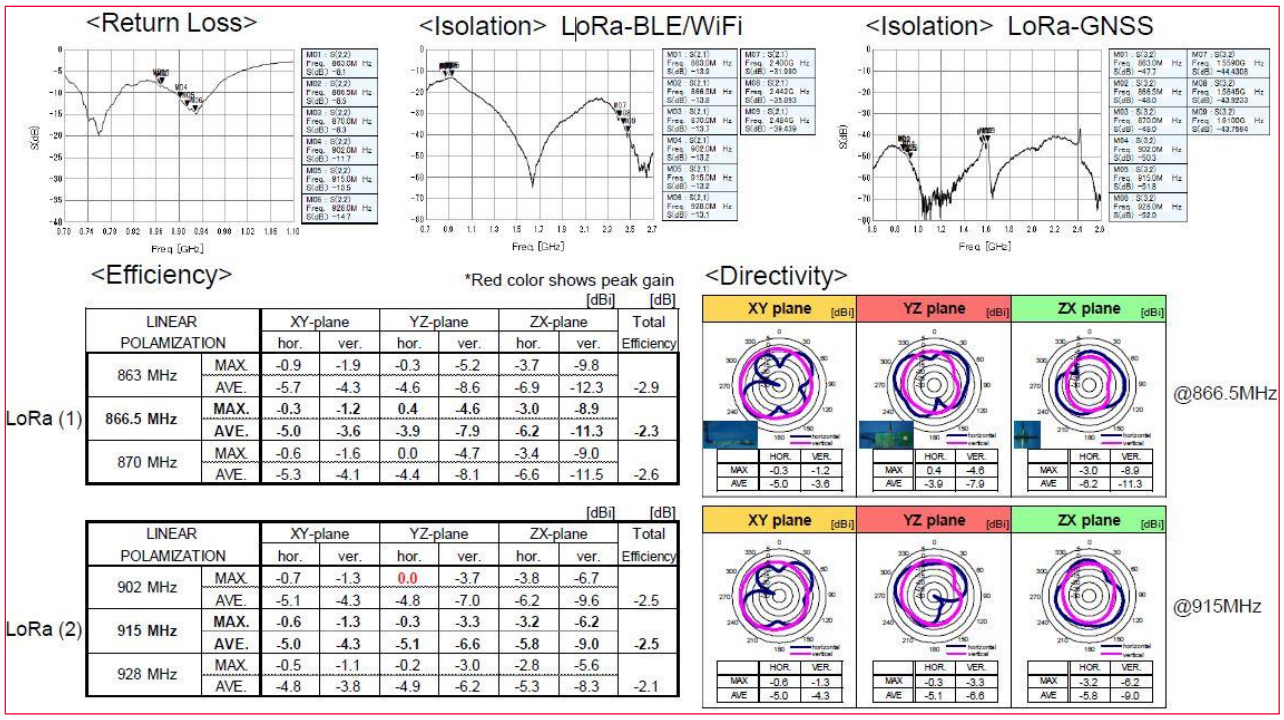


Figure 16: Antenna Performance Measurement Direction

9.5.1 LoRa Antenna



<Efficiency>

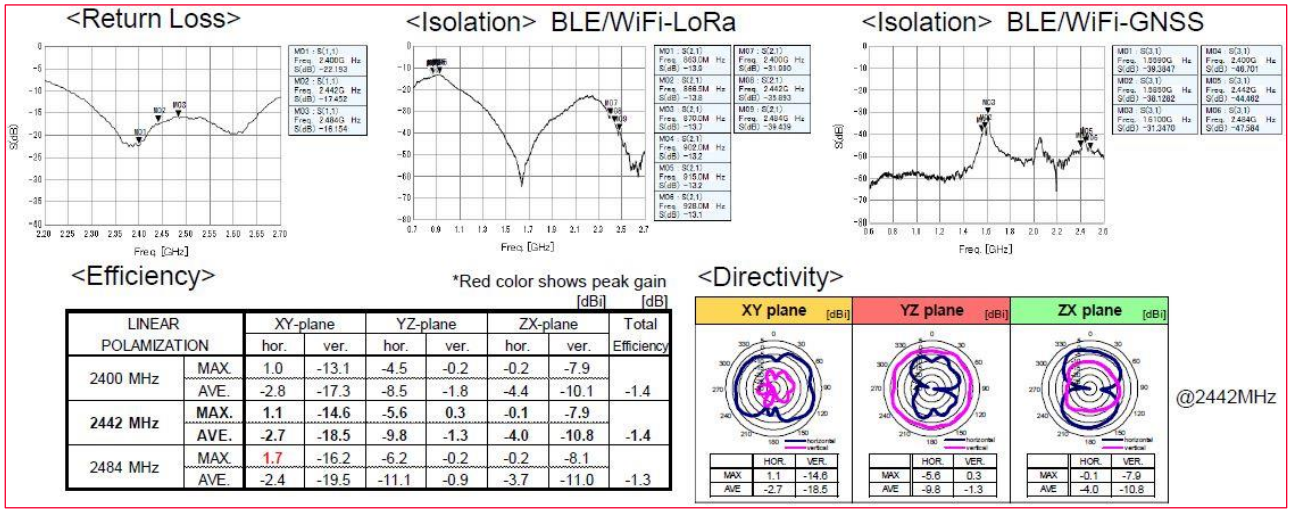
*Red color shows peak gain

	LINEAR POLAMIZATION		XY-plane [dBi] hor.	XY-plane [dBi] ver.	YZ-plane [dBi] hor.	YZ-plane [dBi] ver.	ZX-plane [dBi] hor.	ZX-plane [dBi] ver.	Total [dB] Efficiency
LoRa (1)	863 MHz	MAX.	-0.9	-1.9	-0.3	-5.2	-3.7	-9.8	
		AVE.	-5.7	-4.3	-4.6	-8.6	-6.9	-12.3	-2.9
	866.5 MHz	**MAX.**	**-0.3**	**-1.2**	**0.4**	**-4.6**	**-3.0**	**-8.9**	
		AVE.	**-5.0**	**-3.6**	**-3.9**	**-7.9**	**-6.2**	**-11.3**	**-2.3**
	870 MHz	MAX.	-0.6	-1.6	0.0	-4.7	-3.4	-9.0	
		AVE.	-5.3	-4.1	-4.4	-8.1	-6.6	-11.5	-2.6

	LINEAR POLAMIZATION		XY-plane [dBi] hor.	XY-plane [dBi] ver.	YZ-plane [dBi] hor.	YZ-plane [dBi] ver.	ZX-plane [dBi] hor.	ZX-plane [dBi] ver.	Total [dB] Efficiency
LoRa (2)	902 MHz	MAX.	-0.7	-1.3	0.0	-3.7	-3.8	-6.7	
		AVE.	-5.1	-4.3	-4.8	-7.0	-6.2	-9.6	-2.5
	915 MHz	**MAX.**	**-0.6**	**-1.3**	**-0.3**	**-3.3**	**-3.2**	**-6.2**	
		AVE.	**-5.0**	**-4.3**	**-5.1**	**-6.6**	**-5.8**	**-9.0**	**-2.5**
	928 MHz	MAX.	-0.5	-1.1	-0.2	-3.0	-2.8	-5.6	
		AVE.	-4.8	-3.8	-4.9	-6.2	-5.3	-8.3	-2.1

Figure 17: LoRa Antenna Measurement Result

9.5.2 BLE/Wi-Fi Antenna



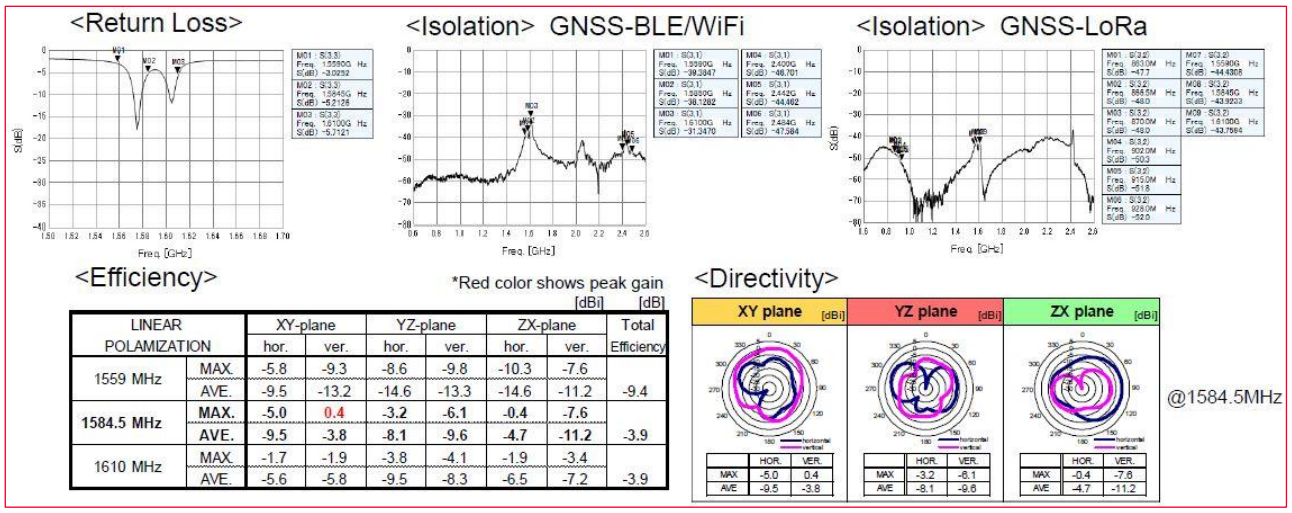
<Efficiency>

*Red color shows peak gain

	LINEAR POLAMIZATION		XY-plane [dBi] hor.	XY-plane [dBi] ver.	YZ-plane [dBi] hor.	YZ-plane [dBi] ver.	ZX-plane [dBi] hor.	ZX-plane [dBi] ver.	Total [dB] Efficiency
2400 MHz		MAX.	1.0	-13.1	-4.5	-0.2	-0.2	-7.9	
		AVE.	-2.8	-17.3	-8.5	-1.8	-4.4	-10.1	-1.4
2442 MHz		**MAX.**	**1.1**	**-14.6**	**-5.6**	**0.3**	**-0.1**	**-7.9**	
		AVE.	**-2.7**	**-18.5**	**-9.8**	**-1.3**	**-4.0**	**-10.8**	**-1.4**
2484 MHz		MAX.	1.7	-16.2	-6.2	-0.2	-0.2	-8.1	
		AVE.	-2.4	-19.5	-11.1	-0.9	-3.7	-11.0	-1.3

Figure 18: BLE/Wi-Fi Antenna Measurement Result

9.5.3 GNSS Antenna



LINEAR POLAMIZATION		XY-plane hor.	XY-plane ver.	YZ-plane hor.	YZ-plane ver.	ZX-plane hor.	ZX-plane ver.	Total Efficiency [dB]
1559 MHz	MAX.	-5.8	-9.3	-8.6	-9.8	-10.3	-7.6	
	AVE.	-9.5	-13.2	-14.6	-13.3	-14.6	-11.2	-9.4
1584.5 MHz	MAX.	-5.0	0.4	-3.2	-6.1	-0.4	-7.6	
	AVE.	-9.5	-3.8	-8.1	-9.6	-4.7	-11.2	-3.9
1610 MHz	MAX.	-1.7	-1.9	-3.8	-4.1	-1.9	-3.4	
	AVE.	-5.6	-5.8	-9.5	-8.3	-6.5	-7.2	-3.9

Figure 19: GNSS Antenna Measurement Result

GNSS antenna plays an important role in navigation devices. Poor GNSS antenna performance can affect GNSS time to first fixed (TTFF) and position accuracy, especially in poor environments.

Since SV signals are from the open sky, the upper hemisphere antenna gain pattern dominates the GNSS receiver performance. Several types of antennas such as PIFA, monopole antenna and IFA with poor upper hemisphere antenna gain pattern, which are not suitable for GNSS applications because their antenna gain pattern is sensitive to PCB ground dimension and mechanical metal components.

We recommend the right-hand circular polarization (RHCP) ceramic patch antenna due to its antenna gain pattern features, which are:

- Higher antenna directivity toward the front side
- Better radiation coverage in the upper hemisphere
- The polarization loss of RHCP ceramic patch antenna is smaller than that of linear polarization (LP) antenna
- Better resistance to multi-path
- Insensitive to metal components which are placed below the RHCP ceramic patch antenna

since the ceramic patch antenna has better radiation coverage in the upper hemisphere, placing the ceramic patch antenna toward the zenith is suitable for the GNSS receiver to receive SV signals.

Please make sure the metal does not overlap the ceramic patch antenna and place metal components or materials below the ceramic patch antenna.

- The antenna placement left-top and right-top corner are recommended.

- Keep GNSS antenna as far from the interference source as possible.
- Keep 50 Ω characteristic impedance of GNSS RF traces, shield it with GND plane nearby the trace and under the trace, place enough GND VIA along the RF trace, reserve pi matching pads on RF trace in front of the antenna for matching tuning.

There are two general contact methods for the patch antenna feeding to PCB.

- **Antenna metal holder contact:** This method is suitable and good for RHCP patch antenna performance. Larger contact area between the antenna metal holder and the PCB GND is recommended.
- **IPEX or Hirose coaxial cable contact:** This method is not suitable for smaller than 10x10x4 RHCP ceramic patch antenna since the coaxial cable grounding area is small. This method is only suitable for larger RHCP ceramic patch antenna.

10 Certification Configuration Information

This section has information about radio and Bluetooth certification.

10.1 Radio Certification Configuration

Table 6: Transmit Power Limit

Country	ID	Tx Power Limit
USA (FCC)	VPYLB1WL	LoRa: 22dBm setting; BLE: max power (setting 31)
Canada (ISED)	772C-LB1WL	LoRa: 22dBm setting; BLE: max power (setting 31)
Europe	EN 300328 V2.2.2, EN 300220-2 V3.2.1, EN 303413 V1.2.1 test report is prepared.	LoRa: 14dBm setting; BLE: max power (setting 31)
Japan	Certificate of Construction Type based on Japanese Radio Law. Ⓡ 218-220026	LoRa: 13dBm setting; BLE: max power (setting 31)

Table 7: Certified antennas

No.	Type	Vendor	Model	Peak Gain (dBi)
1	Patch	Abeeway	ABW007W10	0.4
2	Whip	LPRS	ANT-SS900	0.4 (868MHz) 0.0 (915MHz)
3	Whip	Pulse	W1010	1.7

10.2 Bluetooth Qualification Configuration

Bluetooth Tx power configuration script file should be loaded after Bluetooth device initialization.

- QDID: 202884
- Set Bluetooth Tx Power to Class 1.5.
- For PICS for supported Bluetooth functions refer to Bluetooth SIG site.

11 Reference Performance Data

This section describes the reference performance data for all DC/RF characteristics. **Figure 20: *Burst current definition*** shows the burst current definition for Type 1WL-633 module.

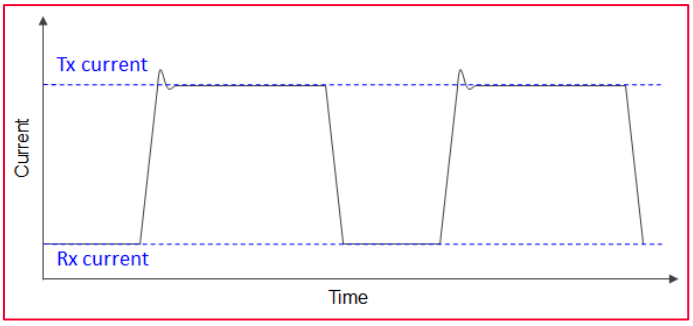


Figure 20: Burst current definition

Table 8: DC/RF Characteristics test Files

Characteristics	Filenames
LoRa	LR1110 firmware version 0x0308, aos-mfg-v1.4-3.elf
BLE	Wireless Firmware version (BLE STACK) 1.13.0, aos-mfg-v1.4-3.elf
Wi-Fi Passive Scan	LR1110 firmware version 0x0308, aos-mfg-v1.4-3.elf
LR1110 GNSS Scan	LR1110 firmware version 0x0308, aos-mfg-v1.4-3.elf
MT3333 GNSS	20190417_GENERAL_Module_AXN5.1.7_C33_SDK_11.bin, MTK_AllInOne_DA_MT3333_MP.bin

11.1 Sleep Current

Conditions: 25 °C, VDD = 3.3V, LR1110 firmware version 0x0308, Application FW: AT3.

Table 9: Sleep Current Specifications

Items	Condition	Contents			
Current Consumption		Minimum	Typical	Maximum	Unit

Items	Condition	Contents			
Supply current in sleep mode	MCU in stop2 mode with RTC, LR1110 and MT3333 OFF.		4.7		µA

11.2 DC/RF Characteristics for Sub-GHz

Conditions: 25 °C, VDD = 3.3V, LR1110 firmware version 0x0308, Application FW: 1.4-3.

Table 10: Sub-GHz Bands Receiver Specifications

Items	Condition	Contents			
Current Consumption		**Minimum**	**Typical**	**Maximum**	**Unit**
Supply current in receiver FSK mode	RxBoost OFF		15.4		mA
	RxBoost ON		17.5		mA
Supply current in receiver LoRa mode, RxBoost OFF	BW=125KHz, SF = 7		9.1		mA
	BW=125KHz, SF = 12		6.9		mA
	BW=250KHz, SF = 7		11.6		mA
	BW=250KHz, SF = 12		7.3		mA
	BW=500KHz, SF = 7		15.2		mA
	BW=500KHz, SF = 12		7.8		mA
Supply current in receiver LoRa mode, RxBoost ON	BW=125KHz, SF = 7		11.2		mA
	BW=125KHz, SF = 12		9.0		mA
	BW=250KHz, SF = 7		13.7		mA
	BW=250KHz, SF = 12		9.4		mA
	BW=500KHz, SF = 7		17.3		mA
	BW=500KHz, SF = 12		9.9		mA
Supply current in LoRa transmitter mode	LP PA 14dBm setting		28		mA
	HP PA 22dBm setting		115		mA
Tx Characteristics		**Minimum**	**Typical**	**Maximum**	**Unit**
TX Output Power	LP PA 14dBm setting	10.5	13.5		dBm
	HP PA 22dBm setting	18	21		dBm
RF Output Power Stability vs Voltage Supply (3.0~3.3V)	LP PA Operating		0.1		dB
	HP PA Operating		0.6		dB
RF Output Power Stability vs Temperature (-40~+85°C)	LP PA Operating		1.3		dB
	HP PA Operating		1.3		dB
TX Power Range	Programmable in steps of -1dB from maximum TX power		31		steps
Rx Characteristics		**Minimum**	**Typical**	**Maximum**	**Unit**
Sensitivity 2-FSK, RxBoost OFF	BRF = 4.8 kb/s, FDA = 5 kHz, BWF = 20 kHz		-116		dBm
Sensitivity 2-FSK, RxBoost ON	BRF = 4.8 kb/s, FDA = 5 kHz, BWF = 20 kHz		-117		dBm
Sensitivity LoRa, RxBoost OFF	BWL = 125 kHz, SF = 7		-125		
	BWL = 125 kHz, SF = 12		-139		

Items	Condition	Contents			
	BWL = 250 kHz, SF = 7		-122		
	BWL = 250 kHz, SF = 12		-136		
	BWL = 500 kHz, SF = 7		-118		
	BWL = 500 kHz, SF = 12		-132		
Sensitivity LoRa, RxBoost ON	BWL = 125 kHz, SF = 7		-127		
	BWL = 125 kHz, SF = 12		-141		
	BWL = 250 kHz, SF = 7		-124		
	BWL = 250 kHz, SF = 12		-138		
	BWL = 500 kHz, SF = 7		-120		
	BWL = 500 kHz, SF = 12		-134		

11.3 DC/RF Characteristics for Wi-Fi Passive Scanner

Conditions: 25 °C, VDD = 3.3V, LR1110 firmware version 0x0308, Application FW: 1.4-3.

Table 11: Wi-Fi Passive Scanner Specifications

Items	Condition	Contents			
Wi-Fi Passive Scan Characteristics		**Minimum**	**Typical**	**Maximum**	**Unit**
RX input frequency	Wi-Fi channels	2412	-	2484	MHz
Supply Current in Wi-Fi scan mode	Preamble detect phase		13.6		mA
	Capture phase		12		mA
	Processing phase		4		mA
Wi-Fi sensitivity for Wi-Fi 802.11 b, DSSS	DBPSK, DR = 1Mb/s		-93		dBm
Wi-Fi sensitivity for Wi-Fi 802.11 g, OFDM, 20MHz channel spacing	BPSK, CR = 1/2, DR = 6 Mb/s		-88		dBm
Wi-Fi sensitivity for Wi-Fi 802.11 n, OFDM, 20MHz channel spacing, short guard interval	BPSK, CR = 1/2, DR = 7.2 Mb/s		-86		dBm

11.4 DC/RF Characteristics for Bluetooth Low Energy

Items	Contents
Bluetooth specification (power class)	Version 5.2 (LE)
Channel frequency (spacing)	2402 to 2480 MHz (2 MHz)
Number of RF Channel	40

11.4.1 1 Mbps PHY Condition

Conditions: 25 °C, VDD = 3.3V, BLE STACK FW: 1.13.0, Application FW: 1.4-3.

Table 12: BLE 1 Mbps PHY Specifications

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode, Max output power		20.8		mA
• Rx mode		13.5		mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Max Output power		5		dBm
In-band emission				
• f_{TX}+/-2 MHz			-20	dBm
• f_{TX}+/-[3+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Stable Modulation Characteristics				
• $\Delta f1_{avg}$	247.5		252.5	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier frequency offset and drift				
• Frequency offset (f_n); n = 0,1,2,3…k	-150		150	kHz
• Frequency drift ($\|f_0-f_n\|$); n = 2,3,4…k			50	kHz
• Drift rate				
• $\|f_1-f_0\|$			20	kHz
• $\|f_n-f_{n-5}\|$; n = 6,7, 8,…k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-93	-70	dBm
Maximum input signal level (PER < 30.8%)	0			dBm

Items	Contents			
PER Report Integrity (-30 dBm input)	50		65.4	%

11.4.2 2 Mbps PHY Condition

Conditions: 25 °C, VDD = 3.3V, BLE STACK FW: 1.13.0, Application FW: 1.4-3.

Table 13: BLE 2 Mbps PHY Specifications

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode, Max output power		20.8		mA
• Rx mode		14.1		mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Max Output power		5		dBm
In-band emission				
• f_{TX}+/-4 MHz			-20	dBm
• f_{TX}+/-5 MHz			-20	dBm
• f_{TX}+/-[6+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	450		550	kHz
• $\Delta f2_{max}$ (at 99.9%)	370			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			-
Stable Modulation Characteristics				
• $\Delta f1_{avg}$	495		505	kHz
• $\Delta f2_{max}$ (at 99.9%)	370			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier frequency offset and drift				
• Frequency offset (f_n); n = 0,1,2,3…k	-150		150	kHz
• Frequency drift ($\|f_0-f_n\|$); n = 2,3,4…k			50	kHz
• Drift rate				
◦ $\|f_1-f_0\|$			20	kHz
◦ $\|f_n-f_{n-5}\|$; n = 6,7, 8,…k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm

Items	Contents			
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-90	-70	dBm
Maximum input signal level (PER < 30.8%)	0			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

11.5 DC/RF Characteristics for GNSS

11.5.1 LR1110 GNSS Scanner Receiver Specification

Conditions: 25 °C, VDD = 3.3V, LR1110 firmware version 0x0308, Application FW: 1.4-3.

Table 14: LR1110 GNSS Scanner Receiver Specifications

Items	Condition	Contents			
Current Consumption		**Minimum**	**Typical**	**Maximum**	**Unit**
Supply current in GNSS scan mode	Capture phase		15.2		mA
	Processing phase		6.3		mA
RX input frequency	GPS		1575.42		MHz
	BeiDou		1561.1		MHz
GNSS sensitivity	GPS, indoor classification, and strong signal SV capture		-133		dBm
	BeiDou, strong signal SV capture		-130		dBm

11.5.2 MT3333 GNSS Receiver Specification

Conditions: 25 °C, VDD_GNSS = 3.3V, VDD_GNSS_BU = 3.3V, MT3333 FW Version: 5.1.7. All sensitivity tests use GPS only constellation, Spirent signal generator and are calibrated to take into account the attenuation of cabling.

Table 15: MT3333 GNSS Receiver Specifications

Items	Condition	Contents			
Current Consumption		**Minimum**	**Typical**	**Maximum**	**Unit**
Supply current	Capture phase (in GPS mode)		29		mA
	Tracking phase (in GPS mode)		15.5		mA
RX input frequency	GPS		1575.42		MHz
	BeiDou		1561.1		MHz
GNSS sensitivity	Tracking		-156		dBm

Items	Condition	Contents			
	Acquisition hot		-156		dBm
	Acquisition cold		-146		dBm
TTFF (Time to first fix)	Hot start, -130dBm		1.6		sec
	Hot start, -140dBm		2.6		sec
	Hot start, -150dBm		13.2		sec
	Full cold start, -130dBm		31		sec
	Full cold start, -140dBm		41		sec
Accuracy -140dBm (10mins)	3D RMS		<10		m

12 Internal Connection

Below tables or pictures the internal truth table of LoRa,GNSS and 2.4G radio, also the internal connection between LR1110, MT3333 and STM32WB55.

Table 16 LoRa Truth Table

LoRa Truth Table

	LR1110_DIO5	LR1110_DIO6	LR1110_DIO7
RFO_HP	H	L	L
RFO_LP	L	H	L
RFI	L	L	H

Table 17 GNSS Truth Table

GNSS Truth Table

	STM32WB55_PB1	STM32WB55_PE3
MT3333	H	L
LR1110	L	H

Table 18 2.4G Truth Table

2,4G Truth Table

	STM32WB55_PB2	STM32WB55_PA3
WiFi Scan	H	L
BLE	L	H

Table 19 Internal Connection Between LR1110 and STM32WB55

Internal Connection Between LR1110 and STM32WB55

LR1110	STM32WB55	Function
DIO0	PC8	LR_BUSY
DIO1	PA4	LR_NSS
DIO2	PA5	LR_SCK
DIO3	PA7	LR_MOSI
DIO4	PA6	LR_MISO
DIO9	PC1	LR_DIO9

DIO11	PA2	ST_LSCO_32K
NRESET	PB5	LR_NRST

Table 20 Internal Connection Between MT3333 and STM32WB55

Internal Connection Between MT3333 and STM32WB55

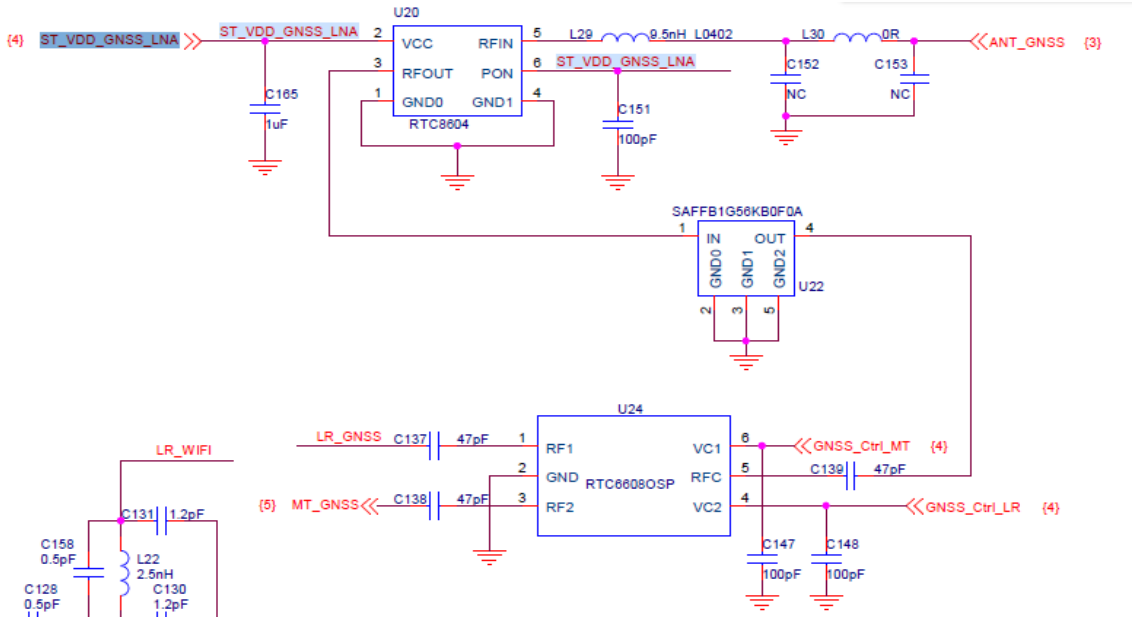
MT3333	STM32WB55	Function
HRST_B	PE4	NRST_GNSS
RX0	PA9	USART_RX_GNSS
TX0	PA10	USART_TX_GNSS
GIO7	PB15	GNSS_PPS
FORCE_ON	PC12	GNSS_FORCE_ON

Table 21 GNSS LNA Control

GNSS LNA Control

GNSS LNA	STM32WB55
GNSS LNA_VCC	STM32WB55_PB0
GNSS LNA_PON	STM32WB55_PB0

Figure 21 GNSS LNA Control



13 Device Address of STM32WB55

13.1 Device Address of STM32WB55

STM32WB55 devices support public and random (static or private) addresses (BLE address). Device addresses can be public or random, both are 48-bits long, and denoted as colon-delimited hex values (e.g. AA:BB:CC:DD:EE:FF).

The public device address must conform with the IEEE 802-2001 standard, using a valid

organization unique identifier (OUI) obtained from the IEEE registration authority. Public device addresses are known as MAC addresses.

Customers willing to develop their own products (based on public device addresses) must obtain from the IEEE Registration Authority their own IEEE-assigned 48-bit universal BLE MAC address, and not use the one already assigned to STM32WB55, as the default device address may duplicate.

If the application needs to use a different public address, it must be obtained from the right organization, and then stored in a persistent memory location of the final product (either within the microcontroller flash memory/OTP, or in an external storage area).

For details, please refer to ST application note AN5289 Rev17

13.2 Device Address in Type 1WL-633 module

There is no universal Bluetooth MAC address obtained from the IEEE registration authority preprogrammed in Type 1WL-633 module.

The module user should handle the address of its final product according to the guidelines aforementioned.

14 References

Table 22 Reference Table reviews all the key reference documents that the user may like to refer to.

Table 22 Reference Table

Support Site	Notes
Murata Type 1WL-633 Module Datasheet	Type 1WL-633 Datasheet_Rev E.pdf
Murata Type 1WL-633 Module Footprint	type1wl_module_footprint_topview.dxf

15 Technical Support Contacts

Table 23 List of Support Resources lists all the support resources available for the Murata LoRa solution**.**

Table 23 List of Support Resources

Support Site	Notes
Murata Community Forum	**Primary support point for technical queries.** This is an open forum for all customers. Registration is required.

Revision History

Revision Code	Date	Changed Item	Comment
	2023.08.09	First version	
A	2023.08.19	Added 4.2 VDD_GNSS power supply option 2 Added 6.4 GNSS_PPS information. Updated 11.1 sleep current. Updated 11.3 Wi-Fi scan current. Updated 11.4 BLE TX current. Updated 11.5.1 LR1110 GNSS scan current. Updated 11.5.2 MT3333 GNSS current.	Update
B	2023.11.17	Updated 4.1 VDD supply range.	Update
C	2024.5.22	Added the internal connection inside module	Update
D	2024.8.20	Added Section 13 for Bluetooth Device Address declaration.	Update
E	2025.11.27	Added the module certified antenna information in 10.1. Corrected typos.	Update

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