Hardware Design Guide

Type 2GT Hardware Application Note

Semtech LR1121 Chipset for LoRa

- Design Name: Type 2GT
- P/N: LBAA0XV2GT-001

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About This Document

Murata's Type 2GT is a small and high-performance module based on Semtech LR1121 chipset, supporting LoRa. This application note provides RF and hardware design guidance.

Refer to Type 2GT datasheet for module specification.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product. In particular, RF, hardware, systems, and software engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert→Tables→Quick Tables→Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Embedded Artists AB Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This document describes the design recommendation for schematic diagrams, printed circuit board (PCB), and also provides the hardware design guide for the Murata Type 2GT module.

2 Intended Audience

This document is intended for:

- Technical support personnel
- Board hardware engineer
- Software engineer

3 Related Documents

- Type 2GT Datasheet
- UM.LR1121.W.APP
- DS.LR1121.W.APP

4 Clock circuit

4.1 TCXO

There is a 32MHz TCXO for the LR1121 IC inside the module. The 32MHz TCXO is powered by VTCXO of LR1121 IC internally.

4.2 LSE

There is an LSE 32.768kHz crystal for LR1121 IC inside the module.

5 Power supply of the module

There is one input power supply on the module.

VDD: Power supply for the LR1121 IC inside the module

The power supplied decoupling capacitors should follow to Figure 1. The capacitors should be placed as close as to the module pins. Figure 2 is an example.

Figure 1: Decoupling capacitors of Power

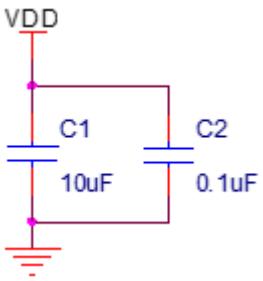
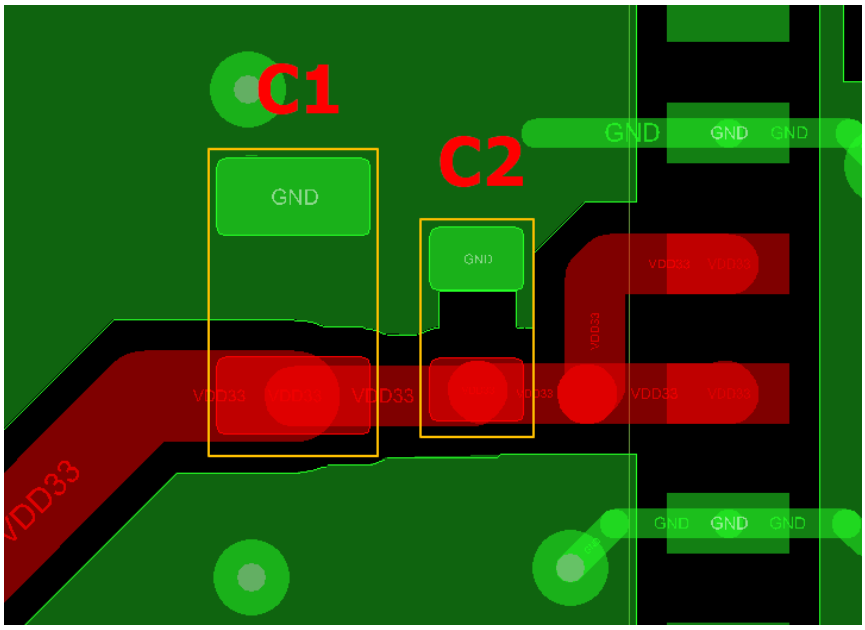


Figure 2: Placement of Decoupling capacitors



6 ANT ports

The ANT ports are the RF path of LoRa sub_G band and 2.4G ISM band signals. The port impedance is designed as about 50 ohm. So when customer connects the port to SMA port or antenna using RF trace, make sure the RF trace impedance is about 50 ohm. The RF trace can be stripe line or co-plane mode. It is better to add some PI type matching components on the trace. In case of mismatch, the impedance can be compensated by the matching circuit.

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7 GPIOs

The 2GT module used 11 digital IOs of LR1121:

- LR1121:DIO0 is used as BUSY signaling, and it is mandatory to properly handle the host controller interface. The signal is connected to the module pin.
- LR1121:DIO1 to DIO4 are dedicated to the SPI interface signals NSS, SCK, MOSI and MISO respectively. These signals are connected to the module pins.
- LR1121:DIO5, DIO6, DIO7 are used to control RF switches in the module. These signals are connected to the module pins.
- LR1121:DIO9 is dedicated to the LR1121 interrupts. It is recommended to connect DIO9 to the host controller for the lowest-power applications. The signal is connected to the module pin.
- LR1121: NRESET allows to cancel on-going functions of the LR1121, and reset all HW and FW. Although a device restart is also possible through host controller commands, it is recommended to allow the host controller to control this signal. The signal is connected to the module pin.

Table 2: Relation between module pins and LR1121 GPIOs

2GT module pin number	2GT module pin name	LR1121 pin
1	DIO9	DIO9
2	DIO8	DIO8
9	LR_BUSY	DIO0
10	LR_NSS	DIO1
11	LR_MISO	DIO4
12	LR_MOSI	DIO3
13	LR_SCK	DIO2
23	RFSW0	DIO5
24	RFSW1	DIO6
25	RFSW2	DIO7
35	LR_NRST	NRESET

8 DC-DC regulator and LDO regulator mode

8.1 Selecting DC-DC Converter or LDO Regulation

Two forms of voltage regulation (DC-DC buck regulator or linear LDO regulator) are available depending upon the design priorities of the application. These LDO and DC-DC be selected to used in the chip core.

Beside it, the LDO and DC-DC are also related with the PA regulator in LR1121.

The PA regulator (Reg_PA) in LR1121 is used to supply of both the Low Power PA and the High Power PA.

The PA regulator is internally connected to the DC-DC /LDO output for the Low Power PA, allowing a +15dBm operation in both DCDC or LDO configurations.

But when the power is high than 15dBm, PA regulator must be configured to connect to VBAT_RF (VDD pin on 2GT module).

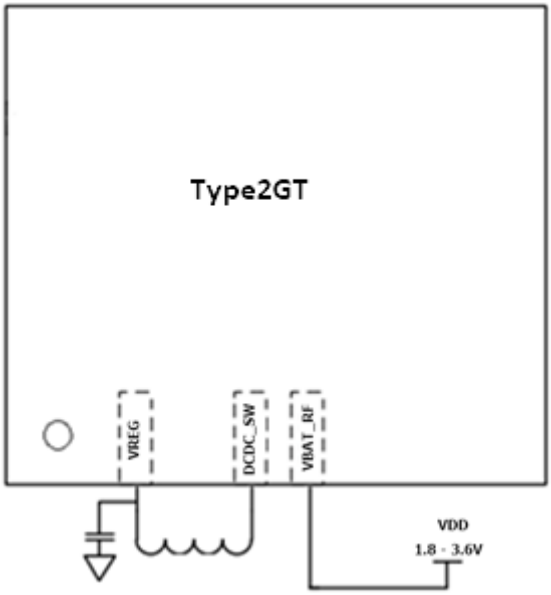
Table 3: Regulation Type versus Circuit Mode

Circuit Mode	Sleep	STDBY_RC	STDBY_XOSC	FS	Rx	Tx
Regulator Type = 0	-	LDO	LDO	LDO	LDO	LDO
Regulator Type = 1	-	LDO	DC-DC + LDO	DC-DC + LDO	DC-DC + LDO	DC-DC + LDO

8.2 2GT with DC-DC Regulator Option

Advantage of this option: The power consumption of the core is reduced. And power consumption of the Tx power (power value is under 15dBm) is smaller compared with LDO mode.
Note: Regulator Mode register value should be set as 0x01 under DC-DC Regulator mode.

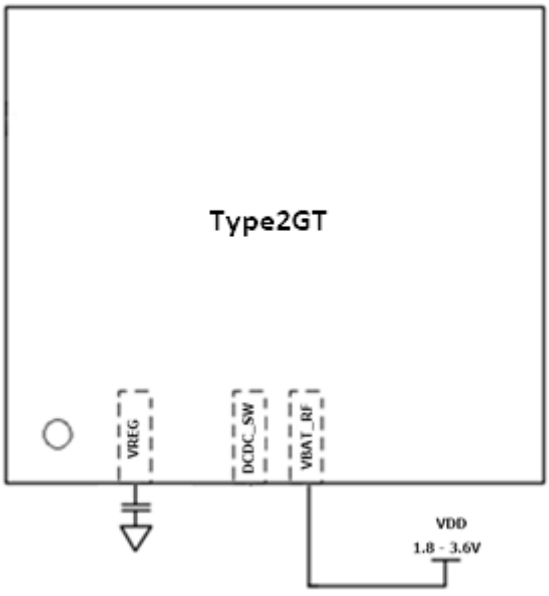
Figure 3: 2GT with DC-DC Regulator Option



8.3 2GT with LDO Regulator Option

The LDO Regulator is used. Power consumption is higher than in DC-DC regulator. Advantage of this option: The cost and space for an external 15 μH inductor are spared.

Figure 4: 2GT with LDO Regulator Option



Note: **Regulator Mode register value should be set as 0x00 under LDO Regulator mode.**

9 Module regulatory compliance information

9.1 CE

This module has been assessed to conform to the essential requirements of Article 3.2 of the 2014/53/EU Radio Equipment Directive.

The assessment reports in accordance with the following standards are available.

ETSI EN 300220-1 V3.1.1 (2017-02)

ETSI EN 300220-2 V3.2.1 (2018-06)

ETSI EN 300440 V2.2.1 (2018-07)

The antennas associated with this module to illustrate the radiated conformity are listed below.

Table 4: CE assessed sub-GHz LoRa antenna

No.	Model	Vendor	Type	Peak Gain (dBi)
1	001-0028	TE	Dipole, Whip	2.0

Table 5: CE assessed 2.4GHz LoRa antenna

No.	Model	Vendor	Type	Peak Gain (dBi)
1	ANT-DB1-RAF-RPS	Linx	Dipole, Whip	2.5

9.2 FCC/ISED

This module has been certified as a single-modular transmitter with the following certification IDs.

FCC ID: VPYLB2GT

IC: 772C-LB2GT

The certified antennas are listed below.

Table 6: FCC/ISED certified sub-GHz LoRa antennas

No.	Model	Vendor	Type	Peak Gain (dBi)
1	001-0002	TE	Dipole, Whip	2.0
2	2195835-1/2/3/4	TE	Monopole, FPC	2.1

Table 7: FCC/ISED certified 2.4GHz LoRa antenna

No.	Model	Vendor	Type	Peak Gain (dBi)
1	ANT-DB1-RAF-RPS	Linx	Dipole, Whip	2.5

9.3 MIC

This module has obtained the Construction Design Certification in accordance with the Radio Act in Japan with the following certification number.

R 218-230222

The registered antennas are listed below.

Table 8: MIC registered sub-GHz LoRa antennas

No.	Model	Vendor	Type	Peak Gain (dBi)
1	001-0002	TE	Whip	2.0
2	ANT-SS900	LRPS	Whip	2.0
3	FXP895.07.0200C	Taoglas	FPC	2.83
4	PC91.07.0100A.db	Taoglas	PCB	2.67
5	ILA.09	Taoglas	Chip	1.57
6	ILA.01	Taoglas	Chip	1.37
7	FXP290.07.0100A	Taoglas	FPC	1.5
8	FXP890.07.0100C	Taoglas	FPC	-0.06
9	TI.93.A111	Taoglas	Whip	2.06

10	TI.92.2113	Taoglas	Whip	2.14
11	TI.09.A.0111	Taoglas	Whip	2.17
12	TLS.90.205111	Taoglas	Module	2.46
13	IS.05.B.301111	Taoglas	Module	2.75
14	M620720	Kyocera AVX	Chip	2.06
15	T13-047-1038	Staff	Whip	2.19
16	T13-047-1040	Staff	Whip	2.19
17	T18-078-1127	Staff	Module	-0.45
18	T18-079-1128	Staff	Module	-2.68
19	T18-018-1098	Staff	Sheet Metal	2.07
20	T16-068-1037	Staff	Whip	1.27
21	T16-068-1021	Staff	Whip	1.61
22	T18-023-1095	Staff	PCB	2.69
23	T16-062-1094	Staff	PCB	-0.98
24	T18-051-1142	Staff	FPC	2.30
25	T22-014-1253	Staff	PCB	1.63
26	T22-007-1230	Staff	PCB	2.30
27	PC91.07.175AO.db.jsr	Taoglas	FPC	0.52
28	T17-058-1069	Staff	Whip	1.21
29	T17-058-1070	Staff	Whip	-0.35
30	T18-037-1116	Staff	PCB	1.88
31	T18-051-1120	Staff	FPC	1.57
32	T18-051-1117	Staff	FPC	1.80
33	T13-023-1043	Staff	FPC	2.18
34	T16-062-1015	Staff	FPC	-7.64
35	T16-062-1022	Staff	PCB	0.16
36	T18-051-1141	Staff	FPC	2.04

37	T18-051-1143	Staff	FPC	1.58
38	T13-047-1039	Staff	Whip	1.79
39	T13-047-1041	Staff	Whip	0.95
40	T15-030-1042	Staff	Whip	2.39
41	T20-030-1184	Staff	Whip	-1.68
42	T18-049-1129	Staff	Module	-0.04
43	T25-030-1295	Staff	Module	-0.18

Table 9: MIC registered 2.4GHz LoRa antennas

No.	Model	Vendor	Type	Peak Gain (dBi)
1	ANT-DB1-RAF-RPS	Linx	Whip	2.5
2	W1010	Pulse Electronics	Whip	2.0
3	GW.15.2113	Taoglas	Whip	2.0
4	PCS.25.A	Taoglas	Chip	2.0
5	WLA.04	Taoglas	Chip	0.5

10 Appendix

The connection information between LR1121 IC and RF switch inside the module is important for the software design.

10.1 Connection of LR1121 IC and RF switch

Table 10: Connection between LR1121 IC and RF switch

LR1121			RF switch	
Pin	Name		Pin	Name
25	DIO5	-----	3	V1

24	DIO6	-----	6	V2
23	DIO7	-----	7	V3

10.2 Relation between the module LoRa operation mode in sub_G and LR1121 IC pin status

Table 11: Relation between the module operation mode in sub_G and LR1121 IC pin status

LoRa sub_G band work mode	LR1121 IC pin DIO5	LR1121 IC pin DIO6	LR1121 IC pin DIO7
Standby	0	0	0
LoRa Rx	0	0	1
LoRa Tx	0	1	0
LoRa Tx_High power	1	0	0

Revision History

Issued Date	Revision Code	Changed Items
2023/07/18	A	Initial Release
2024/01/17	B	Change the document format
2024/08/23	C	Corrected typos
2025/11/27	D	Add section 9 of the module regulatory compliance information
2026/04/27	E	Add 17 new MIC certified sub_G antennas in section 9 of the module regulatory compliance information

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This document might include technical inaccuracies or other errors. Corrections and improvements might be incorporated in a new version of the document.