LBUA5QJ2AB (Type2AB) Hardware Design Guide

Revision History

Issued Date	Revision Code	Changed Items
2021/4/7	**A**	Initial version
2021/5/10	**B**	1. Temperature and voltage measurement 2. PCB design 3. Antenna design
2022/2/14	**C**	1. correct table No on Interface 2. I2C Interface
2023/8/4	**D**	1. Update the links of reference documents 2. Update 6.1 UWB Antenna Design
2023/9/12	**E**	1. Add 4.3 Detectable direction of 3-Axis accelerometer 2. Update Voltage and Temperature Measurement 3. Update Jolie antenna picture 4. Add LNA reference design 5. Add calibration guide

This document is provided “as is” without warranty.
This document might include technical inaccuracies or other errors. Corrections and improvements might be incorporated in new version of the document.

Content

Tables

Figures

About this document

Scope

This document describes the design recommendations and guidelines for the schematic diagrams, printed circuit board (PCB) and some other hardware designs based on Murata Type2AB UWB module.

Intended Audience

This document is intended for:

- Technical support person
- Board hardware engineer
- Software engineer

Reference Documents

[1] Qorvo QM33120W Datasheet, Rev.C, 06/2022

[2] Qorvo QM33100 User Manual, Rev.A, 08/2022

[3] Nordic nRF52840 Product Specification v1.7, 2021-11-30

[4] Murata SP-2AB_UWB+BLE combo module datasheet, Rev.F,09/2023

[5] Murata LBUA5QJ2AB UWB Module Antenna Specification, Rev.3, 09/2023

[6] Qorvo Production Tests for DW3000-Based Products (Application Note APS312), RevA, 06/2021

1. Clock Circuit

1.1 Crystal

There are three embedded crystals inside the module.

- 38.4MHz crystal for Qorvo UWB IC QM33120W.

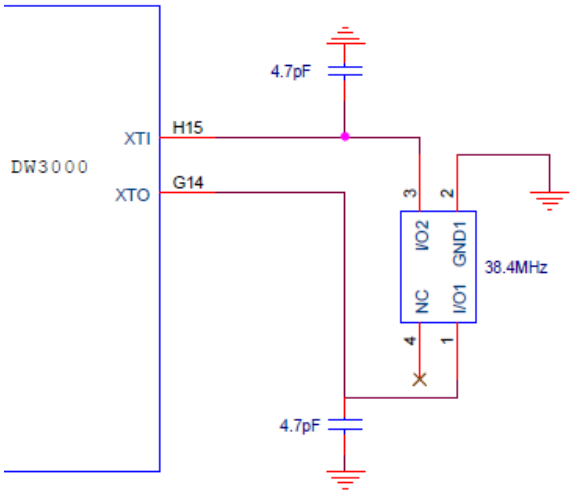


Figure 1 38.4MHz Crystal connection for QM33120W inside module

- 32MHz crystal for Nordic nRF52840 (MCU) HFCLK.

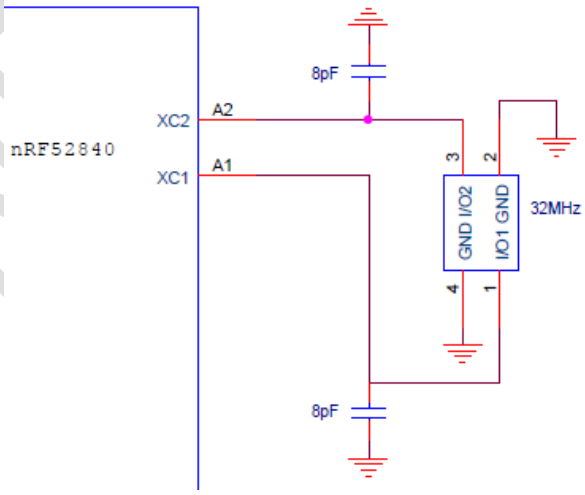


Figure 2 32MHz Crystal connection for nRF52840 inside module

- 32.768KHz crystal for Nordic nRF52840 (MCU) LFCLK.

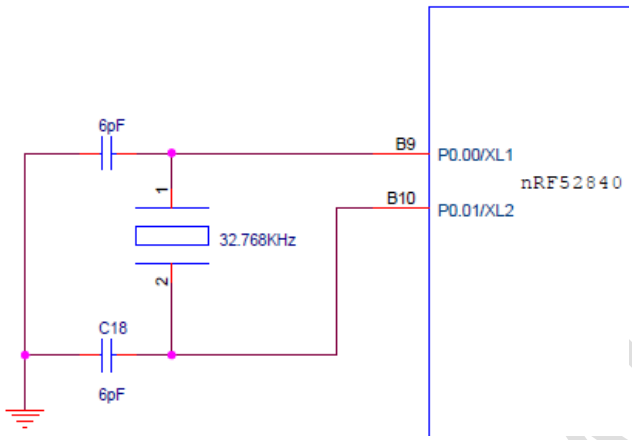


Figure 3 32.768KHz Crystal connection for nRF52840 inside module

When customers design their own firmware, please ensure the configuration of *HFCLK* and *LFCLK* for nRF52840 are compatible with 2AB module hardware design.

Please refer to nRF52840 datasheet for more details about *HFCLK* and *LFCLK* configurations.

2. Power Supply

2.1 Module power supply

There are several input power supplies for the module.

- VDD1: Main power supply (2.5~3.6V) for UWB IC QM33120W.
- VDD2: Power supply (2.5~3.6V) for UWB IC QM33120W.
- VDDMCU: Power supply (2.5~3.6V) for MCU nRF52840.
- VUSB: Power supply (4.4~5.5V) for MCU nRF52840 USB part.

Please refer to Figure 4 for the decoupling capacitors of power supplies. The capacitors should be placed as close as to the module pins.

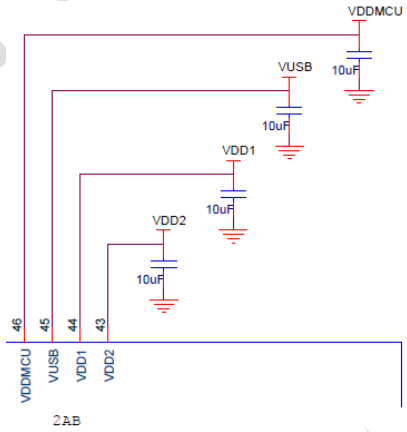


Figure 4 Decoupling capacitors for power supplies

Note: If you don't use USB function of Nrf52840, VUSB is left open.

2.2 nRF52840 power supply configuration

nRF52840 contains two main supply regulator stages, REG0 and REG1.

Each regulator stage has the following regulator type options:

- Low-dropout regulator (LDO)
- Buck regulator (DC/DC)

The two voltage regulators (REG0 and REG1) can be configured in several ways, depending on the selected Supply Voltage mode (normal/high) and the regulator type option (LDO or DC/DC).

nRF52840 power supply configuration of 2AB module is shown as below:

- Normal Voltage mode, DC/DC REG1 enabled

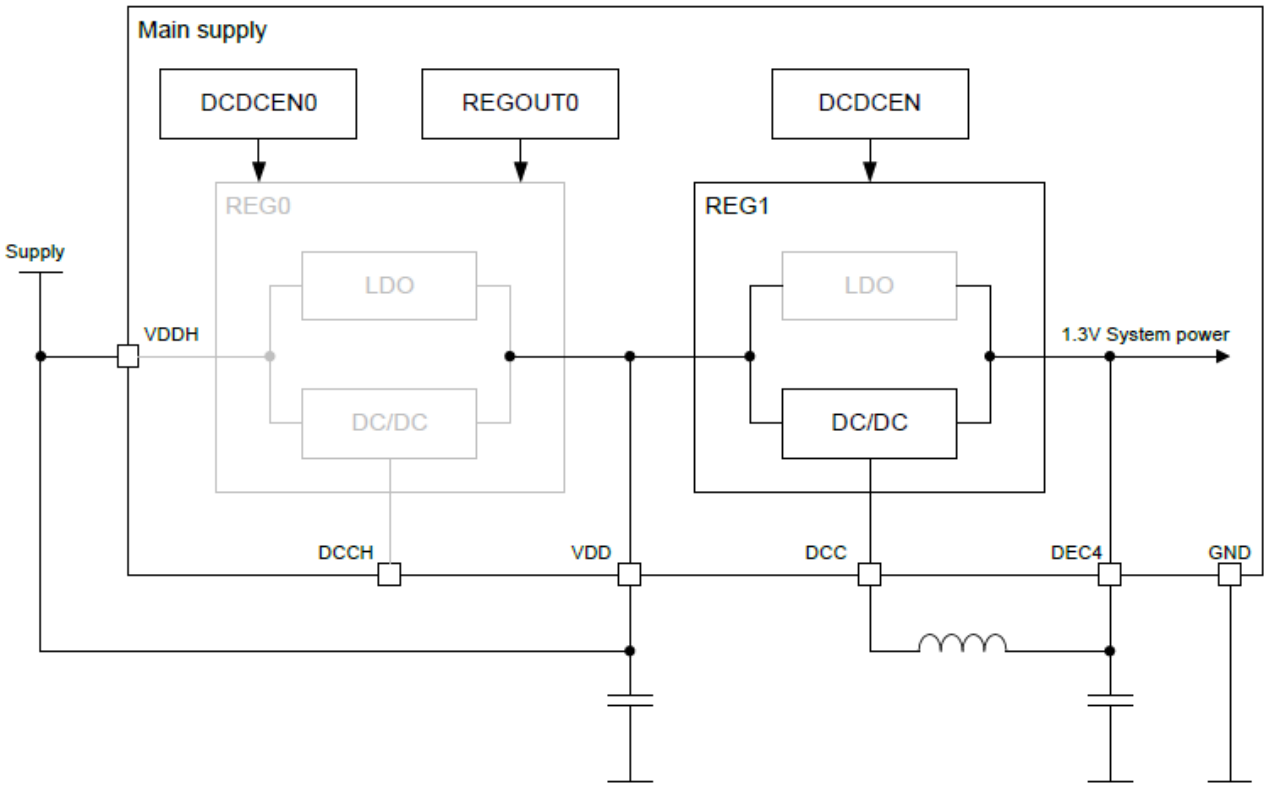


Figure 5 nRF52840 power supply configuration of 2AB module

When customers design their own firmware, please ensure the configurations of voltage regulators are correct.

Please refer to nRF52840 datasheet for the detailed configurations of REG0 and REG1.

3. Interface

3.1 UART interface

The pins below are used as UART interface that multiplexed with GPIOs, please refer to Table 1 for details.

Table 1 UART interface

Module	Connection to MCU	Multiplexed Function
Pin.50	P0.08	UART_RX
Pin.51	P0.07	UART_TX

Notes: The UART definition as above is based on 2AB test FW configuration. These interfaces can be mapped to other physical pins according to customer FW configuration.

3.2 SPI interface

The pins below are used as SPI interface that multiplexed with GPIOs, please refer to Table 2 for details.

Table 2 SPI interface

Module	Connection to MCU	Multiplexed Function
Pin.2	P0.05	SPIS_CLK
Pin.3	P0.04	SPIS_CS
Pin.4	P0.27	SPIS_MOSI
Pin.52	P0.06	SPIS_MISO

Notes: The SPI definition as above is based on 2AB test FW configuration. These interfaces can be mapped to other physical pins according to customer FW configuration.

3.3 I2C interface

The pins below are used as I2C interface, please refer to Table 3 for details.

Table 3 I2C interface

Module	Connection to nRF52840	Connect to 3-axis sensor	Function
Pin.29	P0.22	SDA/SDI/SDO	I2C_SDA
Pin.30	P0.19	SCL/SPC	I2C_SCL

Notes: These two pins connected to 3-axis sensor in the module, so these Pins cannot use for other functions.

3.4 USB interface

The pins below are used as USB interface, please refer to Table 4 for details.

Table 4 USB interface

Module	Connection to nRF52840	Function
Pin.39	D+	USB_D+
Pin.40	D-	USB_D-
Pin.45	VBUS	Power supply for USB interface

The USB peripheral features a number of dedicated pins.

The dedicated USB pins can be grouped in two categories, signal and power. The signal pins consist of the D+ and D- pins, which are to be connected to the USB host. They are dedicated pins, and not available as standard GPIOs. The USB implements the 5V Short Circuit Withstand ECN meaning that these two pins are not 5 V tolerant.

The signal pins and the pull-up will operate only while VBUS is in its valid voltage range, and USB is

enabled through the ENABLE register.
Notes: If don't use USB interface, please left VUSB, USB_D+ and USB_D- open.

3.5 SWD interface

The pins below are used as SWD interface that multiplexed with GPIOs, please refer to Table 5 for details.

Table 5 SWD interface

Module	Connection to nRF52840	Multiplexed Function
Pin.24	SWCLK	SWCLK
Pin.25	SWDIO	SWDIO

3.6 GPIOs

The GPIOs can be configured by software as output (Push-pull or open drain), or as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. Please refer to Table 6 for I/O specifications.

Table 6 I/O specification

Symbol	Description	Min.	Typical	Max.	Unit
V_{IH}	Input high voltage	0.7 x VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 x VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7 V	VDD - 0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD - 0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD - 0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7 V	VSS		VSS + 0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS + 0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS + 0.4	V
$I_{OL,SD}$	Current at VSS+0.4 V, output set low, standard drive, VDD ≥ 1.7 V	1	2	4	mA
$I_{OL,HDH}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
$I_{OL,HDL}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
$I_{OH,SD}$	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7 ≥1.7	1	2	4	mA
$I_{OH,HDH}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
$I_{OH,HDL}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
$t_{RF,15pF}$	Rise/fall time, standard drive mode, 10-90%, 15 pF load(*1)		9		ns

$t_{RF,25pF}$	Rise/fall time, standard drive mode, 10-90%, 25 pF load(*1)		13		ns
$t_{RF,50pF}$	Rise/fall time, standard drive mode, 10-90%, 50 pF load(*1)		25		ns
$t_{HRF,15pF}$	Rise/Fall time, high drive mode, 10-90%, 15 pF load(*1)		4		ns
$t_{HRF,25pF}$	Rise/Fall time, high drive mode, 10-90%, 25 pF load(*1)		5		ns
$t_{HRF,50pF}$	Rise/Fall time, high drive mode, 10-90%, 50 pF load(*1)		8		ns
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
C_{PAD}	Pad capacitance		3		pF
C_{PAD_NFC}	Pad capacitance on NFC pads 4 pF		4		pF
I_{NFC_LEAK}	Leakage current between NFC pads when driven to different states		1	10	µA

(*1) Rise and fall times based on simulations.

4. Internal Connection Inside Module

4.1 Internal connection between MCU and UWB IC

The following table shows the internal connection between MCU nRF52840 and UWB IC.

Table 7 Connection between MCU and UWB IC

MCU		Function	UWB IC	
Pin	Name		Pin	Name
H5	P0.23	-----	A6	SPIMISO
H6	P0.16	-----	A8	SPICLK
J5	P0.20	-----	B5	SPICSn
J6	P0.17	-----	B7	SPIMOSI
K2	P0.25	-----	B1	IRQ
G3	P1.02	-----	B9	WakeUp
K7	P0.15	-----	A10	RSTn

4.2 Internal connection between MCU nRF52840 and 3-Axis accelerometer

3-axis accelerometer LIS2DW12 is integrated in 2AB module for motion detecting. Table below shows the connection between MCU nRF52840 and 3-Axis accelerometer.

Table 8 Connection between MCU and 3-Axis motion detector

MCU			3-Axis motion detector	
Pin	Name		Pin	Name
K4	P0.19	-----	1	SCL/SPC
F3	P1.03	-----	2	CS
J3	P1.00	-----	3	SDO/SA0
K3	P0.22	-----	4	SDA/SDI/SDO
H1	P1.04	-----	11	INT2
J1	P1.01	-----	12	INT1

4.3 Detectable direction of 3-Axis accelerometer

Picture below shows the direction of the detectable accelerations of the integrated sensor. Please refer to LIS2DW12 for more details about the acceleration detection.

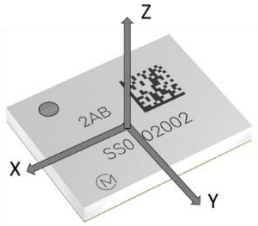


Figure 6 Direction of the detectable accelerations

5. Voltage and Temperature Measurement

The on-chip voltage and temperature monitors allow the host to read the voltage on the VDD1 pin and the internal die temperature information from the QM33120.

According to latest QM33120 Datasheet, due to complexities associated with silicon thermal profiles across product variants, package types and operating modes, the temperature and battery voltage readback functions of the QM33120 IC are not supported.

If temperature and/or voltage readings are required, it is suggested to implement this external to the QM33120 IC, e.g. ADC of host MCU.

6. OTP Map

Table 9 describes the OTP map inside module.

Table 9 OTP map

2AB OTP memory map					
Address	**Byte[3]**	**Byte[2]**	**Byte[1]**	**Byte[0]**	**Note**
0x00	64 bit EUI				Lower 4 bytes of EUI
0x01					Higher 4 bytes of EUI
0x10					Uncallocated
0x11	CH5 TX Power Level PRF64				
0x12					Uncallocated
0x13	CH9 TX Power Level PRF64				
0x14					Uncallocated
0x15					
0x16					
0x17					
0x18					
0x19			Vbat	Temp	
0x1A	CH5 PDoA code PRF64		CH9 PDoA code PRF64		
0x1B		CH5 PG COUNT PRF64		CH9 PG COUNT PRF64	
0x1C	CH5 Antenna Delay PRF 64		CH9 Antenna Delay PRF 64		
0x1D					Uncallocated
0x1E	CH5 PG_DELAY PRF64	CH9 PG_DELAY PRF64	-	XTAL_trim	
0x1F	-	-	-	OTP Revision	
0x36-0x5C					Uncallocated
0x5D		Sensor_flag	Module version		
0x5E	BT MAC				Lower 4 bytes of MAC
0x5F			BT MAC		Higher 2 bytes of MAC

7. PCB design

The following are some recommendations for the module layout:

- Keep all the traces as short as possible.

- Avoid mixing Analog (RF1, RF2), Power (VDD1, VDD2, VDDMCU) and Digital (SPI etc) groups together.
- Place all the decoupling capacitors as close to the corresponding module pads as possible, the smaller capacitor should be closer to the pad. Connect ground pad of each capacitor to the good ground plane directly to minimize ESR and ESL of the return current path.
- RF1 and RF2 lines should be 50 Ohm impedance-controlled lines. The matching capacitor pads should be embedded into the track (have the same width) to remove any possible discontinuities.
- Keep RF trace as wider as possible, and for the stack-up, the first solid copper layer should be at least 0.45mm away from the Top layer (RF trace layer).
- It is recommended to remove the solder mask on the RF trace.

8. Antenna design

8.1 UWB antenna design

Some reference antennas for UWB applications are described below.

8.1.1 Antenna for TWR and TDoA application

1) WB002 UWB Omni-directional Planar Antenna

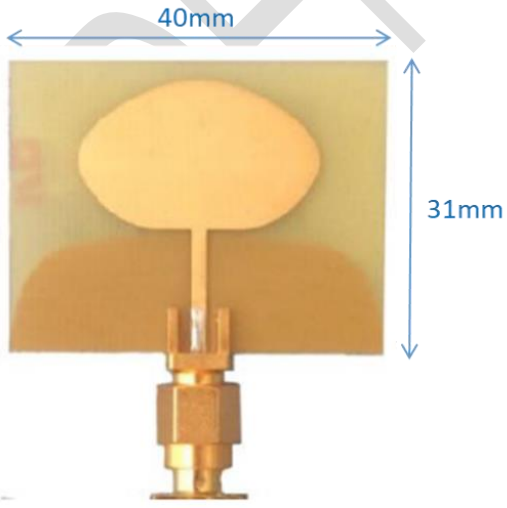
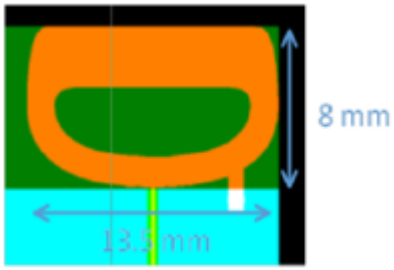


Figure 7 WB002 UWB antenna

Key features:

- Operational Frequency Range: 3 GHz to 8 GHz
- Maximum Gain: 3.3 dBi at 6.5 GHz
- Radiation Pattern: Omni-directional
- Can be integrated into existing PCB
- Can buy existing SMA type antenna from online shop and quickly used for some demo system.

For more information about this antenna, please refer to Qorvo's design files at the link below: *WB001, WB002 & WB003 Antenna Design Files*



2) *WB003* UWB Omni-directional Planar Antenna

Figure 8 WB003 UWB antenna

Key features:

- Operational Frequency Range: channel 5, 6.5 GHz
- Maximum Gain: 2.5 dBi at 6.5 GHz
- Radiation Pattern: Omni-directional
- Small size, can be integrated into existing PCB

This antenna is used on 2AB module certification board.

For more information about this antenna, please refer to Qorvo's antenna design files at the link below:

WB001, WB002 & WB003 Antenna Design Files

8.1.2 Antenna Arrays for PDoA/AoA Application

The antenna arrays, including Qorvo *ML005, ML009* and *JL359,* can be used on the anchors in PdoA/AoA applications.

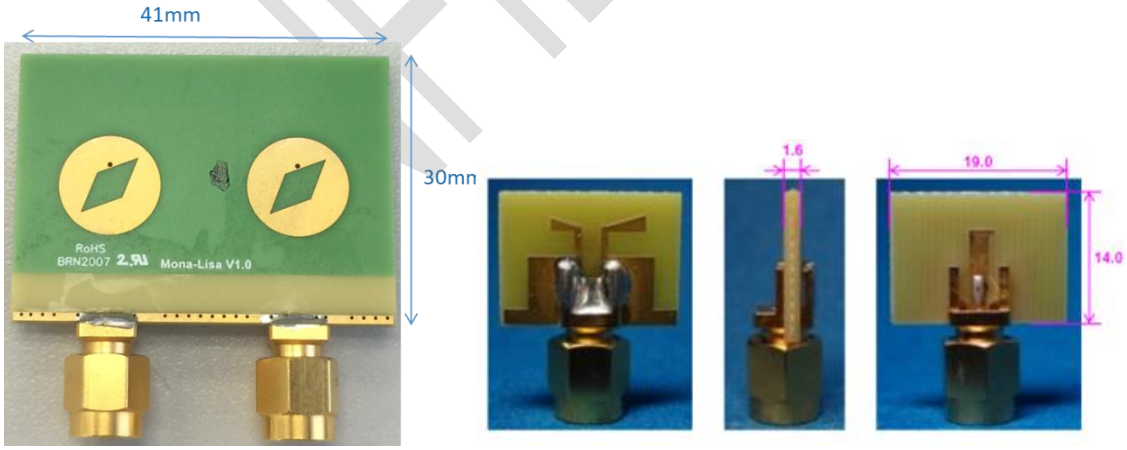


Figure 9 ML005 PDoA anchor antenna (left) and WB005 tag antenna(right)

Please noted that the distance between two antennas should be less than or equal to one-half wavelength, $\lambda/2$, of the operational radio signals.

The tags generally need good performance on omni-directional radiation. It is recommended to use Qorvo *WB005*, *WB009* or *JL159* respectively paring with the anchors.

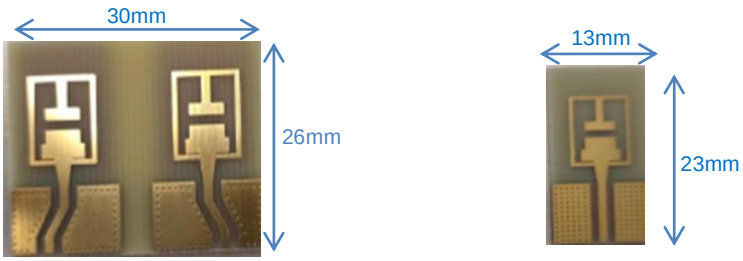


Figure 10 JL359 PDoA antenna (left) and JL159 tag antenna (right)

Table 10 UWB PDoA Antennas

Name	Design Number	Polarization	Directionality	Channels supported
Mona Lisa Ch5	ML005	Circular	PDoA/AoA Anchor	Channel 5 (6.5GHz)
Mona Lisa Ch9	ML009	Circular	PDoA/AoA Anchor	Channel 9 (8 GHz)
CP Wings Ch5	WB005	Circular	Omnidirectional tag	Channel 5 (6.5GHz)
CP Wings Ch9	WB009	Circular	Omnidirectional tag	Channel 9 (8 GHz)
Jolie AoA	JL359	Linear	PDoA/AoA Anchor	Channel 9 (8 GHz) & Channel 5 (6.5GHz)
Jolie Omni	JL159	Linear	Omnidirectional tag	Channel 9 (8 GHz) & Channel 5 (6.5GHz)

For more information about the antennas, please contact Qorvo FAE.

8.2 Bluetooth antenna design

The following antenna (red area in picture below) can be used for 2AB BLE RF port.

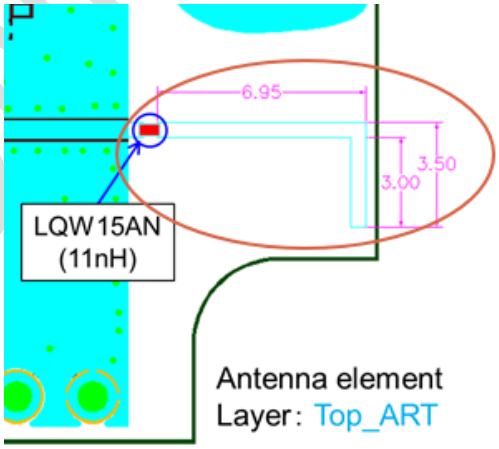


Figure 11 Bluetooth antenna design

- Please connect the module and antenna area with 50ohm line.
- Please apply 1 matching component in antenna area.
- Land size for component, please follow your design rule.

9. LNA reference design

To achieve better RX performance, Qorvo LNA QM14068 is recommended to add on the RF path. There is about 6dB increase in RX sensitivity when LNA is added.

Figure below is a reference circuit with LNA.

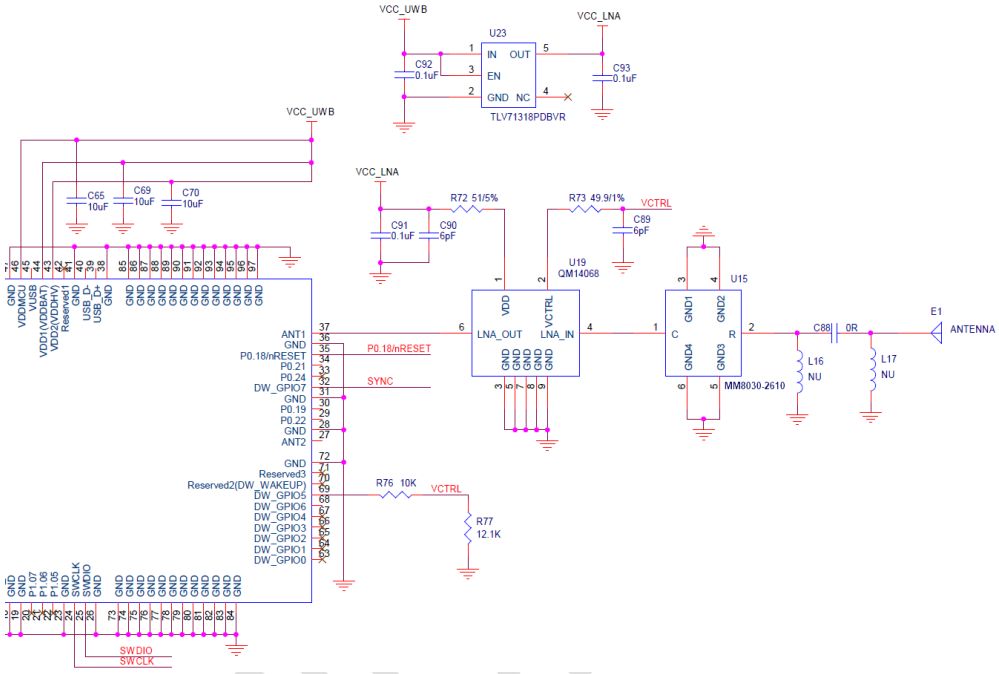


Figure 12 Reference design with LNA

Note:

a) TLV71318 is LDO for LNA power supply.

b) QM33120 GPIO5 is used as VCTRL signal for LNA.

c) MM8030-2610 is a RF switch connector for conducted test only. It can be removed if conducted test is not needed.

10. Calibration

Some calibrations are carried out in 2AB module production testing, including frequency error, TX power, antenna delay and PDoA code. The calibration results are stored into 2AB module OTP memory.

Please note that all the tests are performed as *conductive test* via module's RF port. Customers should add appropriate compensations to fit their final products.

Please refer to [6] for more details about calibrations and production testing of DW3000-based products.

10.1 TX power adjustment

TX power was calibrated for each unit in module production line. There are two purposes for TX power calibration. One is to minimize the device-to-device variations, the other is to calibrate the Power Spectral Density (PSD) to meet regulatory limit.

Certification regulations typically specify a transmit power limit of -41.3dBm/MHz, and generally measure this using a 1ms dwell time in each 1 MHz segment. If a packet is short (the frame duration is less than 1000μs per 1ms cycle), it is possible to boost the power for the actual transmit packet while PSD staying within the regulatory limits.

The figure below shows some examples for the allowed boost power.

$$\text{Relative Power (dB)} = 10\log_{10}\left(\frac{Frame\_Length}{1000\ us}\right)$$

Frame duration(us)	Boost Allowed (dB)
1000	0.0
900	0.5
800	1.0
700	1.5
600	2.2
500	3.0
400	4.0
300	5.2
275	5.6
250	6.0
225	6.5
200	7.0
175	7.6
150	8.2
125	9.0
100	10.0
75	11.2
50	13.0

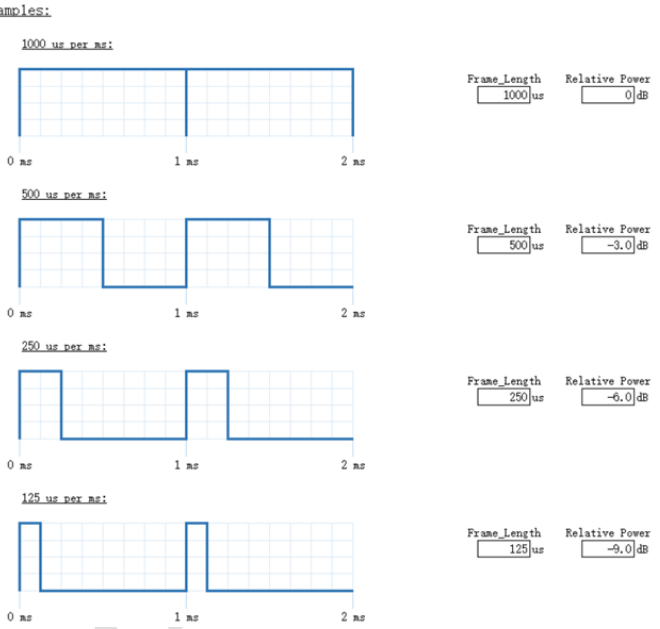


Figure 13 Boost power examples

250us frame duration is used for 2AB TX power calibration in production line.

On customer side, there are three factors need to be considered for power adjustment to make sure the final product output power meets the regulatory limit.

- Frame duration in actual application
- PCB trace loss on customer board
- Antenna gain

There are two steps for power adjustment:

Step1: Calculate the power difference between the customer's condition and 2AB module test condition. For example:

- Frame duration: 125us
- EVB trace loss: 1dB
- Antenna gain: 3dBi

The power difference should be:

Power diff = Boost gain + EVB trace loss - antenna gain = 3 + 1 - 3 = 1 (dB)

That means the customer can increase power by 1dB based on module OTP TX power value.

Step2: Adjust the TX power code setting by the relevant API and set the new TX power code to TX power

control register.

Regarding TX power adjustment with a certain delta (+1dB in example above) from OTP value, please contact muRata to get the sample code for reference.

10.2 Antenna delay calibration

Figure below shows the TOF scheme for distance measurement. The signal propagation time from antenna to UWB IC core may be difference for each unit due to the variation of BPF, RF switch, UWB IC etc. These need to be calibrated out to ensure the accuracy of distance measurement across devices.

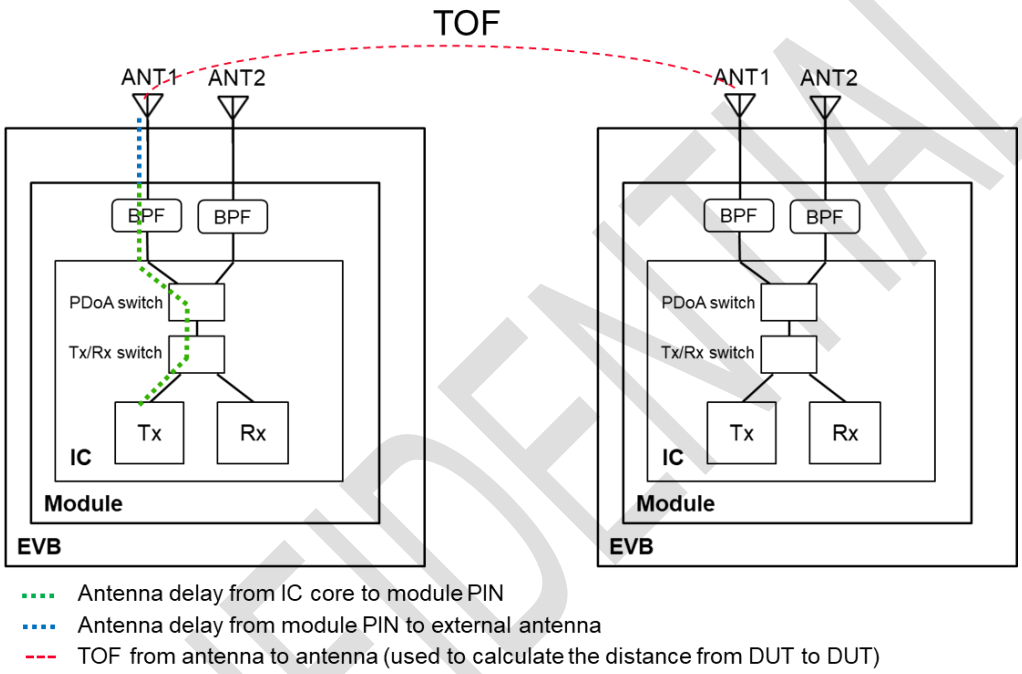


Figure 14 TOF Scheme

The antenna delay from IC core to module PIN is calibrated for each unit in module production line to minimize the device-to-device variations. Antenna delay from module PIN to external antenna should be calibrated on customer side.

Basically, customers do not need to do the antenna delay calibration for each DUT but need to calibrate the antenna delay for each kind of design (PCB, antenna).

Antenna delay calibration steps are as below:

1. Run double side TWR on a known distance over a sufficient sample of units (e.g 10pcs), get the average measured distance data.
2. Calculate time delay = (measured distance – actual distance)/ c
3. Transfer Time delay to antenna delay (record as external antenna delay)
4. Total actual antenna delay = antenna delay in OTP + external antenna delay
5. Apply the new antenna delay in FW

Please contact muRata for more details about the antenna delay calibration if needed.

10.3 Phase Difference (PDoA) calibration

There are differences in the propagation time of signals on the two RF paths, caused by process variation in the PCB, any front-end components such as BPF, RF switch ICs, the DW3000 IC, etc. These need to be calibrated out to ensure accurate results across devices.

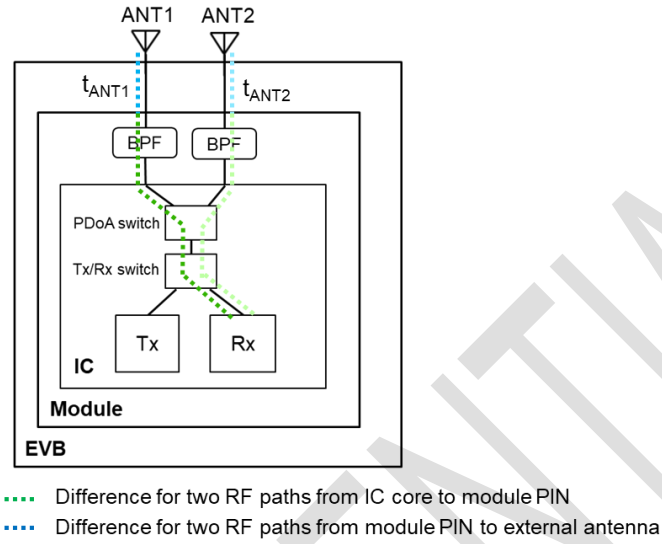


Figure 15 PDoA calibration image

The difference for two RF paths from IC core to module PIN is calibrated for each unit in module production line and stored as PDoA code in OTP. Difference from module PIN to external antenna should be calibrated on customer side.

Basically, customer no need to do the PDoA calibration for each DUT, but for each type of antenna design, sufficient PDoA test is needed to generate a new LUT for accurate AoA measurement.

Please contact muRata for more details about the PDoA calibration if needed.