

### OVERVIEW

ORing isolation is not required to achieve sharing of current between paralleled power supplies. However, for applications where reliability is critical it may be desired to protect against the unlikely event of a power module fault that would compromise the common bus.

The reference design in the schematic below shows how it may be implemented for the full-power main output, using MOSFETs to provide very low voltage drop.

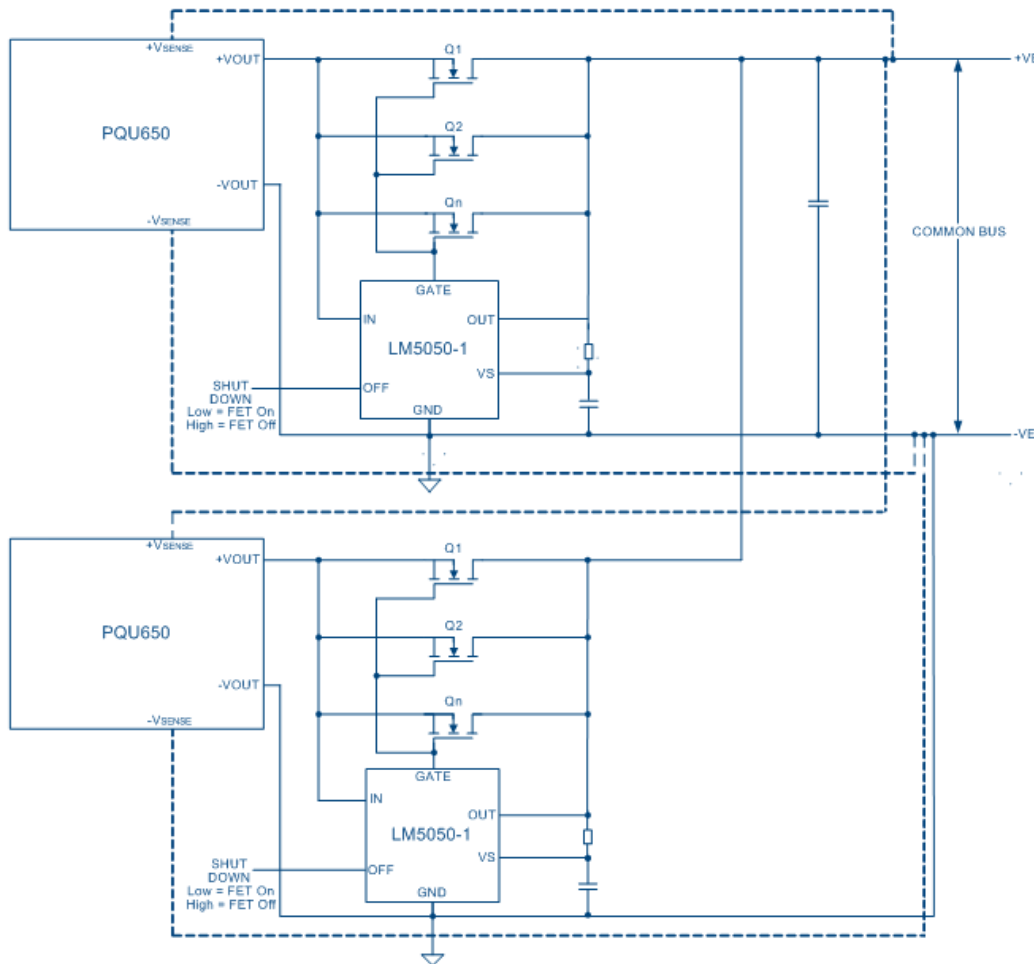
For the lower current auxiliary (V2) output, ORing is most easily implemented with diodes rated to tolerate the reverse voltage, leakage current and the forward current.

The Aux (V2) outputs can be tied together for redundancy but total combined output power (at initial power up) must not exceed 2.5W; external ORing devices are recommended to preserve redundancy.

It is not recommended that the 12V Fan (V3) outputs are connected in parallel since these outputs are only semi regulated.

NB: Optional remote sense connections are not mandatory for parallel operation.

### General Schematic



NB: Consult the TI website for definitive details: <http://www.ti.com/lit/ds/symlink/lm5050-1.pdf>

### Suggested MOSFETS

The following is a list of MOSFETS shown as a guide. They are rated for voltage withstand for the respective output voltage variants. It should be stressed that the number of MOSFETS used in a customer deployment shall be at the discretion of the End User who will be best placed to assess from an operational perspective based on:

- Overall forward voltage drop (and therefore point of load output voltage regulation).
- Thermal limitations; the suggested devices are SMD parts and therefore their thermal management will largely rely on their deployment in the End User equipment; the relevant datasheet for the MOSFET will provide a guide of junction temperature rises for a given area of copper pad of suitable density.
- Whether the end system relies solely on natural convection cooling or is provided with forced convection airflow that will influence the component temperatures at system level.

Manufacturer	PQU650-12	PQU650-24	PQU650-28	PQU650-48	PQU650-54
	FDMS8050	FDMS86550	FDMS86550	FDMS86350	FDMS86350
Fairchild/On Semi	N-Channel 30V, 55A <sup>1</sup> , 0.65mΩ	N-Channel 60V, 32A <sup>1</sup> , 1.65mΩ	N-Channel 60V, 32A <sup>1</sup> , 1.65mΩ	N-Channel 80 V, 25A <sup>1</sup> , 2.4mΩ	N-Channel 80 V, 25A <sup>1</sup> , 2.4mΩ

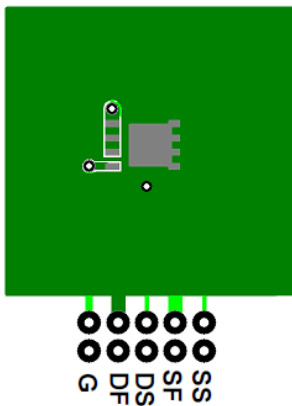
**Note:**

<sup>1</sup>: The current as shown is applicable to T<sub>A</sub> = 25°C.

R<sub>θJA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad of 2oz copper pad on a 1.5in x 1.5in board of FR-4 material

R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the end user's board design.

The End User shall evaluate the MOSFET critical temperatures in their deployment for safe and reliable operation.



45°C/W when mounted on a 1in<sup>2</sup> pad of 2oz copper.

Reference to the LM5050-1 Datasheet may assist in MOSFET selection: <http://www.ti.com/product/LM5050-1>

