Communication Protocol Support

The D1U4CS-W family of power supplies currently supports 3.3V-bus and 5V-bus standard-mode (100kHz) I²C Serial Communication as outlined in Philips Semiconductors "The I²C Bus Specification Version 2.1" (January 2000).

The D1U4CS-W family of power supplies can also support 3.3V-bus and 5V-bus SMBUS Serial Communication as outlined in the SBS Implementers forum "System Management Bus (SMBUS) Specification Version 2.0" (August 2000)

D1U4CS-W power supplies are configured to operate as slave-only devices.

However, they can be re-configured to support single master operation and multi-master and slave operation.

The available address lines currently allows for communication with up to 8 D1U4CS-W power supplies on a single serial communication bus.

Each D1U4CS-W power supply contains a :

1. 2K serial EEPROM device used for FRU data storage (FRU data specs customer specific)
2. System-On-Chip (SOC) -type controller used for D1U4CS-W status, fault, and parametric data reporting and remote on/off control

I²C Device Addressing

The D1U4CS-W family of power supplies supports 8-bit I²C addressing (7-bit slave address plus 1-bit read/write control). The specified I²C addresses are as follows:

Table A1 - I²C Device Addresses

Device Name	Device Type	PS Slot					
		#	A2	A1	A0	I²C Address	
Standalone EEPROM	24AA024	0	0	0	0	1010 000	0xA0
		1	0	0	1	1010 001	0xA2
		2	0	1	0	1010 010	0xA4
		3	0	1	1	1010 011	0xA6
		4	1	0	0	1010 100	0xA8
		5	1	0	1	1010 101	0xAA
		6	1	1	0	1010 110	0xAC
		7	1	1	1	1010 111	0xAE
Flash-Emulated EEPROM	microcontroller flash-emulated EEPROM	0	0	0	0	1110 000	0xE0
		1	0	0	1	1110 001	0xE2
		2	0	1	0	1110 010	0xE4
		3	0	1	1	1110 011	0xE6
		4	1	0	0	1110 100	0xE8
		5	1	0	1	1110 101	0xEA
		6	1	1	0	1110 110	0xEC
		7	1	1	1	1110 111	0xEE
I²C Port	microcontroller	0	0	0	0	1011 000	0xB0
		1	0	0	1	1011 001	0xB2
		2	0	1	0	1011 010	0xB4
		3	0	1	1	1011 011	0xB6
		4	1	0	0	1011 100	0xB8
		5	1	0	1	1011 101	0xBA
		6	1	1	0	1011 110	0xBC
		7	1	1	1	1011 111	0xBE

RAM Bytes Accessible Through I²C Serial Communications

Upon power up, the D1U4CS-W power supplies maintain 27 RAM bytes that are accessible through I²C serial communication. These bytes provide power supply status information, fault information, and sensor data.

The 27 data bytes are ordered as follows:

Byte 0: Status0 - Power supply operation status 0
Byte 1: Status1 - Power supply operation status 1
Byte 2: Fault0 - Power supply fault 0
Byte 3: Fault1 - Power supply fault 1
Byte 4: Vout2 - Upper (MSB) Byte of 16-bit representation of Main Output Voltage
Byte 5: Vout1 - Lower (LSB) Byte of 16-bit representation of Main Output Voltage
Byte 6: Iout2 - Upper (MSB) Byte of 16-bit representation of Main Output Current
Byte 7: Iout1 - Lower (LSB) Byte of 16-bit representation of Main Output Current
Byte 8: Stanby_Vout2 - Upper (MSB) Byte of 16-bit representation of Standby Output Voltage
Byte 9: Stanby_Vout1 - Lower (LSB) Byte of 16-bit representation of Standby Output Voltage
Byte 10: Stanby_Iout2 - Upper (MSB) Byte of 16-bit representation of Standby Output Current
Byte 11: Stanby_Iout1 - Lower (LSB) Byte of 16-bit representation of Standby Output Current
Byte 12: Fan1_Speed2 - Upper (MSB) Byte of 16-bit representation of Fan1 speed
Byte 13: Fan1_Speed1 - Lower (LSB) Byte of 16-bit representation of Fan1 speed
Byte 14: Fan2_Speed2 - Upper (MSB) Byte of 16-bit representation of Fan2 speed
Byte 15: Fan2_Speed1 - Lower (LSB) Byte of 16-bit representation of Fan2 speed
Byte 16: Amb_Temp_2 - Upper (MSB) Byte of 16-bit representation of Ambient Temperature
Byte 17: Amb_Temp_1 - Lower (LSB) Byte of 16-bit representation of Ambient Temperature
Byte 18: HS2_Temp_2 - Upper (MSB) Byte of 16-bit representation of heatsink 2 Temperature
Byte 19: HS2_Temp_1 - Lower (LSB) Byte of 16-bit representation of heatsink 2 Temperature
Byte 20; AC_RmsV2 - Upper (MSB) Byte of 16-bit representation of AC RMS voltage
Byte 21: AC_RmsV1 - Lower (LSB) Byte of 16-bit representation of AC RMS voltage
Byte 22: AC_RmsI2 - Upper (MSB) Byte of 16-bit representation of AC RMS current
Byte 23: AC_RmsI1 - Lower (LSB) Byte of 16-bit representation of AC RMS current
Byte 24: HS1_Temp_2 - Upper (MSB) Byte of 16-bit representation of heatsink1 temperature
Byte 25: HS1_Temp_1 - Lower (LSB) Byte of 16-bit representation of heatsink1 temperature
Byte 26: Confirmation_Byte - Trimming and Calibration Confirmation Byte

Status/Fault Bits Definition

Byte 0 - The D1U4CS-W Status 0 register function and definitions are as follows:

BYTE 0 – Status0 Register							
7	6	5	4	3	2	1	0
PS_ON	PWOK	ACOK	Fail	Fan Failure	OT Warning	OT Critical	AC HI Range
MSB							LSB

Bit #	Bit Status Description	
	Set	Clear
7	Main Output is Enabled	Main Output is Disabled
6	PWOK is OK	PWOK is not OK
5	AC is Ok	AC is Faulted
4	PS is Failed	PS is not Failed
3	Fan2 or Fan1 is Failed	No Fan Fail
2	PS Temperature Warning	No PS Temperature Warning
1	PS Shutdown due to OT	No Over Temperature Shutdown
0	AC Hi is Detected	No AC Hi is Detected

Byte 1 - The D1U4CS-W Status1 register function and definitions are as follows:

BYTE 1 – Status1 Register							
7	6	5	4	3	2	1	0
Flash Constants	-	-	Heatsink2 Sensor	Heatsink1 Sensor	AC I Sensor	AC V Sensor	Pri-Sec Comm.
MSB							LSB

Bit #	Bit Status Description	
	Set	Clear
7	Flash Constants Corrupted	Flash Constants OK
6	-	-
5	-	-
4	Heatsink2 Sensor Failed	Heatsink2 Sensor OK
3	Heatsink1 Sensor Failed	Heatsink1 Sensor OK
2	AC I Sensor Failed	AC I Sensor OK
1	AC V Sensor Failed	AC V Sensor OK
0	Primary-Secondary Communication Failed	Primary-Secondary Communication OK

Byte 2 - The D1U4CS-W Fault 0 register function and definitions are as follows:

BYTE 2 – Fault0 Register							
7	6	5	4	3	2	1	0
Main OV	Main UV	Main OC	Standby Fault	Fan1 Warning	Fan2 Warning	AC Low	24V Fault
MSB							LSB

Bit #	Bit Status Description	
	Set	Clear
7	Main Output Over-voltage Fault	No OV Fault
6	Main Output Under-voltage Fault	No UV Fault
5	Main Output Over-current Fault	No OC Fault
4	Standby Fault	No Standby Fault
3	Fan1 Warning	No fan1 Warning
2	Fan2 Warning	No fan2 Warning
1	AC Low is Detected	No AC Low is Detected
0	24V is below 18V	24V is above 19V

Byte 3 - The D1U4CS-W Fault1 register is reserved for future use.

Byte 26 - The D1U4CS-W confirmation register function and definitions are as follows:

BYTE 26 – Confirmation Register							
7	6	5	4	3	2	1	0
Trimming	AC I lo line cal.	AC I hi line cal.	AC V lo line cal.	AC V hi line cal.	Stby V cal.	Main V cal.	Main I cal.
MSB							LSB

Bit #	Bit Status Description	
	Set	Clear
7	Main V, I, and Standby V Trimming Done	Trimming Not Done
6	AC I Lo Line Calibration Done	AC I Lo Line Calibration Not Done
5	AC I Hi Line Calibration Done	AC I Hi Line Calibration Not Done
4	AC V Lo Line Calibration Done	AC V Lo Line Calibration Not Done
3	AC V Hi Line Calibration Done	AC V Hi Line Calibration Not Done
2	Standby Voltage Calibration Done	Standby Voltage Calibration Not Done
1	Main Voltage Calibration Done	Main Voltage Calibration Not Done
0	Main Current Calibration Done	Main Current Calibration Not Done

Sensor Data Interpretation

Byte 4 (MSB) and Byte 5 (LSB) - 16-bit 2's complement representation of the Main Output Voltage

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-128 to +127.996 V (DC)	(1/256 V)/LSB	+/- 2% of rated output voltage (0^0-50^0C)

Byte 6 (MSB) and Byte 7 (LSB) - 16-bit unsigned integer representation of the Main Output Current

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	0-1023.984375 A (DC)	(1/64 A)/LSB	+/- 5% of rated output current (0^0-50^0C)

Byte 8 (MSB) and Byte 9 (LSB) - 16-bit 2's complement representation of the Standby Output Voltage

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-128 to +127.996 V (DC)	(1/256 V)/LSB	+/- 2% of rated output voltage (0^0-50^0C)

Byte 10 (MSB) and Byte 11 (LSB) - 16-bit unsigned integer representation of the Standby Output Current

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	0-1023.984375 A (DC)	(1/64 A)/LSB	+/- 5% of rated output current (0^0-50^0C)

Byte 12 (MSB) and Byte 13 (LSB) - 16-bit unsigned integer representation of the Fan1 Speed in RPM

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	0-65,535 RPM	1 RPM/LSB	+/- 200 RPM within limits (0^0-50^0C)

Byte 14 (MSB) and Byte 15 (LSB) - 16-bit unsigned integer representation of the Fan2 Speed in RPM

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	0-65,535 RPM	1 RPM/LSB	+/- 200 RPM within limits (0^0-50^0C)

Byte 16 (MSB) and Byte 17 (LSB) - 16-bit 2's complement representation of the Ambient Temperature in deg C

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-512^0C to +511.984375^{0}C	(1/64 ^{0}C)/LSB	+/- 3^0C within limits (0^0 to +50^0C)

Byte 18 (MSB) and Byte 19 (LSB) - 16-bit 2's complement representation of the Heatsink 2 Temperature in deg C

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-512^0C to +511.984375^{0}C	(1/64 ^{0}C)/LSB	+/- 3^0C within limits (0^0 to +50^0C)

Byte 20 (MSB) and Byte 21 (LSB) - 16-bit 2's complement representation of the Input RMS Voltage

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-1024 to +1023.98675 V (RMS)	(1/32 V)/LSB	+/- 5% of rated input voltage (0^0-50^0C)

Byte 22 (MSB) and Byte 23 (LSB) - 16-bit unsigned integer representation of the Input RMS Current

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	0-1023.984375 A (RMS)	(1/64 A)/LSB	+/- 5% of rated input current (0^0-50^0C)

Byte 24 (MSB) and Byte 25 (LSB) - 16-bit 2's complement representation of the Heatsink 1 Temperature in deg C

Model	Data Range	Transfer Equation	Accuracy
D1U4CS-W	-512^0C to +511.984375^{0}C	(1/64 ^{0}C)/LSB	+/- 3^0C within limits (0^0 to +50^0C)

Power Supply Enable/Disable Control

Enable Action:

1. If I^2C commands to enable the PS (single byte command 0xD4), the PS will be enabled;
2. If PS_ON_L switch is ON (PSON_L=LOW), the PS will be enabled;

Disable Action:

1. If I^2C commands to disable the PS (single byte command 0xD3), the PS will be disabled;
2. If PS_ON_L switch is OFF (PSON_L=High), the PS will be disabled;

This means the latest command overrides the previous command. At any moment, PSON_L switch can enable and disable the ps. Similarly, at any moment, I^2C can enable and disable the ps. The latest control signal dominates.

Fan Speed Control

The D1U4CS-W power supply autonomously adjusts the fan pwm using the efficiency-improving cooling algorithm. The firmware calculates the fan pwm based on the following input data: load current, temperature, output voltages, and ps operating state. For safety reason, if micro-controller enters reset state, fan goes full speed.

I²C Read/Write Method for Microcontroller PSMI Port

Using the slot specific I²C address 0xB?, the D1U4CS-W family supports the standard access method of PSMI (Power Supply Management Interface).

The PSMI Read method is as follows:

The host transmits the register number to the slave;
After receiving ACK from slave, the host could start a read request;
After receiving ACK from slave, the host could receive the low byte from the slave;
After ACK from host, the host could receive the high byte from the slave;
After completion of transmitting high byte, the slave will transition to idle state;
The data transmission sequence should be as follows:

PSMI Read Method

START	Slave Address	W	ACK	Register Number	ACK

START	Slave Address	R	ACK	Low Byte	ACK	High Byte	ACK	STOP

Note: Shaded data is from slave to master

The PSMI Write method is as follows:

The host transmits the register number to the slave;
After receiving ACK from slave, the host transmits the low byte to the slave;
After receiving ACK from slave, the host transmits the high byte to the slave;
After receiving ACK from slave, the host transmits STOP to the slave;
After receiving STOP from host, the slave start internal writing operation;
During internal writing operation, further read/write is prohibited;
The data transmission sequence should be as follows:

PSMI Write Method

START	Slave Address	W	ACK	Register Number	ACK	Low Byte	ACK	High Byte	ACK	STOP

Note: Shaded data is from slave to master

Mapping of the Microcontroller RAM Bytes to PSMI Registers

The implemented PSMI registers are detailed in the Table A3. Here is a mapping of the microcontroller RAM bytes to the PSMI registers.

Table A2 - Mapping of Micontroller RAM Bytes to PSMI Registers

Data Name	Byte Number	PSMI Register
Status1 Status0	Byte1 Byte0	0xD0
Fault1 Fault0	Byte3 Byte2	0xD1
Vout1 Vout2	Byte5 Byte4	0x28
Iout1 Iout2	Byte7 Byte6	0x33
Standby_Vout1 Standby_Vout2	Byte9 Byte8	0x29
Standby_Iout1 Standby_Iout2	Byte11 Byte10	0x34
Fan1_Speed1 Fan1_Speed2	Byte13 Byte12	0x20
Fan2_Speed1 Fan2_Speed2	Byte15 Byte14	0x21
Amb_Temp1 Amb_Temp2	Byte17 Byte16	0x02
HS2_Temp1 HS2_Temp2	Byte19 Byte18	0x01
AC_RmsV1 AC_RmsV2	Byte21 Byte20	0x32
AC_RmsI1 AC_RmsI2	Byte23 Byte22	0x3D
HS1_Temp1 HS1_Temp2	Byte25 Byte24	0x00

Note: This table shows the data transmission sequence of PSMI: low byte first. For example, to transmit PSMI register 0xD0, the Byte1 is transmitted first, Byte0 is trasmitted later

Summary of the Implemented PSMI Registers

Table A3 - The PSMI Registers Implemented for D1U4CS-W Family Power Supply

Register		PSMI Description	Register Access	Contents
dec	hex			
0	00	T1 temperature sensor data	Read Only	see A8
1	01	T2 temperature sensor data	Read Only	see A8
2	02	T3 temperature sensor data	Read Only	see A8
3	03	T4 temperature sensor data	No Access	0000
4	04	Reserved	No Access	0000
5	05	Reserved	No Access	0000
6	06	Thermal sensor configuration	Read Only	1300
7	07	Temperature sensor types	Read Only	0000
8	08	T1 temperature sensor offset	Read Only	0000
9	09	T2 temperature sensor offset	Read Only	0000
10	0A	T3 temperature sensor offset	Read Only	0000
11	0B	T4 temperature sensor offset	Read Only	0000
12	0C	Fan speed resolutions (F1, F2)	Read Only	0000
13	0D	Fan speed resolutions (F3, F4)	Read Only	0000
14	0E	F1 fan speed control configuration	Read Only	983A
15	0F	F2 fan speed control configuration	Read Only	983A
16	10	F3 fan speed control configuration	Read Only	0000
17	11	F4 fan speed control configuration	Read Only	0000
18	12	Voltage/current sensor configuration	Read Only	520A
19	13	Fan control associations	Read Only	0000
20	14	F1/F2 fan temperature associations	Read Only	0000
21	15	F3/F4 fan temperature associations	Read Only	0000
22	16	Shutdown events supported	Read Only	3F00
23	17	Status events supported	Read Only	3000
24	18	Control functions supported	Read Only	0005
25	19	Warning events supported	Read Only	2100
26	1A	Reserved configuration registers	No Access	0000
27	1B	Reserved configuration registers	No Access	0000
28	1C	Reserved configuration registers	No Access	0000
29	1D	Reserved configuration registers	No Access	0000
30	1E	Reserved configuration registers	No Access	0000
31	1F	Reserved configuration registers	No Access	0000
32	20	F1 fan speed sensor	Read Only	see A8
33	21	F2 fan speed sensor	Read Only	see A8
34	22	F3 fan speed sensor	Read Only	0000
35	23	F4 fan speed sensor	Read Only	0000
36	24	F1 fan speed control	Read / Write	see PSMI 2.12
37	25	F2 fan speed control	Read / Write	0000
38	26	F3 fan speed control	Read / Write	0000
39	27	F4 fan speed control	Read / Write	0000
40	28	Vout1 voltage sensor	Read Only	see A8
41	29	Vout2 voltage sensor	Read Only	see A8
42	2A	Vout3 voltage sensor	Read Only	0000
43	2B	Vout4 voltage sensor	Read Only	0000
44	2C	Vout5 voltage sensor	Read Only	0000
45	2D	Vout6 voltage sensor	Read Only	0000
46	2E	Vout7 voltage sensor	Read Only	0000
47	2F	Vout8 voltage sensor	Read Only	0000
48	30	Vout9 voltage sensor	Read Only	0000
49	31	Vout10 voltage sensor	Read Only	0000
50	32	Vin voltage sensor	Read Only	see A8

Register		PSMI Description	Register Access	Contents
dec	hex			
51	33	Vout1 current sensor	Read Only	see A8
52	34	Vout2 current sensor	Read Only	see A8
53	35	Vout3 current sensor	Read Only	0000
54	36	Vout4 current sensor	Read Only	0000
55	37	Vout5 current sensor	Read Only	0000
56	38	Vout6 current sensor	Read Only	0000
57	39	Vout7 current sensor	Read Only	0000
58	3A	Vout8 current sensor	Read Only	0000
59	3B	Vout9 current sensor	Read Only	0000
60	3C	Vout10 current sensor	Read Only	0000
61	3D	Vin current sensor	Read Only	see A8
62	3E	Discovery Key 1 / Discovery Key 2	Read Only	5053
63	3F	Discovery Key 3 / Discovery Key 4	Read Only	4D49
64	40	PSMI Major / Minor Version	Read Only	020C
65	41	Power supply code major / minor version	Read Only	0101
66	42	Supplier ID1	Read Only	0000
67	43	Supplier ID2	Read Only	0000
68	44	Reserved	No Access	0000
69	45	Reserved	No Access	0000
70	46	Reserved	No Access	0000
71	47	Reserved	No Access	0000
72	48	Reserved	No Access	0000
73	49	Reserved	No Access	0000
74	4A	Reserved	No Access	0000
75	4B	Reserved	No Access	0000
76	4C	Reserved	No Access	0000
77	4D	Reserved	No Access	0000
78	4E	Reserved	No Access	0000
79	4F	Reserved	No Access	0000
80	50	Reserved	No Access	0000
81	51	Reserved	No Access	0000
82	52	Reserved	No Access	0000
83	53	Vout1 peak current sensor	Read Only	0000
84	54	Vout2 peak current sensor	Read Only	0000
85	55	Vout3 peak current sensor	Read Only	0000
86	56	Vout4 peak current sensor	Read Only	0000
87	57	Vout5 peak current sensor	Read Only	0000
88	58	Vout6 peak current sensor	Read Only	0000
89	59	Vout7 peak current sensor	Read Only	0000
90	5A	Vout8 peak current sensor	Read Only	0000
91	5B	Vout9 peak current sensor	Read Only	0000
92	5C	Vout10 peak current sensor	Read Only	0000
93	5D	Vin peak current sensor	Read Only	0000
94	5E	Shutdown events register	Read / Write Reset	see PSMI 2.12
95	5F	Thermal warning events register	Read / Write Reset	see PSMI 2.12
96	60	Output current warning event register	Read / Write Reset	see PSMI 2.12
97	61	Input warning events	Read / Write Reset	see PSMI 2.12
98	62	Status Register Reset	Read / Write Reset	see PSMI 2.12
99	63	Control Register	Read / Write Reset	see PSMI 2.12
100	64	T1 maximum temperature	Read Only	4010
101	65	T2 maximum temperature	Read Only	4010
102	66	T3 maximum temperature	Read Only	4010
103	67	T4 maximum temperature	Read Only	0000
104	68	F1 operating minimum	Read Only	8813

Register		PSMI Description	Register Access	Contents
dec	hex			
105	69	F2 operating minimum	Read Only	8813
106	6A	F3 operating minimum	Read Only	0000
107	6B	F4 operating minimum	Read Only	0000
108	6C	Maximum fan speed sound power	Read Only	0000
109	6D	Vout1 maximum voltage	Read Only	330C
110	6E	Vout1 minimum voltage	Read Only	CD0B
111	6F	Vout2 maximum voltage	Read Only	DA05
112	70	Vout2 minimum voltage	Read Only	DA04
113	71	Vout3 maximum voltage	Read Only	0000
114	72	Vout3 minimum voltage	Read Only	0000
115	73	Vout4 maximum voltage	Read Only	0000
116	74	Vout4 minimum voltage	Read Only	0000
117	75	Vout5 maximum voltage	Read Only	0000
118	76	Vout5 minimum voltage	Read Only	0000
119	77	Vout6 maximum voltage	Read Only	0000
120	78	Vout6 minimum voltage	Read Only	0000
121	79	Vout7 maximum voltage	Read Only	0000
122	7A	Vout7 minimum voltage	Read Only	0000
123	7B	Vout8 maximum voltage	Read Only	0000
124	7C	Vout8 minimum voltage	Read Only	0000
125	7D	Vout9 maximum voltage	Read Only	0000
126	7E	Vout9 minimum voltage	Read Only	0000
127	7F	Vout10 maximum voltage	Read Only	0000
128	80	Vout10 minimum voltage	Read Only	0000
129	81	Vout1 current spec1	Read Only	0000
130	82	Vout1 current spec2	Read Only	4009
131	83	Vout1 current spec3	Read Only	A40A
132	84	Vout1 current spec4	Read Only	070C
133	85	Vout1 current spec5	Read Only	0000
134	86	Vout1 current spec6	Read Only	0000
135	87	Vout1 current spec7	Read Only	0000
136	88	Vout1 current spec8	Read Only	0000
137	89	Vout1 current spec9	Read Only	0000
138	8A	Vout1 current spec10	Read Only	0000
139	8B	Vout2 current spec1	Read Only	0700
140	8C	Vout2 current spec2	Read Only	C000
141	8D	Vout2 current spec3	Read Only	DD00
142	8E	Vout2 current spec4	Read Only	FA00
143	8F	Vout2 current spec5	Read Only	0000
144	90	Vout2 current spec6	Read Only	0000
145	91	Vout2 current spec7	Read Only	0000
146	92	Vout2 current spec8	Read Only	0000
147	93	Vout2 current spec9	Read Only	0000
148	94	Vout2 current spec10	Read Only	0000
149	95	Vout3 current spec1	Read Only	0000
150	96	Vout3 current spec2	Read Only	0000
151	97	Vout3 current spec3	Read Only	0000
152	98	Vout3 current spec4	Read Only	0000
153	99	Vout3 current spec5	Read Only	0000
154	9A	Vout3 current spec6	Read Only	0000
155	9B	Vout3 current spec7	Read Only	0000
156	9C	Vout3 current spec8	Read Only	0000
157	9D	Vout3 current spec9	Read Only	0000
158	9E	Vout3 current spec10	Read Only	0000

Register		PSMI Description	Register Access	Contents
dec	hex			
159	9F	Input current limit spec1	Read Only	6301
160	A0	Input current limit spec2	Read Only	B200
161	A1	Input current limit spec3	Read Only	0000
162	A2	Input voltage limit spec1	Read Only	A00A
163	A3	Input voltage limit spec2	Read Only	4015
164	A4	Input voltage limit spec3	Read Only	0000
165	A5	Vout1 output power limit	Read Only	9001
166	A6	Vout2 output power limit	Read Only	0F00
167	A7	Vout3 output power limit	Read Only	0000
168	A8	Combined output select1 (power limit)	Read Only	9F01
169	A9	Combined output power limit1	Read Only	1200
170	AA	Combined output select2 (power limit)	Read Only	9F01
171	AB	Combined output power limit2	Read Only	1200
172	AC	Output current sensor bandwidth	Read Only	8813
173	AD	Input current sensor bandwidth	Read Only	6400
174	AE	High line / light load output power	Read Only	8C00
175	AF	High line / medium load output power	Read Only	C800
176	B0	High line / high load output power	Read Only	9001
177	B1	High line / light load & High line / medium load efficiency limit	Read Only	5055
178	B2	High line / high load efficiency limit	Read Only	5500
179	B3	Low line / light load output power	Read Only	8C00
180	B4	Low line / medium load output power	Read Only	C800
181	B5	Low line / high load output power	Read Only	9001
182	B6	Low line / light load & Low line / medium load efficiency limit	Read Only	5055
183	B7	Low line / high load efficiency limit	Read Only	5500
184	B8	Vout1 load share error limit	Read Only	4300
185	B9	Vout2 load share error limit	Read Only	0000
186	BA	Vout3 load share error limit	Read Only	0000
187	BB	Vout4 load share error limit	Read Only	0000
188	BC	Redundancy configuration	Read Only	0201
189	BD	Reserved	No Access	0000
190	BE	Reserved	No Access	0000
191	BF	Reserved	No Access	0000
192	C0	Vendor specific registers	TBD	TBD
193	C1	Vendor specific registers	TBD	TBD
194	C2	Vendor specific registers	TBD	TBD
195	C3	Vendor specific registers	TBD	TBD
196	C4	Vendor specific registers	TBD	TBD
197	C5	Vendor specific registers	TBD	TBD
198	C6	Vendor specific registers	TBD	TBD
199	C7	Vendor specific registers	TBD	TBD
200	C8	Vendor specific registers	TBD	TBD
201	C9	Vendor specific registers	TBD	TBD
202	CA	Vendor specific registers	TBD	TBD
203	CB	Vendor specific registers	TBD	TBD
204	CC	Vendor specific registers	TBD	TBD
205	CD	Vendor specific registers	TBD	TBD
206	CE	Vendor specific registers	TBD	TBD
207	CF	Vendor specific registers	TBD	TBD
208	D0	Custom feature area	Read Only	see A8
		Lo Byte: vPS_Status1		
		Hi Byte: vPS_Status0		

Register		PSMI Description	Register Access	Contents
dec	hex			
209	D1	Custom feature area	Read Only	see A8
		Lo Byte: vPS_Fault1		
		Hi Byte: vPS-Fault0		
210	D2	Custom feature area	Read Only	see A3
		Lo Byte: Confirmation Byte		
		Hi Byte: 0x00		
211	D3	Custom feature area	Write Only	see A5
		One Byte Command to Disable ps		
212	D4	Custom feature area	Write Only	see A5
		One Byte Command to Enable ps		
213	D5	Custom feature area	Write Only	see A12
		One Byte Command to De-assert SMBALERT/L		
214	D6	Custom feature area	TBD	TBD
215	D7	Custom feature area	TBD	TBD
216	D8	Custom feature area	TBD	TBD
217	D9	Custom feature area	TBD	TBD
218	DA	Custom feature area	TBD	TBD
219	DB	Custom feature area	TBD	TBD
220	DC	Custom feature area	TBD	TBD
221	DD	Custom feature area	TBD	TBD
222	DE	Custom feature area	TBD	TBD
223	DF	Custom feature area	TBD	TBD
224	E0	Reserved	No Access	0000
225	E1	Reserved	No Access	0000
226	E2	Reserved	No Access	0000
227	E3	Reserved	No Access	0000
228	E4	Reserved	No Access	0000
229	E5	Reserved	No Access	0000
230	E6	Reserved	No Access	0000
231	E7	Reserved	No Access	0000
232	E8	Reserved	No Access	0000
233	E9	Reserved	No Access	0000
234	EA	Reserved	No Access	0000
235	EB	Reserved	No Access	0000
236	EC	Reserved	No Access	0000
237	ED	Reserved	No Access	0000
238	EE	Reserved	No Access	0000
239	EF	Reserved	No Access	0000
240	F0	Reserved	No Access	0000
241	F1	Reserved	No Access	0000
242	F2	Reserved	No Access	0000
243	F3	Reserved	No Access	0000
244	F4	Reserved	No Access	0000
245	F5	Reserved	No Access	0000
246	F6	Reserved	No Access	0000
247	F7	Reserved	No Access	0000
248	F8	Reserved	No Access	0000
249	F9	Reserved	No Access	0000
250	FA	Reserved	No Access	0000
251	FB	Reserved	No Access	0000
252	FC	Reserved	No Access	0000
253	FD	Reserved	No Access	0000
254	FE	Reserved	No Access	0000
255	FF	Reserved	No Access	0000

Flash-Emulated EEPROM Read/Write Method

The D1U4CS-W family supports a 2 Kbit flash-emulated EEPROM. This enables the host to read and write the microcontroller's internal flash memory that was reserved as the emulated EEPROM. The read protocol includes Current Address Read, Sequential Read, and Random Read. The write protocol includes Byte Write and Multi-Byte Write.

The Current Address Read method is as follows:

The internal read address pointer is initialized to point to the address 0;
The address pointer is incremented by one after each byte read operation;
After the last address (255) has been read, the pointer wraps to the address 0;
The data transmission sequence should be as follows:

Emulated EEPROM Current Address Read

START	Slave Address	R	ACK	Data	NACK	STOP

Note: Shaded data is from slave to master

The Sequential Read method is as follows:

The internal read address pointer is pointing to the address 0;
The address pointer is incremented by one after each byte read operation;
After the last address (255) has been read, the pointer wraps to the address 0;
The data transmission sequence should be as follows:

Emulated EEPROM Sequential Read

START	Slave Address	R	ACK	Data(0)	ACK	…	Data(i)	NACK	STOP

Note: Shaded data is from slave to master

The Random Read method is as follows:

The internal read address pointer is set at any time by a write command:

Write Command to Set Read Address Pointer

START	Slave Address	W	ACK	Read Address	ACK

Note: Shaded data is from slave to master

Subsequent data transmission sequence should be as follows:

Emulated EEPROM Random Read

START	Slave Address	R	ACK	Data	NACK	STOP

Note: Shaded data is from slave to master

The address pointer is incremented by one after each byte read operation;
After the last address (255) has been read, the pointer wraps to the address 0;

The Byte Write method is as follows:

The host transmits the write address to the slave;
After receiving ACK from slave, the host transmits the data to the slave;
After receiving ACK from slave, the host transmits STOP to the slave;
After receiving STOP from host, the slave start internal writing operation;
During internal writing operation, further read/write is prohibited;
The data transmission sequence should be as follows:

Emulated EEPROM Byte Write

START	Slave Address	W	ACK	Write Address	ACK	Data	ACK	STOP

Note: Shaded data is from slave to master

The Multi-Byte Write method is as follows:

The host transmits the write address to the slave;
After receiving ACK from slave, the host transmits the data 0 to the slave;
After receiving ACK from slave, the host transmits data 1 to the slave;
After transmitting data n and receiving ACK from slave, the host transmits STOP to the slave;
After receiving STOP from host, the slave start internal writing operation;
During internal writing operation, further read/write is prohibited;
The data transmission sequence should be as follows:

Emulated EEPROM Page Write

START	Slave Address	W	ACK	Write Address	ACK	Data(0)	ACK	……	Data(n)	ACK	STOP

Note: Shaded data is from slave to master

Diagnostic Data structure in the Emulated EEPROM

Total size of the emulated EEPROM is 256 Bytes. The first 64 bytes are used to store product information. The remaining space is used to store firmware diagnostic data. The product information is as follows:

1. **Manufacturer:** **"MURATA-PS," addresses 0-8**
2. **Manufacturer's Part Number:** **"D1U4CS-W-2200-12-HxxC," addresses 9-14**
3. **Product serial Number:** **"123456789," addresses 15-23**
4. **Customer Specification Number:** **"804-120109-001-A," addresses 24-39**
5. **Customer Revision Number:** **"A1," addresses 40-41**
6. **Firmware Revision Number:** **"V01R01A1," addresses 42-49**

When the main output voltage is shutdown due to OT, OC, or OV faults, the firmware captures a snapshot of the internal data (RAM Byte0 to Byte26), and put the snapshot in the EEPROM. Only one snapshot is available for retrieval. The latest snapshot overrides the previous snapshot. The data is structured like this:

Byte0: **address 64**
Byte1: **address 65**
Byte2: **address 66**
Byte3: **address 67**
Byte4: **address 68**
Byte5: **address 69**
Byte6: **address 70**
Byte7: **address 71**
Byte8: **address 72**
Byte9: **address 73**
Byte10: **address 74**
Byte11: **address 75**
Byte12: **address 76**
Byte13: **address 77**
Byte14: **address 78**
Byte15: **address 79**
Byte16: **address 80**
Byte17: **address 81**
Byte18: **address 82**
Byte19: **address 83**
Byte20: **address 84**
Byte21: **address 85**
Byte22: **address 86**
Byte23: **address 87**
Byte24: **address 88**
Byte25: **address 89**
Byte26: **address 90**

The latest snapshot is retained until a host erases it or a new snapshot overrides it.

SMBAlert/L Signal

If any of the OV, OC, or OT faults is detected, the SMBALERT/L signal is asserted. When SMBALERT/L is detected or periodically, a host can use the SMBUS Alert Response Address (ARA: 0x0C) to talk to the unit. Here is the method a host de-asserts the SMBALET/L signal:

The host broadcasts to all the slaves on the network using ARA address 0x0C;
Only the slave that asserted the SMBALERT/L acknowledges and transmits its I^2C Device Address to the broadcasting I^2C host;

SMBUS Alert Method

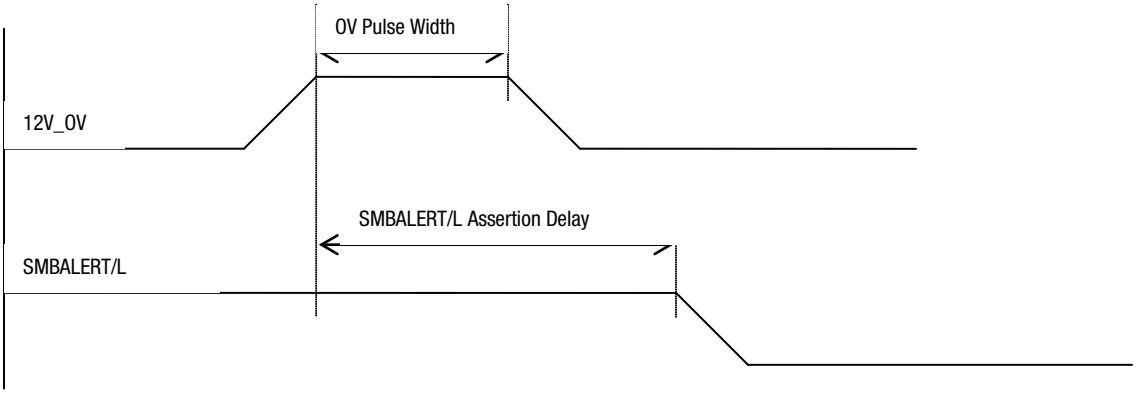
START	Slave Address	R	ACK	Device Address	ACK	P

Note: Shaded data is from slave to master

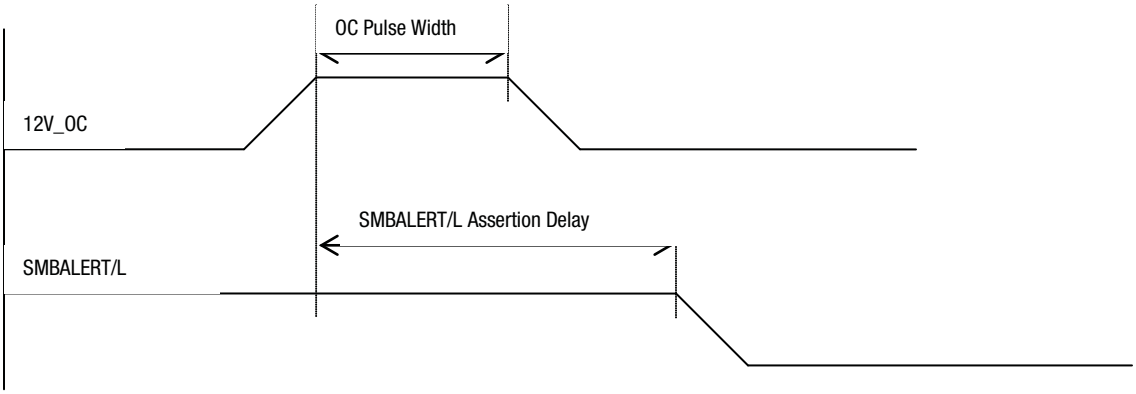
The host then talks to the received I^2C Device Address using the PSMI register 0xD5;
The PSMI register 0xD5 is a one byte command for the host to command the slave to de-assert SMBALERT/L signal;
The host could repeat the above steps until the SMBALERT/L is de-asserted; however, a slave may have repeated OT fault since OT is an auto-recoverable fault, in this case, it is the host's decision to repeat the above de-asserting steps or just let the slave take care of the SMBALERT/L signal.

Here are the timing diagrams for SMBALERT/L Assertion and De-assertion.

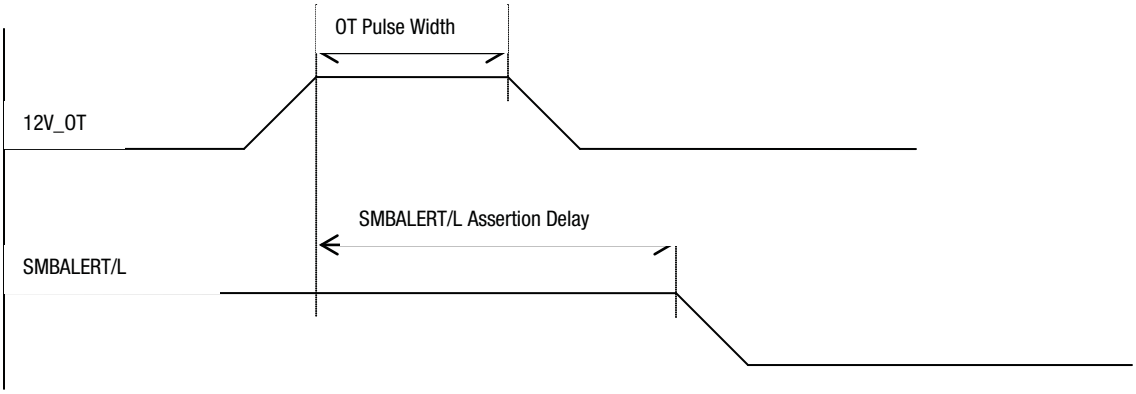
Main OV to SMBALERT/L Assertion Delay



Main OC to SMBALERT/L Assertion Delay



Main OT to SMBALERT/L Assertion Delay



I²C Command to SMBALERT/L De-assertion Delay

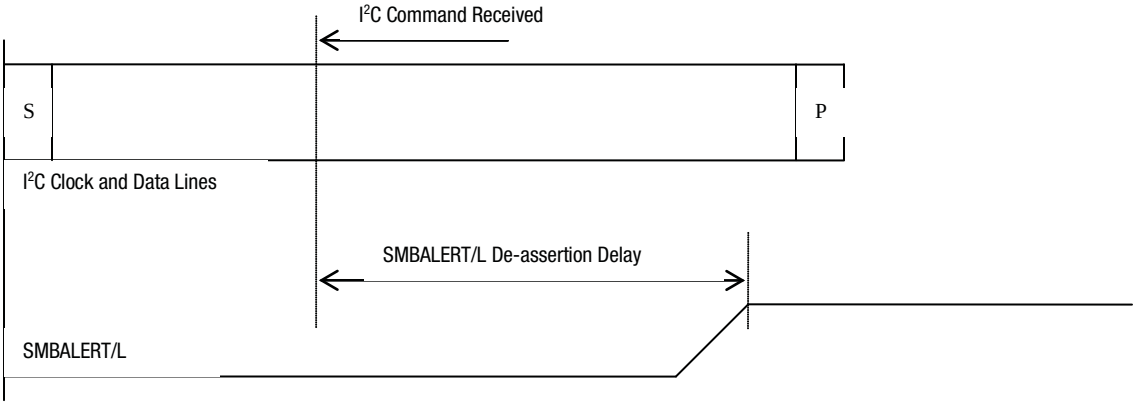


Table A4. Summary of SMBALERT/L Timing Parameters

SMBALERT Timing	Min	Max	Note
Main OV Pulse Width	200 us	-	Rise and fall times must be within spec
Main OC Pulse Width	200 us	-	Rise and fall times must be within spec
Main OT Pulse Width	200 us	-	Rise and fall times must be within spec
SMBALERT/L Assertion Delay	0	10 ms	
SMBALERT/L De-assertion delay	0	10 ms	

SMBALERT/L Signal during Power Up/Down and Turn On/Off