

PREFACE:

This application note describes the configuration of the dual function "Input_OK / Rapid_ON" signal pin and <u>cold redundant features</u> of the D1U54P-x-2000-12-HxxC-xx series power supplies.

GENERAL NOTES:

- This product series is compliant with PMBus[™] Part I and Part II Rev 1.2.
- Configuration of this signal pin requires write commands issued by host/system via the PMBus[™].
- Refer to PMBus[™] Communications Protocol Application Note <u>ACAN-81</u> for additional details.

DESCRIPTION OF DUAL FUNCTION SIGNAL PIN "C1"

Pin "C1" can be configured to operate as any one of the following two functions:

1) **INPUT_OK** (Default configuration upon initial power up):

Functions as a traditional AC_OK or DC_OK signal and is described in the following table.

If actual deployment requires the AC or DC input OK signal, then no further configuration is required as this is the initial power up default setting.

Signal Name	I/O	Description	Interface Details
		The signal output is driven high when input source is available and within acceptable	Pulled up internally via 511R to
		limits. The output is driven low to indicate loss of input power.	VDD ¹ and pulled down via 10K ²
INPUT_OK	Output	There is a minimum of 1ms pre-warning time before the signal is driven low prior to	A logic high >2.0Vdc
		the PWR_OK signal going low. The power supply must ensure that this interface	A logic low <0.8Vdc
		signal provides accurate status when AC power is lost.	Driven low by internal buffer

¹VDD is an internal bias supply, either 3.3Vdc or 5.0Vdc, depending on model, and is reduced slightly due to internal pull-up/down resistors and QTY PSUs installed with INPUT_OK signal tied together.

² It is recommended for deployments > 4 PSUs that the INPUT_OK signals be logically ORed together instead of directly tied together to maintain adequate Logic High level criteria.

2) RAPID_ON: (configured via PMBus[™]).

Rapid_ON is a bi-directional logic signal and forms the "cold redundant" (CR) bus when pin C1 of up to four (4) load sharing PSUs are connected together at the host/system. This bus is therefore required for cold redundant operation.

The system interaction with this signal must be limited to forming the cold redundant bus and not utilize this signal for other functions. This signal is controlled by the PSU as follows:

- > Pullup voltage -- the PSU assigned the roll of "COLD_REDUNDANT_ACTIVE" provides the pullup and acts as "Master" for the bus.
- > Each bus connected PSU drives the Rapid_ON bus LOW when any fault is detected.
- > Each bus connected PSU powers on its main output rapidly within 100µS after detection of LOW state on this bus.

Note: "Rapid_ON" pin configuration is retained once setup via PMBus[™], even when AC power is recycled this remains the new default setting until commanded to INPUT_OK (signal pin is thereby reconfigured to operate as an AC_OK signal)

To revert back to default INPUT_OK MODE the following command must be written:

1	7	1	1	8	1	1	8	1	1	8	1	1
S	Slave Address	WR	А	EAh	А	Ρ	69h	А	Ρ	96h	А	Ρ



RAPID_ON SIGNAL VOLTAGE LEVELS:

The signal is internally buffered by a Schmitt Trigger device. The voltage varies depending on the standby voltage (3.3V or 5.0V for example) and the QTY of PSUs connected, due to an internal 10K pull-down resistor.

Model	Standby Valtaga	Rapid_ON DC voltage level vs QTY PSUs						
MOUEI	Standby Voltage	QTY 2	QTY 3	QTY 4				
D1U54x-x-2000-12-H HAxC	5.0 Vdc	4.49 Vdc	4.23 Vdc	3.98 Vdc				
D1U54x-x-2000-12-H HBxC	3.3 Vdc	2.69 Vdc	2.79 Vdc	2.63 Vdc				
D1U54x-x-2000-12-H HCxC	5.0 Vdc	2.69 Vdc	2.79 Vdc	2.63 Vdc				

TWO COLD REDUNDANT MODE OPTIONS:

In order to accommodate a wide range of system applications, two cold redundant modes are supported:

- 1. Automatic Mode: standard Intel CRPS cold redundancy protocol, up to four (4) PSUs.
- 2. <u>Manual Mode</u>: PSU output on/off decision is made by the system/host based on PSU sensor readings via PMBus[™], and not limited to four (4) PSUs.

General requirements for a power supply operating in either of the above CR modes:

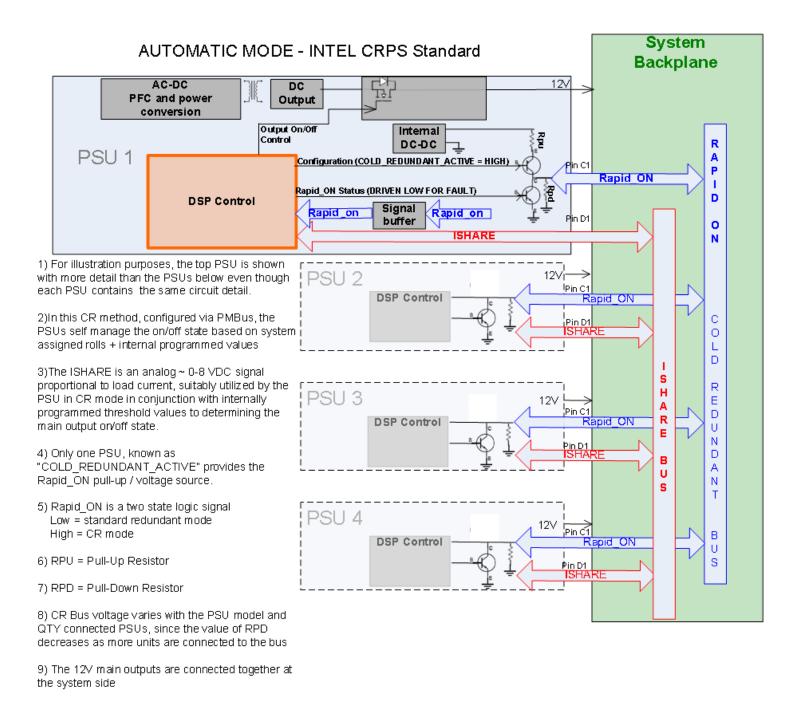
- > Turn on main output within 100µs of RAPID_ON bus being driven LOW
- > Turn off main output ORing FET
- > Maintain a pre-ORing capacitors charge level of at least 12.6V
- Keep PWOK asserted
- > Disconnect any internal parasitic loads that would otherwise cause the output cap to discharge
- > Turn off internal fan
- Pre-bias its voltage error amplifier to maximum duty cycle (preventing the loop compensation from slowing the turn on process in the event of assertion of the RAPID ON bus.
- > Disable power up soft start output circuit
- > Keep the PFC stage Operating at the lowest possible operating frequency and the bulk capacitor charged
- > No PMBus[™] fault or warning conditions reported via STATUS commands
- > PMBus[™] READ_EOUT (where supported) command shall continue to increment its sample counter and update its power accumulator
- > PMBus[™] READ_PIN command should continue to report its input power
- If RAPID_ON bus is pulled down, the operating PSU's must share load conventionally. The system must reassign the PSU rolls to restore CR mode. Link back to logic table



Automatic Mode (INTEL CRPS compliant)

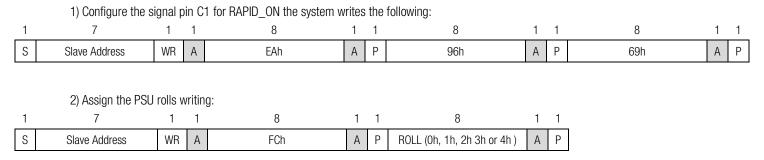
Link Back to CR options

The output on/off control is decided by the PSU based on a comparison of the voltage level of the ISHARE bus voltage and internal fixed thresholds. Once the system successfully completes the PSU roll assignment and the bus is set to active (high), the PSUs determine the output on/off status and how many PSUs share the load.





PMBus[™] COMMANDS FOR AUTOMATIC MODE LINK TO PMBUS[™] DEFINITIONS



Roll Names:

CONVENTIONAL REDUNDANCY: (BYTE 0X0h)

COLD_REDUNDANT_ACTIVE_MODE (aka MASTER): (byte 0x01h) At least one (1) PSU must be assigned this roll, aka "Always On" COLD_STANDBY_LEVEL_1: (byte 0x02h) next unit to power load as ISHARE bus increases > threshold / third to shed as load falls COLD_STANDBY_LEVEL_2: (byte 0x03h) next unit to power load as ISHARE bus increases > second threshold / second to shed as load falls COLD_STANDBY_LEVEL_3: (byte 0x04h) next unit to power load as ISHARE bus increases > third threshold / first to shed as load falls

Threshold Current ON/OFF voltage and PMBus[™] Roll Byte assignment Table:

Basic Logic table based of	on various	scenarios:	-	-	
		Threshold Current (Adc)		Natao	Description
Roll	PMBus [™] Roll Byte	ACTIVE_ON	COLD_STANDBY	Notes	Description
Standard Redundancy	0x0h	N/A	N/A	Always on; ignores RAPID_ON and maintains normal operation	Turns the power supply ON into standard redundant load sharing mode. The power supply's CR_BUS# signal shall be OPEN but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
Cold_Redundant_Active aka ACTIVE & MASTER	0x1h	_	-	Always on; ignores RAPID_ON and maintains normal operation (behaves same as conventional redundant)	 Defines this power supply to be the one that is always ON in a cold redundancy configuration. Provides the Bus Pull-up
COLD_STANDBY_1	0x2h	66.67	30	Output turns on after at load current of 66.67A, remains on until load falls below 30A	Level 1 - Defines the power supply that is first to turn of
COLD_STANDBY_2	0x3h	103.33	62.3	Output turns on after at load current of 103.33, remains on until load falls below 62.3A	
COLD_STANDBY_3	0x4h	140	94.6	current of 140A, remains on	



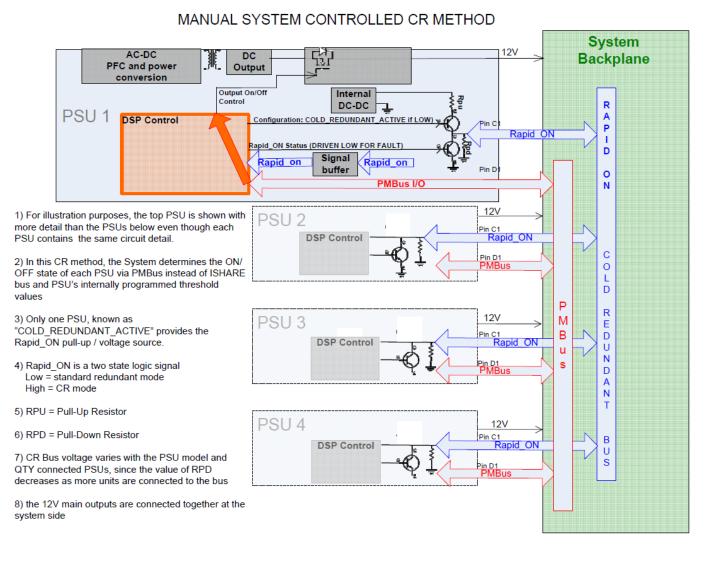
Logic table of output state:			
RAPID_ON Bus State	ISHARE Bus Voltage	Main output State	Cold redundant State
High	<vactive_on_threshold<sup>1</vactive_on_threshold<sup>	OFF	COLD_STANDBY
High	>VACTIVE_ON_threshold ¹	ON	ACTIVE_ON
Low	Doesn't Care	ON	Conventional Redundancy
¹ Is the PSI I's internally progra	ammed fixed threshold limits (determine	the on/off status) accordin	na to direction of change

¹ Is the PSU's internally programmed fixed threshold limits (determine the on/off status) according to direction of change.

Manual Mode:

Link Back to CR options

After the PSUs are installed and the MASTER & ACTIVE PSU is assigned, the system host controls the on/off status of the "non-master & active" PSU(s) via PMBus[™] as system requires, by forcing their status as ACTIVE or COLD_STANDBY. A significant feature of this cold redundant mode is that more than four (4) PSU's can be connected.





PMbus™ CONFIGURATION, MANUAL MODE COLD REDUNDANCY LINK TO PMBUS™ DEFINITIONS

1. Configure the multi-function signal pin C1 as "RAPID_ON" by:

1	7	1	1	8	1	1	8	1	1	8	1	1
S	Slave Address	W R	А	EAh	А	Ρ	96h	А	Р	69h	А	Ρ
	2. Configur	e the F	PSUs	for CR by assigning the PSU	rolls	wri	ing:					
1	7	1	1	8	1	1	8	1	1			
S	Slave Address	WR	А	FCh	А	Р	ROLL (0h, 55h, 0xEh)	А	Р			

Roll Names:

CONVENTIONAL REDUNDANCY: (BYTE 0X0h) = DEFAULT SETTTING

COLD_REDUNDANCY_FORCED_ACTIVE: (byte 0x55h) At least one (1) PSU must be assigned this roll, aka "Always On" (subsequent PSUs assigned this same roll will be known as "ACTIVE & SLAVE" and the first PSU Assigned the roll of "55" provides the bus pull-up) COLD_REDUNDANCY_FORCED_STANDBY_X: (byte 0xEh) System makes the PSU output on/off decision and write either "55h" or "Eh" as system requires. Up to 8 PSUs can be controlled in this mode.

NOTE: If the MASTER & ACTIVE PSU to a is written to mode "0x0" by host/system, the CR bus will be forced low and all connected PSUs will end CR mode and immediately share conventionally, while COLD_STANDBY_x assigned PSUs simply enter conventional current share and do not pull down the CR bus.



GENERAL COLD REDUNDANT MODE NOTES:

- 1) A COLD_STANDBY PSU can be assigned any of the three levels, for example, if system contains 2 PSUs, the 2nd COLD_STANDBY PSU can be assigned level 1, level 2 or level 3, as system may require.
- 2) PSU extraction: extraction of a PSU will not cancel CR mode as long as it is not the ACTIVE & MASTER and does not cause OCP Fault
- 3) Power supply insertion: A previously configured COLD_STANDBY PSU can be extracted and re-inserted without issue as long as AC input remains connected as the input power maintains secondary side DSP operation. Likewise if input voltage be removed, the PSU "forgets" it's CR roll and will power up as STD redundancy. In that situation, the other PSUs are operating in CR mode, and so the last PSU inserted will attempt to load share, but to what degree is indeterminate. Therefore that PSU roll needs to be reassigned.
- 4) Recycling of AC or DC input: ACTIVE & MASTER = will cause bus to collapse and cancel CR mode. The other PSUs will turn on their main outputs and share load conventionally. If a COLD_STANDBY unit has it's input recycled, CR operation will continue and the connected PSUs will maintain their status/roll.. Again, upon applying the input voltage, this PSU will need it's roll reassigned + load share degree is indeterminate.
- 5) System can cancel CR mode and force standard redundancy by re-assigning ACTIVE & MASTER PSU as Cold_Standby_x (roll byte: CMD_0x0h)
- 6) PMBus[™] warnings do not clear the RAPID_ON bus or end CR Mode, only faults clear the bus.
- 7) ROLL reassignment: The PSUs can be reassigned their rolls only after clearing the RAPID_ON bus (cancelling CR mode).
- 8) "Cold_Redundant_x" Rolls a PSU can be assigned either of the three "x" levels, useful in deployments of <4 PSUs.
- 9) The first PSU roll assigned must be assigned roll COLD_REDUNDANT_ACTIVE / ACTIVE & MASTER
- 10) Once the COLD_REDUNDANT_ACTIVE / ACTIVE & MASTER has been set, the Rapid_ON bus must be cleared in order to reassign this roll.
- 11) Conventional sharing mode is activated (CR mode cancelled) upon any of these events:
 - a. PSU fault (Assertion of the RAPID_ON signal, causing all PSU's to be on within 100uS)
 - b. Reassigning the Active & Master PSU to Cold_Redundant_x via Roll via PMBus™
 - c. Loss of input power to the COLD_REDUNDANT_ACTIVE / ACTIVE & MASTER PSU
 - d. Extracting COLD_REDUNDANT_ACTIVE / ACTIVE & MASTER PSU
- 12) Indicators of CR mode operation:

Visual indication PMBus [™] register & or visual	ACTIVE_MASTER / ACTIVE & SLAVE COLD REDUNDANT ACTIVE	COLD STBY / FORCED STBY
LED (Visual)	On Solid	Blinks 2hz
Fan (PMBus™)	Fan rotation	No fan rotation
Output current main (PMBus™)	Output load detected	No load current
Main output voltage (PMBus™)	12.0 VDC output	Trimmed to 12.3 – 12.4VDC (compensates for ORING drop)

GENERAL DESCRIPTION AND POSSIBLE BENEFITS OF COLD REDUNDANCY:

Cold redundancy is a specific mode of current sharing in a redundant system where the load demand is light for prolonged periods of time. CR provides a means of shedding PSUs when load is light, while maintaining the ability to rapidly power on as demand increases, without loss of load voltage or system operations. The main potential benefit is that PSUs, because they share a higher load, operate at a higher efficiency.

Cold redundant features of this PSU series enable the host system with a method of improving efficiency under light loading conditions in redundant configurations such as 1+1, 2+1, 3+1 or 2+2 without compromising fault tolerance and redundancy.

Automatic CR mode also reduces the system CPU demand and resources since the PSUs self-manage the on/off optimization. Back to Overview



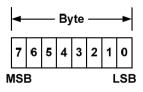
RELATED DOCUMENTS & APPLICATION NOTES					
Document Number	Description	Link			
ACAN-81	D1U54P-x-2000 Communication Protocol	http://power.murata.com/datasheet?/data/apnotes/acan-81.pdf			
D1U54P-x-2000-12-HxxC-xx	Product datasheet	http://www.murata-ps.com/datasheet?http://www.murata-ps.com/data/acdcsupplies/cps_d1u-w-2000.pdf			

Link back to Overview

PMBus[™] Protocol Definitions (Reference PMBus part 1 Revision V1.1) (Back to configuration details)

Symbol	Meaning
7	A vertical rectangle indicates a single bit sent from the host (bus master) to a slave
7	A vertical rectangle with a shaded interior indicates a bit sent from a slave device to the bus master.
7	A rectangle with a number over it represents one or more bits, as indicated by the number
s	The START condition sent from a bus master device
S r	A REPEATED START condition sent from a bus master device

Symbol	Meaning
Α	An Acknowledge (ACK) condition send from the host
N A	A Not Acknowledge (NACK) condition sent from the host
Α	An Acknowledge (ACK) condition sent from a slave device
NA	A Not Acknowledge (NACK) condition sent from a slave device
Ρ	A STOP condition sent by a bus master device
7 SLAVE ADDRESS	The first seven bits of the address byte, generally corresponding to the physical address of the device.
R	The bit [0] of the address byte with a value of 1, indicating the device is being addressed with a read.
w	The bit [0] of the address byte with a value of 0, indicating the device is being addressed with a write.
7 BROADCAST ADDRESS	The SMBus broadcast address to which all devices must respond. The value is 000000b. This is always used only with the bit [0] equal to 0 (write).



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