

## Intel VRM 10.2 DCAN-60 by Wisam Moussa, Ph.D.

### Scope

This application note applies to the Murata Power Solutions VR10.x Series Voltage Regulator Modules (VRMs), designed to meet Intel's VRM 10.2 Specifications. The data sheet is available at [murata-ps.com/data/power/cps/odc\\_vr102b150cu-3c.pdf](http://murata-ps.com/data/power/cps/odc_vr102b150cu-3c.pdf).

With the noted exception, these Voltage Regulator Modules from Murata Power Solutions utilize the ADP3188 Controller from OnSemi (formerly Analog Devices).

Note: The following information has been excerpted from the Analog Devices datasheet for the ADP3188, for the sole purpose of providing applications support to users of the VR10.1 or VR10.2 VRM modules from Murata Power Solutions.

The ADP3188 is a highly efficient, multiphase, synchronous buck switching regulator controller optimized for converting a 12V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.8375V and 1.6V.

### Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in the following table (see table 1 below, from the ADP3188 datasheet).

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor RB and is used for sensing and controlling the output voltage at this point. A current source (equal to IREF) from the FB pin flowing through RB is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

### Dynamic VID

The ADP3188 has the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3188 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time prevents a false code due to logic skew while the six VID inputs are changing. Additionally, the first VID change initiates the PWRGD and crowbar blanking functions for a minimum of 100  $\mu$ s to prevent a false PWRGD or crowbar event. Each VID change resets the internal timer.

### LL0, LL1

These pins are used to adjust the load line for the VRM10.2 module, as per Intel's spec.

### Recommended Bulk Capacitance

The recommended Bulk Output Capacitance for the VRM10.2 applications are: 16x UCC 4PS560MH11 or equivalent. These caps need to be placed close to the connector to minimize any distributed inductance.

For more information, please contact:  
Wisam Moussa, Ph.D.  
Director, Global Field Applications

 **Murata Power Solutions**

Office: (919) 388-4210



**Table 1 - VRM10.2 DAC Codes**

VID4	VID3	VID2	VID1	VID0	VID5	Output	VID4	VID3	VID2	VID1	VID0	VID5	Output
1	1	1	1	1	1	No CPU	1	1	0	1	0	0	1.2125 V
1	1	1	1	1	0	No CPU	1	1	0	0	1	1	1.2250 V
0	1	0	1	0	0	0.8375 V	1	1	0	0	1	0	1.2375 V
0	1	0	0	1	1	0.8500 V	1	1	0	0	0	1	1.2500 V
0	1	0	0	1	0	0.8625 V	1	1	0	0	0	0	1.2625 V
0	1	0	0	0	1	0.8750 V	1	0	1	1	1	1	1.2750 V
0	1	0	0	0	0	0.8875 V	1	0	1	1	1	0	1.2875 V
0	0	1	1	1	1	0.9000 V	1	0	1	1	0	1	1.3000 V
0	0	1	1	1	0	0.9125 V	1	0	1	1	0	0	1.3125 V
0	0	1	1	0	1	0.9250 V	1	0	1	0	1	1	1.3250 V
0	0	1	1	0	0	0.9375 V	1	0	1	0	1	0	1.3375 V
0	0	1	0	1	1	0.9500 V	1	0	1	0	0	1	1.3500 V
0	0	1	0	1	0	0.9625 V	1	0	1	0	0	0	1.3625 V
0	0	1	0	0	1	0.9750 V	1	0	0	1	1	1	1.3750 V
0	0	1	0	0	0	0.9875 V	1	0	0	1	1	0	1.3875 V
0	0	0	1	1	1	1.0000 V	1	0	0	1	0	1	1.4000 V
0	0	0	1	1	0	1.0125 V	1	0	0	1	0	0	1.4125 V
0	0	0	1	0	1	1.0250 V	1	0	0	0	1	1	1.4250 V
0	0	0	1	0	0	1.0375 V	1	0	0	0	1	0	1.4375 V
0	0	0	0	1	1	1.0500 V	1	0	0	0	0	1	1.4500 V
0	0	0	0	1	0	1.0625 V	1	0	0	0	0	0	1.4625 V
0	0	0	0	0	1	1.0750 V	0	1	1	1	1	1	1.4750 V
0	0	0	0	0	0	1.0875 V	0	1	1	1	1	0	1.4875 V
1	1	1	1	0	1	1.1000 V	0	1	1	1	0	1	1.5000 V
1	1	1	1	0	0	1.1125 V	0	1	1	1	0	0	1.5125 V
1	1	1	0	1	1	1.1250 V	0	1	1	0	1	1	1.5250 V
1	1	1	0	1	0	1.1375 V	0	1	1	0	1	0	1.5375 V
1	1	1	0	0	1	1.1500 V	0	1	1	0	0	1	1.5500 V
1	1	1	0	0	0	1.1625 V	0	1	1	0	0	0	1.5625 V
1	1	0	1	1	1	1.1750 V	0	1	0	1	1	1	1.5750 V
1	1	0	1	1	0	1.1875 V	0	1	0	1	1	0	1.5875 V
1	1	0	1	0	1	1.2000 V	0	1	0	1	0	1	1.6000 V

Reference: Table 4, page 12 of the ADP3188 data sheet

Murata Power Solutions, Inc.  
 11 Cabot Boulevard, Mansfield, MA 02048-1151 U.S.A.  
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