Murata Power Solutions

Application Note

Tracking/Sequence for Point-of-Load DC/DC Converters
DCAN-61

PoL Power Sequencing

Whereas in the old days, one master switch simultaneously turned on the power for all parts of a system, many modern systems require multiple supply voltages for different on-board sections. Typically the CPU or microcontroller needs 1.8 Volts or lower. Memory (particularly DDR) may use 1.8 to 2.5 Volts. Interface "glue" and "chipset" logic might use +3.3Vdc power while Input/Output subsystems may need +5V. Finally, peripherals use 5V and/or 12V.

Timing is Everything

This mix of system voltages is being distributed by several local power solutions including Point-of-load (POL) DC/DC converters and sometimes a linear regulator, all sourced from a master AC power supply. While this mix of voltages is challenging enough, a further difficulty is the start-up and shutdown timing relationship between these power sources and relative voltage differences between them.

For many systems, the CPU and memory must be powered up, boot-strap loaded and stabilized before the I/O section is turned on. This avoids uncommanded data bytes being transferred, compromising an active external network or placing the I/O section in an undefined mode. Or it keeps bad commands out of disk and peripheral controllers until they are ready to go to work.

Another goal for staggered power-up is to avoid an oversize load applied to the master source all at once. A more serious reason to manage the timing and voltage differences is to avoid either a latchup condition in programmable logic (a latchup might ignore commands or would respond improperly to them) or a high current startup situation (which may damage on-board circuits). And on the power down phase, inappropriate timing or voltages can cause interface logic to send a wrong "epitaph" command.

Two Approaches

There are two ways to manage these timing and voltage differences. Either the power up/down sequence can be controlled by discrete On/Off logic controls for each power supply (see Figure 1). Or the power up/down cycle is set by Sequencing or Tracking circuits. Some systems combine both methods.

The first system (discrete On/Off controls) applies signals from an already-powered logic sequencer or dedicated microcontroller which turns on each downstream power section in cascaded series. This of course assumes all POL's have On/Off controls. A distinct advantage of the sequencing controller is that it can produce an "All On" output signal to state that the full system is stable and ready to go to work. For additional safety, the sequencer can monitor the output voltages of all downstream POL's with an A/D converter system.

However the sequencer controller has some obvious difficulties besides extra cost, wiring and programming complexity. First, power is applied as a fast-rising, all-or-nothing step which may be unacceptable to certain circuits, especially large output bypass capacitors. These could force POL's into over-current shutdown. And some circuits (such as many linear regulators and some POL's) may not have convenient start-up controls. This requires designing and fabricating external power controls such as high-current MOSFET's.

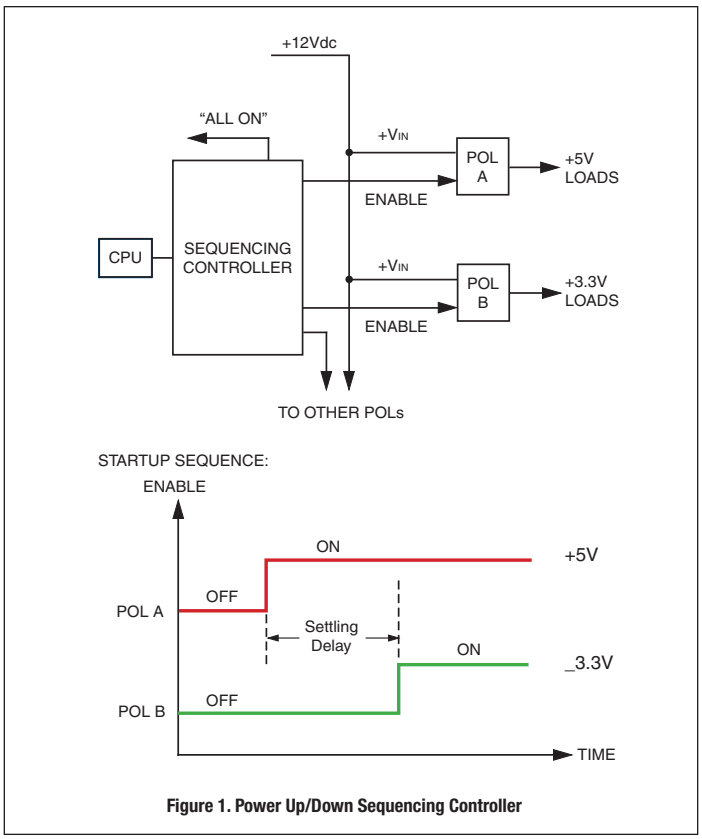

Figure 1. Power Up/Down Sequencing Controller

If the power up/down timing needs to be closely controlled, each POL must be characterized for start-up and down times. These often vary—one POL may stabilize in 15 milliseconds whereas another takes 50 milliseconds. Another problem is that the sequencing controller itself must be "already running" and stabilized before starting up other circuits. If there is a glitch in the system, the power up/down sequencer could get out of step with possible disastrous results. Lastly, changing the timing may require reprogramming the logic sequencer or rewriting software.

Sequence/Track Input

A different power sequencing solution is employed on Murata Power Solutions' PoL DC/DC converter. After external input power is applied and the converter stabilizes, a high impedance Sequence/Track input pin accepts an external analog voltage. The output power voltage will then track this Sequence/Track input at a one-to-one ratio up to the nominal set point voltage for that

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converter. This Sequencing input may be ramped, delayed, stepped or otherwise phased as needed for the output power, all fully controlled by the user's simple external circuits. As a direct input to the converter's feedback loop, response to the Sequence/Track input is very fast (milliseconds).

By properly controlling this Sequence pin, most operations of the discrete On/Off logic sequencer may be duplicated. The Sequence pin system does not use the converter's Enable On/Off control (unless it is a master emergency shut down system).

Power Phasing Architectures

Observe the simplified timing diagrams below. There are many possible power phasing architectures and these are just some examples to help you analyze your system. Each application will be different. Multiple output voltages may require more complex timing than that shown here.

These diagrams illustrate the time and slew rate relationship between two typical power output voltages. Generally the Master will be a primary power voltage in the system which must be present first or coincident with any Slave power voltages. The Master output voltage is connected to the Slave's Sequence input, either by a voltage divider, divider-plus-capacitor or some other method. Several standard sequencing architectures are prevalent. They are concerned with three factors:

- The time relationship between the Master and Slave voltages
- The voltage difference relationship between the Master and Slave
- The voltage slew rate (ramp slope) of each converter's output.

For most systems, the time relationship is the dominant factor. The voltage difference relationship is important for systems very concerned about possible latchup of programmable devices or overdriving ESD diodes. Lower slew rates avoid overcurrent shutdown during bypass cap charge-up.

In Figure 2, two POL's ramp up at the same rate until they reach their different respective final set point voltages. During the ramp, their voltages are nearly identical. This avoids problems with large currents flowing between logic systems which are not initialized yet. Since both end voltages are different, each converter reaches it's setpoint voltage at a different time.

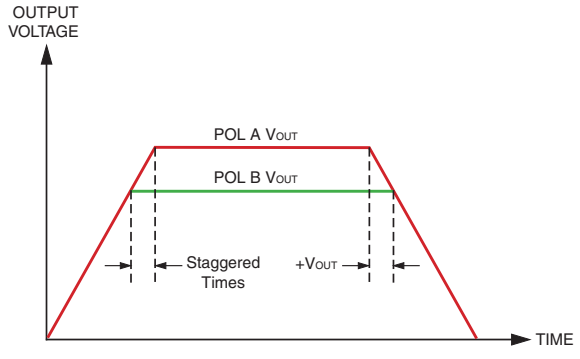

Figure 2. Coincident or Simultaneous Phasing (Identical Slew Rates)

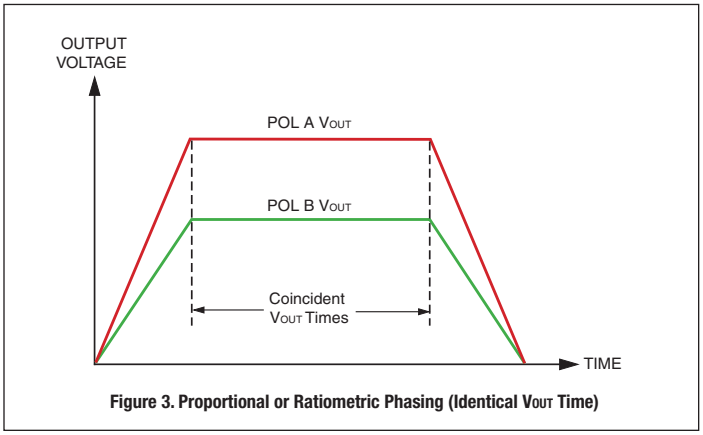

Figure 3. Proportional or Ratiometric Phasing (Identical VOUT Time)

Figure 3 shows two POL's with different slew rates in order to reach differing final voltages at about the same time.

Figures 4 and 5 show both delayed start up and delayed final voltages for two converters. Figure 4 is called "Inclusive" because the later starting POL finishes inside the earlier POL. The timing in Figure 4 is more easily built using a combined digital sequence controller and the Sequence/Track pin.

Figure 5 is the same strategy as Figure 4 but with an "exclusive" timing relationship staggered approximately the same at power-up and power-down.

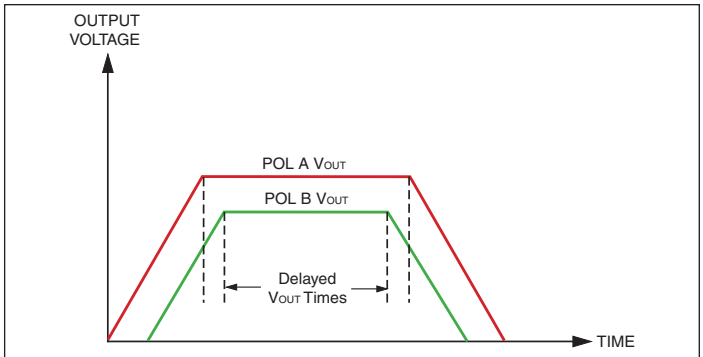

Figure 4. Staggered or Sequential Phasing—Inclusive (Fixed Delays)

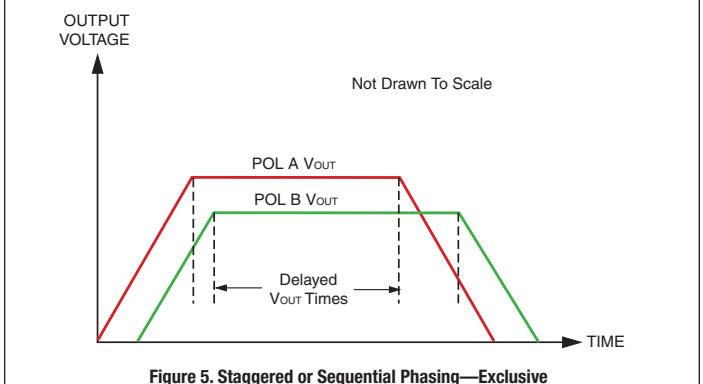

Figure 5. Staggered or Sequential Phasing—Exclusive (Fixed Cascaded Delays)

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