Murata Power Solutions

LSN2-T/22-D12

Non-isolated, DOSA-SIP,
22A Selectable-Output DC/DC Converters

Discontinued

ORDERING GUIDE SUMMARY					
Model	**V_{OUT} Range**	**I_{OUT} Range**	**V_{IN} Range**	**Ripple/Noise**	**Efficiency**
LSN2-T/22-D12	0.8-5V	0-22A	8.3-14V	35mVpk-pk	95%

FEATURES

- User-selectable outputs: 0.8-5V
- 22 Amps maximum output current
- Double lead free to RoHS standards
- Selectable phased start-up sequencing and tracking
- Wide range V_{IN} 8.3-14V
- Up to 112 Watts total output power
- Very high efficiency up to 94%
- Starts up into pre-biased load
- Fast settling, high di/dt I_{OUT} slew rate

DESCRIPTION

These miniature point-of-load (POL) switching DC/DC converters are ideal regulation and supply elements for mixed voltage systems. Fully compatible with the Distributed-power Open Standards Alliance specification (www.dosa-power.com), LSN2's can power CPU's, programmable logic and mixed-voltage systems with little heat and low noise. A typical application uses a master isolated 12Vdc supply and individual LSN2 converters for local 1.8 and 3.3Vdc supplies. All system isolation resides in the central supply, leaving lower cost POL regulation at the load. The LSN2's can deliver very high power (to 112 Watts) in a tiny area without heat sinking or external components. They feature quick transient response (to 25µsec) and very fast current slew rates (to 20A/µsec).

INPUT CHARACTERISTICS		
Parameter	Typ. @ 25°C, full load	Notes
Voltage Range	8.3-14V	12V nominal
Current, full power	8.77A	
Undervoltage Shutdown	Included	With autorestart hysteresis
Short Circuit Current	60mA	Output is short circuited
Remote On/Off Control	Positive or negative polarity	Default polarity is positive

OUTPUT CHARACTERISTICS		
Parameter	Typ. @ 25°C, full load	Notes
Voltage	0.8-5V	User adjustable
Current	0-22A	
Power Output	112W max.	
Accuracy	±2% of V_{NOM}	50% load
Ripple & Noise	35mVpp	
Line and Load Regulation (max.)	±0.1% / ±0.3%	
Overcurrent Protection	Hiccup autorecovery	Continuous short circuit protection
Overtemperature Protection	+115°C shutdown	
Efficiency (minimum)	94%	
Efficiency (typical)	95%	

GENERAL SPECIFICATIONS		
Parameter	Typ. @ 25°C, full load	Notes
Transient Response	40µsec	50% load step to 2% of final value
Operating Temperature Range	–40 to +60°C	With 200 lfm airflow
Safety	UL/IEC/EN 60950	And CSA C22.2-No.60950
EMI, Conducted/Radiated	FCC pt.15, class B	May require external filter

MECHANICAL CHARACTERISTICS	
22 Amp model	0.50 x 2.00 x 0.38 inches (12.7 x 50.8 x 9.653 mm)

RoHS COMPLIANT

For full details go to www.murata-ps.com/rohs

Lead-free construction/attach

DOSA Distributed-power Open Standards Alliance

PERFORMANCE SPECIFICATIONS AND ORDERING GUIDE ①

Model ⑦	Output							Input			Efficiency		Package (Case/ Pinout)
	V_{OUT} (Volts)	I_{OUT} (Amps)	Power (Watts)	R/N (mVp-p) ②		Regulation (max.) ③		V_{IN} Nom. (Volts)	Range (Volts)	I_{IN} ④ (mA/A)	V_{OUT} = 5V		
				Typ.	Max.	Line	Load				Min.	Typ.	
LSN2-T/22-D12 ⑤	0.8-5	22 ⑥	112	35	50	±0.1%	±0.3%	12	8.3-14	100/8.77	93.5%	95%	B14, P68

① Typical at T_A = +25°C under nominal line voltage and full-load conditions, unless noted. All models are tested and specified with external 22µF tantalum input and 1 ‖ 10µF output capacitors. These capacitors are necessary for our test equipment and may not be required to achieve specified performance in your applications. See I/O Filtering and Noise Reduction.

② Ripple/Noise (R/N) is tested/specified over a 20MHz bandwidth and may be reduced with external filtering. See I/O Filtering and Noise Reduction for details. R/N specs are shown at V_{OUT} = +1V

③ These devices have no minimum-load requirements and will regulate under no-load conditions. Regulation specifications describe the output-voltage deviation as the line voltage or load is varied from its nominal/midpoint value to either extreme.

④ Nominal line voltage, no-load/full-load conditions.

⑤ LSN2-T/22-D12 efficiencies are shown at 5V_{OUT}.

⑥ Max. output current is 20 Amps with $V_{OUT} \geq$ 3.3V.

⑦ This is an incomplete model number. Please refer to the Part Number Structure when ordering.

PART NUMBER STRUCTURE

L SN2 - T / 22 - D12 N B G - C

Output Configuration:
L = Unipolar Low Voltage

Non-Isolated SIP

Nominal Output Voltage:
0.8-5 Volts (D12)

Maximum Rated Output
Current in Amps

Input Voltage Range:
D12 = 8.3-14 Volts (12V nominal)

On/Off Polarity:
Blank = Positive polarity
N = Negative polarity

VTRACK/Sequence:
Blank = Installed
B = is not installed

Power Good Output:
Blank = Omitted
G = Installed

RoHS-6 compliant*

*Contact Murata Power Solutions (DATEL) for availability.

Note:
Not all model number combinations are available. Contact Murata Power Solutions (DATEL).

Performance/Functional Specifications (1)

INPUT	
Input Voltage Range	See Ordering Guide
Isolation	Not isolated, input and output commons are internally connected
Start-Up Threshold	8.1 Volts
Undervoltage Shutdown	7.5 Volts
Overvoltage Shutdown	None
Reflected (Back) Ripple Current (2)	20mAp-p
Internal Input Filter Type	Capacitive
Reverse Polarity Protection	See fuse information
Recommended External Fuse	25 Amps
Input Current:	
Full Load Conditions	See Ordering Guide
Inrush Transient	$0.4A^2sec$
Shutdown Mode (Off, UV, OT)	5mA
Output Short Circuit	60mA
No Load	100mA, 5VOUT
Low Line (VIN = VMIN)	12.62 Amps
Remote On/Off Control: (5)	
Positive Logic (no model suffix)	OFF = ground pin to +0.3V max. ON = open pin or +2.5V min. to +VIN max.
Negative Logic ("N" model suffix)	ON = 0 to +0.3V max. OFF = open pin or +2.5V min. to +VIN max.
Current	1mA max.

OUTPUT	
Voltage Output Range	See Ordering Guide
Minimum Loading	No minimum load
Accuracy (50% load)	±2% of VNOM
Voltage Adjustment Range (13)	See Ordering Guide
Temperature Coefficient	±0.02% of VOUT range per °C
Ripple/Noise (20 MHz bandwidth)	See Ordering Guide and (8)
Line/Load Regulation (See Tech Notes)	See Ordering Guide and (10)
Efficiency	See Ordering Guide
Maximum Capacitive Loading: (15)	
Cap-ESR = 0.001 to 0.01Ω	2000µF
Cap-ESR >0.01Ω	10,000µF
Current Limit Inception: (98% of VOUT)	45 Amps (cold startup) 43 Amps (after warm up)
Short Circuit Mode (6)	
Short Circuit Current Output	600mA
Protection Method (17)	Hiccup autorecovery on overload removal
Short Circuit Duration	Continuous, no damage (output shorted to ground)
Prebias Startup (16)	Converter will start up if the external output voltage is less than VSET
Sequencing (Omit "B" model suffix)	
Slew Rate	2V max. per millisecond
Startup delay until sequence start	10 milliseconds
Tracking accuracy, rising input	VOUT = ±200mV max. of Sequence In
Tracking accuracy, falling input	VOUT = ±400mV max. of Sequence In
Sequence pin input impedance	1MΩ
Remote Sense to VOUT	0.5V max. (7)
Power Good Output (14)	TRUE (OK) = open drain
("G" suffix)	FALSE (not OK) = Signal Ground to 0.4V
Power_Good Configuration	MOSFET to ground with external user pullup, 10mA max. sink

DYNAMIC CHARACTERISTICS	
Dynamic Load Response (50-100-50% load step, di/dt = 20A/µsec)	40µsec to ±2% of final value
Start-Up Time (VIN on to VOUT regulated or On/Off to VOUT)	7msec for VOUT = nominal
Switching Frequency	250 ±30kHz

ENVIRONMENTAL	
Calculated MTBF (4)	TBC Hours
Operating Temperature Range See Derating Curves	–40 to +85°C with derating
Operating PC Board Temperature	–40 to +100°C max. (12)
Storage Temperature Range	–55 to +125°C
Thermal Protection/Shutdown	+115°C
Relative Humidity	To 85°C/85% RH, non-condensing

PHYSICAL	
Outline Dimensions	See Mechanical Specifications
Weight	0.28 ounces (7.8 grams)
Pin Material	Tin plate over copper alloy
Electromagnetic Interference (conducted and radiated)	FCC part 15, class B, EN55022 (may need external filter)
Safety	UL/cUL 60950-1 CSA-C22.2 No.60950-1 IEC/EN 60950-1
Flammability Rating	UL94V-0

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Continuous or transient)	+15 Volts
On/Off Control	–0V min. to +VIN max.
Input Reverse Polarity Protection	See Fuse section
Output Current (7)	Current-limited. Devices can withstand sustained short circuit without damage.
Storage Temperature	–55 to +125°C
Lead Temperature (soldering 10 sec. max.)	+280°C

These are stress ratings. Exposure of devices to any of these conditions may adversely affect long-term reliability. Proper operation under conditions other than those listed in the Performance/Functional Specifications Table is not implied.

Performance/Functional Specification Notes:

(1) All models are tested and specified with external 1 || 10µF ceramic/tantalum output capacitors and a 22µF external input capacitor. All capacitors are low ESR types. These capacitors are necessary to accommodate our test equipment and may not be required to achieve specified performance in your applications. All models are stable and regulate within spec under no-load conditions.

General conditions for Specifications are +25°C, VIN = nominal, VOUT = nominal, full load. "Nominal" output voltage is +5V.

(2) Input Back Ripple Current is tested and specified over a 5-20MHz bandwidth. Input filtering is CIN = 2 x 100µF tantalum, CBUS = 1000µF electrolytic, LBUS = 1µH.

(3) Note that Maximum Power Derating curves indicate an average current at nominal input voltage. At higher temperatures and/or lower airflow, the DC/DC converter will tolerate brief full current outputs if the total RMS current over time does not exceed the derating curve.

(4) Mean Time Before Failure is calculated using the Telcordia (Belcore) SR-332 Method 1, Case 3, ground fixed conditions, TPCBOARD = +25°C, full output load, natural air convection.

(5) The On/Off Control may be driven with external logic or by applying appropriate external voltages which are referenced to –Input Common. The On/Off Control Input should use either an open collector/open drain transistor or logic gate which does not exceed +VIN. A 68KΩ external pullup resistor to +VIN will cause the "ON" state for negative logic models.

(6) Short circuit shutdown begins when the output voltage under increasing load degrades approximately 2% from the selected setting.

Performance/Functional Specification Notes:

(7) If Sense is connected remotely at the load, up to 0.5 Volts difference is allowed between the Sense and +VOUT pins to compensate for ohmic voltage drop in the power lines. A larger voltage drop may cause the converter to exceed maximum power dissipation.

(8) Output noise may be further reduced by adding an external filter. See I/O Filtering and Noise Reduction.

(9) All models are fully operational and meet published specifications, including "cold start" at –40°C. The package temperature of all on-board components must not exceed +128°C.

(10) Regulation specifications describe the deviation as the line input voltage or output load current is varied from a nominal midpoint value to either extreme.

(11) Other input or output voltage ranges are available under scheduled quantity special order.

(12) Maximum PC board temperature is measured with the sensor in the center.

(13) Do not exceed maximum power specifications when adjusting the output trim.

(14) When Sequencing is not used, the Power Good output is TRUE at any time the output is within approximately ±10% of the voltage set point. Power Good basically indicates if the converter is in regulation. Power Good detects Over Temperature if the PWM has shut down due to OT. Power Good does not directly detect Over Current.

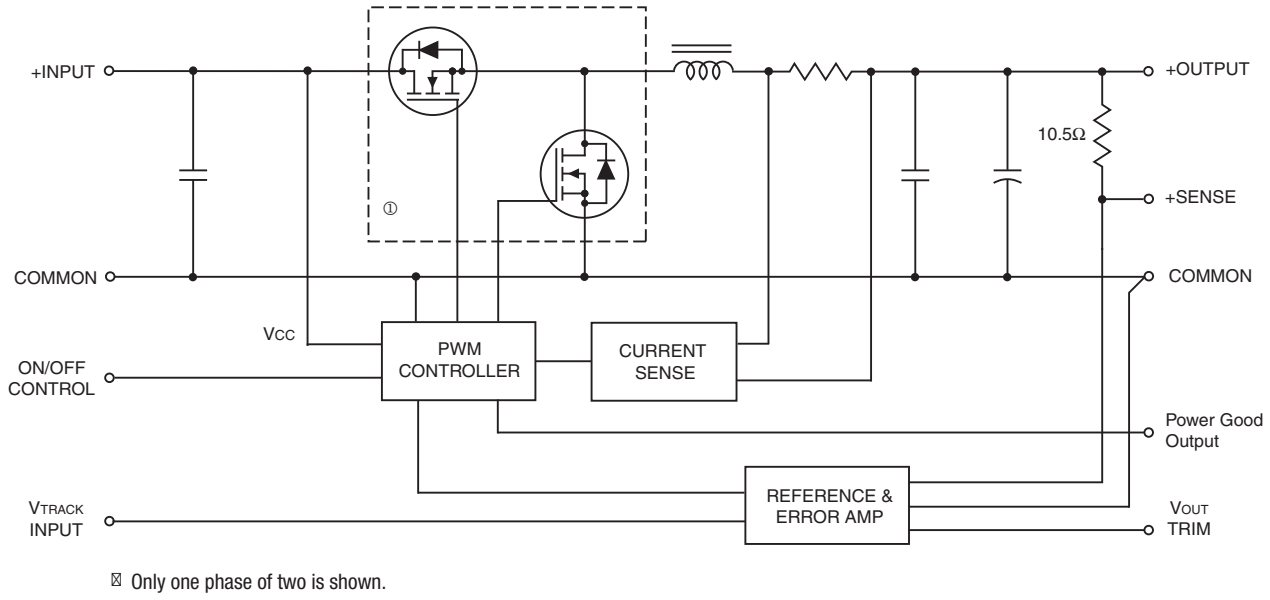
If Sequencing is in progress, Power Good will falsely indicate TRUE (valid) before the output reaches its setpoint. Ignore Power Good if Sequencing is in transition.

(15) The maximum output capacitive loads depend on the the Equivalent Series Resistance (ESR) of the external output capacitor. Use only as much output filtering as needed *and no more*. Low ESR ceramic caps may degrade dynamic performance. Thoroughly test your system under full load with all components installed.

(16) Do not use Pre-bias startup and sequencing together. See Technical Notes below.

(17) After short circuit shutdown, if the load is partially removed such that the load still exceeds the overcurrent (OC) detection, the converter will remain in hiccup restart mode.

(18) For best noise performance, leave the Track/Sequence pin OPEN when not used.



① Only one phase of two is shown.

Figure 1. LSN2 Series Simplified Schematic

TECHNICAL NOTES

I/O Filtering and Noise Reduction

All models in the LSN2 Series are tested and specified with external 1 || 10µF ceramic/tantalum output capacitors and a 22µF tantalum input capacitor. These capacitors are necessary to accommodate our test equipment and may not be required to achieve desired performance in your application. The LSN2's are designed with high-quality, high-performance internal I/O caps, and will operate within spec in most applications with no additional external components.

In particular, the LSN2's input capacitors are specified for low ESR and are fully rated to handle the units' input ripple currents. Similarly, the internal output capacitors are specified for low ESR and full-range frequency response.

In critical applications, input/output ripple/noise may be further reduced using filtering techniques, the simplest being the installation of external I/O caps.

External input capacitors serve primarily as energy-storage devices. They minimize high-frequency variations in input voltage (usually caused by IR drops in conductors leading to the DC/DC) as the switching converter draws pulses of current. Input capacitors should be selected for bulk capacitance (at appropriate frequencies), low ESR, and high rms-ripple-current ratings. The switching nature of modern DC/DC's requires that the dc input voltage source have low ac impedance at the frequencies of interest. Highly inductive source impedances can greatly affect system stability. Your specific system configuration may necessitate additional considerations.

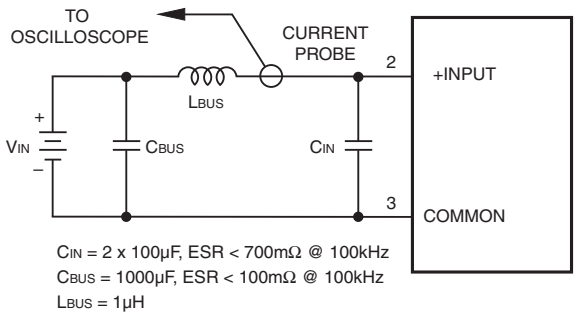


Figure 2. Measuring Input Ripple Current

Output ripple/noise (also referred to as periodic and random deviations or PARD) may be reduced below specified limits with the installation of additional external output capacitors. Output capacitors function as true filter elements and should be selected for bulk capacitance, low ESR, and appropriate frequency response. Any scope measurements of PARD should be made directly at the DC/DC output pins with scope probe ground less than 0.5" in length.

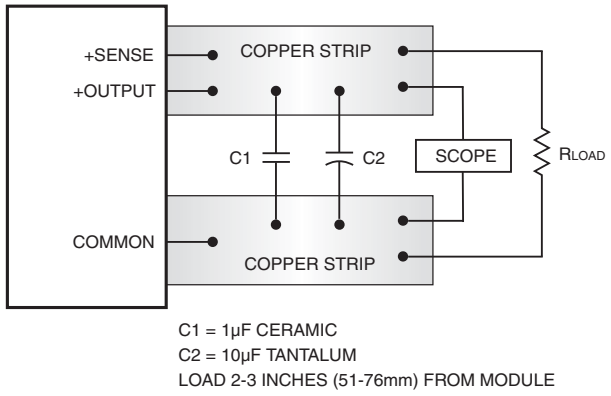


Figure 3. Measuring Output Ripple/Noise (PARD)

All external capacitors should have appropriate voltage ratings and be located as close to the converters as possible. Temperature variations for all relevant parameters should be taken into consideration.

The most effective combination of external I/O capacitors will be a function of your line voltage and source impedance, as well as your particular load and layout conditions. Our Applications Engineers can recommend potential solutions and discuss the possibility of our modifying a given device's internal filtering to meet your specific requirements. Contact our Applications Engineering Group for additional details.

Input Fusing

Most applications and or safety agencies require the installation of fuses at the inputs of power conversion components. The LSN2 Series are not internally fused. Therefore, if input fusing is mandatory, either a normal-blow or a slow-blow fuse with a value no greater than twice the maximum input current calculated at low line with the converter's minimum efficiency should be installed within the ungrounded input path to the converter.

Safety Considerations

LSN2 SIPs are non-isolated DC/DC converters. In general, all DC/DC's must be installed, including considerations for I/O voltages and spacing/separation requirements, in compliance with relevant safety-agency specifications (usually UL/IEC/EN60950).

In particular, for a non-isolated converter's output voltage to meet SELV (safety extra low voltage) requirements, its input must be SELV compliant. If the output needs to be ELV (extra low voltage), the input must be ELV.

Input Overvoltage and Reverse-Polarity Protection

LSN2 SIP Series DC/DC's do not incorporate either input overvoltage or input reverse-polarity protection. Input voltages in excess of the specified absolute maximum ratings and input polarity reversals of longer than "instantaneous" duration can cause permanent damage to these devices.

Start-Up Time

The V_{IN} to V_{OUT} Start-Up Time is the interval between the time at which a ramping input voltage crosses the lower limit of the specified input voltage range and the fully loaded output voltage enters and remains within its specified accuracy band. Actual measured times will vary with input source impedance, external input capacitance, and the slew rate and final value of the input voltage as it appears to the converter.

The On/Off to V_{OUT} Start-Up Time assumes the converter is turned off via the On/Off Control with the nominal input voltage already applied to the converter. The specification defines the interval between the time at which the converter is turned on and the fully loaded output voltage enters and remains within its specified accuracy band. See Typical Performance Curves.

Remote Sense

LSN2 Series offer an output sense function. The sense function enables point-of-use regulation for overcoming moderate IR drops in conductors and/or cabling. Since these are non-isolated devices whose inputs and outputs usually share the same ground plane, sense is provided only for the +Output.

The remote sense line is part of the feedback control loop regulating the DC/DC converter's output. The sense line carries very little current and consequently requires a minimal cross-sectional-area conductor. As such, it is not a low-impedance point and must be treated with care in layout and cabling. Sense lines should be run adjacent to signals (preferably ground), and in cable and/or discrete-wiring applications, twisted-pair or similar techniques should be used. To prevent high frequency voltage differences between V_{OUT} and Sense, we recommend installation of a 1000pF capacitor close to the converter.

The sense function is capable of compensating for voltage drops between the +Output and +Sense pins that do not exceed 10% of V_{OUT}.

$$[V_{OUT}(+) - \text{Common}] - [\text{Sense}(+) - \text{Common}] \leq 10\% V_{OUT}$$

Power derating (output current limiting) is based upon maximum output current and voltage at the converter's output pins. Use of trim and sense functions can cause the output voltage to increase, thereby increasing output power beyond the LSN2's specified rating. Therefore:

$$(V_{OUT} \text{ at pins}) \times (I_{OUT}) \leq \text{rated output power}$$

The internal 10.5Ω resistor between +Sense and +Output (see Figure 1) serves to protect the sense function by limiting the output current flowing through the sense line if the main output is disconnected. It also prevents output voltage runaway if the sense connection is disconnected.

Note: If the sense function is not used for remote regulation, +Sense must be tied to +Output at the DC/DC converter pins.

Remote On/Off Control

The input-side remote On/Off Control is an external input signal available in either positive (no suffix) or negative ("N" suffix) polarity. Normally this input is controlled by the user's external transistor or relay. With simple external circuits, it may also be selected by logic outputs. Please note however that the actual control threshold levels vary somewhat with the PWM supply and therefore are best suited to "open collector" or "open drain" type logic. The On/Off control takes effect only when appropriate input power has been applied and stabilized (approximately 7msec).

For positive polarity, the default operation leaves this pin open (unconnected) or HIGH. The output will then always be on (enabled) whenever appropriate input power is applied. Negative polarity models require the On/Off to be grounded to the –Input terminal or brought LOW to turn the converter on.

To turn the converter off, for positive polarity models, ground the On/Off control or bring it LOW. For negative polarity, raise the On/Off at least to +2.5V to turn it off.

Dynamic control of the On/Off must be capable of sinking or sourcing the

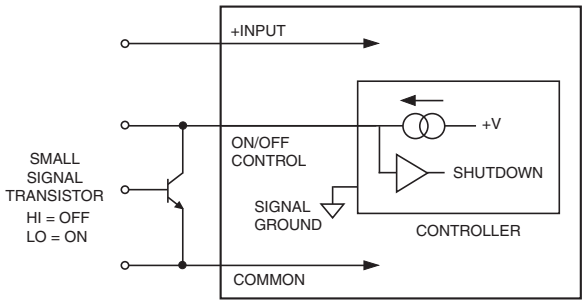


Figure 4. On/Off Control Using An External Open Collector Driver

control current (approximately 1mA max.) and not overdrive the input greater than the $+V_{IN}$ power input. Always wait for the input power to stabilize before activating the On/Off control. Be aware that a delay of several milliseconds occurs (see specifications) between activation of the control and the resulting change in the output.

Power-up sequencing

If a controlled start-up of one or more LSN2 Series DC/DC converters is required, or if several output voltages need to be powered-up in a given sequence, the On/Off control pin can be driven with an external open collector device as per Figure 4.

Leaving the input of the on/off circuit closed during power-up will have the output of the DC/DC converter disabled. When the input to the external open collector is pulled high, the DC/DC converter's output will be enabled.

Output Overvoltage Protection

LSN2 SIP Series DC/DC converters do not incorporate output overvoltage protection. In the extremely rare situation in which the device's feedback loop is broken, the output voltage may run to excessively high levels ($V_{OUT} = V_{IN}$). If it is absolutely imperative that you protect your load against any and all possible overvoltage situations, voltage limiting circuitry must be provided external to the power converter.

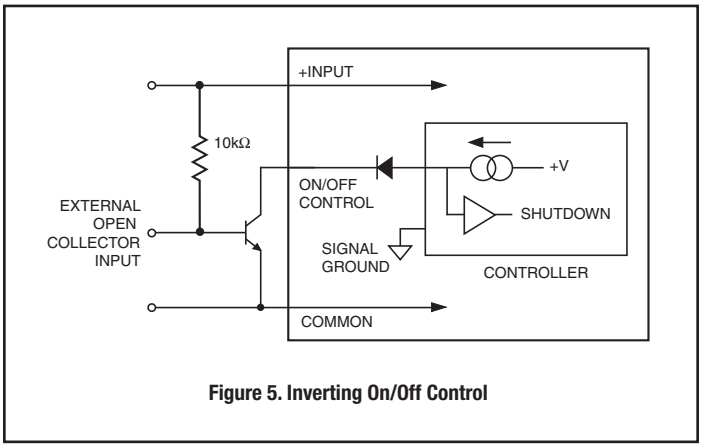


Figure 5. Inverting On/Off Control

Output Overcurrent Detection

Overloading the power converter's output for an extended time will invariably cause internal component temperatures to exceed their maximum ratings and eventually lead to component failure. High-current-carrying components such as inductors, FET's and diodes are at the highest risk. LSN2 SIP Series DC/DC converters incorporate an output overcurrent detection and shutdown function that serves to protect both the power converter and its load.

If the output current exceeds it maximum rating by typically 50% or if the output voltage drops to less than 98% of it original value, the LSN2's internal overcurrent-detection circuitry immediately turns off the converter, which then goes into a "hiccup" mode. While hiccupping, the converter will continuously attempt to restart itself, go into overcurrent, and then shut down. Once the output short is removed, the converter will automatically restart itself.

Output Reverse Conduction

Many DC/DC's using synchronous rectification suffer from Output Reverse Conduction. If those devices have a voltage applied across their output before a voltage is applied to their input (this typically occurs when another power supply starts before them in a power-sequenced application), they will either fail to start or self destruct. In both cases, the cause is the "freewheeling" or "catch" FET biasing itself on and effectively becoming a short circuit.

LSN2 SIP DC/DC converters do not suffer from Output Reverse Conduction. They employ proprietary gate drive circuitry that makes them immune to moderate applied output overvoltages.

Thermal Considerations and Thermal Protection

The typical output-current thermal-derating curves shown below enable designers to determine how much current they can reliably derive from each model of the LSN2 SIPs under known ambient-temperature and air-flow conditions. Similarly, the curves indicate how much air flow is required to reliably deliver a specific output current at known temperatures.

The highest temperatures in LSN2 SIPs occur at their output inductor, whose heat is generated primarily by I^2R losses. The derating curves were developed using thermocouples to monitor the inductor temperature and varying the load to keep that temperature below +110°C under the assorted conditions of air flow and air temperature. Once the temperature exceeds +115°C (approx.), the thermal protection will disable the converter. Automatic restart occurs after the temperature has dropped below about +110°C.

As you may deduce from the derating curves and observe in the efficiency curves on the following pages, LSN2 SIPs maintain virtually constant efficiency from half to full load, and consequently deliver very impressive temperature performance even if operating at full load.

Lastly, when LSN2 SIPs are installed in system boards, they are obviously subject to numerous factors and tolerances not taken into account here. If you are attempting to extract the most current out of these units under demanding temperature conditions, we advise you to monitor the output-inductor temperature to ensure it remains below +110°C at all times.

Pre-Biased Startup

Newer systems with multiple power voltages have an additional problem besides startup sequencing. Some sections have power already partially applied (possibly because of earlier power sequencing) or have leakage power present so that the DC/DC converter must power up into an existing voltage. This power may either be stored in an external bypass capacitor or supplied by an active source.

This "pre-biased" condition can also occur with some types of programmable logic or because of blocking diode leakage or small currents passed through forward biased ESD diodes. Conventional DC/DC's may fail to start up correctly if there is output voltage already present. And some external circuits are adversely affected when the low side MOSFET in a synchronous rectifier converter sinks current at start up.

The LSN2 series includes a pre-bias startup mode to prevent these initialization problems. Essentially, the converter acts as a simple buck converter until the output reaches its set point voltage at which time it converts to a synchronous rectifier design. This feature is variously called "monotonic" because the voltage does not decay (from low side MOSFET shorting) or produce a negative transient once the input power is applied and the startup sequence begins.

Don't Use Pre-Biasing and Sequencing Together

Normally, you would use startup sequencing on multiple DC/DC's to solve the Pre-Bias problem. By causing all power sources to ramp up together, no one source can dominate and force the others to fail to start. For most applications, do not use startup sequencing in a Pre-Bias application, especially with an external active power source.

If you have active source pre-biasing, leave the Sequence input open so that the output will step up quickly and safely. A symptom of this condition is repeated failed starts. You can further verify this by removing the existing load and testing it with a separate passive resistive load which does not exceed full current. If the resistive load starts successfully, you may be trying to drive an external pre-biased active source.

It may also be possible to use pre-bias and sequencing together if the Pre-Bias source is in fact only a small external bypass capacitor slowly charged by leakage currents. Test your application to be sure.

Output Adjustments

The LSN2 series includes a special output voltage trimming feature which is fully compatible with competitive units. The output voltage may be varied using a single trim resistor from the Trim input to Power Common (pin 4) or an external DC trim voltage applied between the Trim input and Power Common.

As with other trim adjustments, be sure to use a precision low-tempco resistor (±100 ppm/°C) mounted close to the converter with short leads. Also be aware that the output voltage accuracy is ±2% (typical) therefore you may need to vary this resistance slightly to achieve your desired output setting.

Resistor Trim Equation:

$$R_{TRIM}\ (\Omega) = \frac{10500}{V_O - 0.7525} - 1000$$

V_{OUT}	0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{TRIM} (kΩ)	Open	41.424	22.46	13.05	9.024	5.009	3.122	1.472

Voltage Trim

The LSN2 Series may also be trimmed using an external voltage applied between the Trim input and Output Common. Be aware that the internal "load" impedance looking into trim pin is less than 5kΩ. Therefore, you may have to compensate for this in the source resistance of your external voltage reference.

Use a low noise DC reference and short leads. Mount the leads close to the converter. Consider using a small bypass capacitor (0.1µF ceramic) between trim and output common to improve stability.

Voltage Trim Equation:

$$V_{TRIM}\ (\text{in Volts}) = 0.7 - (0.0667 \times (V_O - 0.7525))$$

The LSN2 fixed trim voltages to set the output voltage are:

V_{OUT}	0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
V_{TRIM} (V)	Open	0.6835	0.670	0.650	0.630	0.583	0.530	0.4166

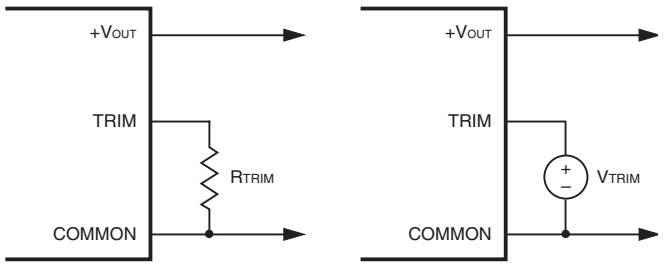


Figure 6. Trim Connections

LSN2 Power Sequencing

Whereas in the old days, one master switch simultaneously turned on the power for all parts of a system, many modern systems require multiple supply voltages for different on-board sections. Typically the CPU or microcontroller needs 1.8 Volts or lower. Memory (particularly DDR) may use 1.8 to 2.5 Volts. Interface "glue" and "chipset" logic might use +3.3Vdc power while Input/Output subsystems may need +5V. Finally, peripherals use 5V and/or 12V.

Timing is Everything

This mix of system voltages is being distributed by several local power solutions including Point-of-load (POL) DC/DC converters and sometimes a linear regulator, all sourced from a master AC power supply. While this mix of voltages is challenging enough, a further difficulty is the start-up and shutdown timing relationship between these power sources and relative voltage differences between them.

For many systems, the CPU and memory must be powered up, boot-strap loaded and stabilized before the I/O section is turned on. This avoids uncommanded data bytes being transferred, compromising an active external network or placing the I/O section in an undefined mode. Or it keeps bad commands out of disk and peripheral controllers until they are ready to go to work.

Another goal for staggered power-up is to avoid an oversize load applied to the master source all at once. A more serious reason to manage the timing and voltage differences is to avoid either a latchup condition in programmable logic (a latchup might ignore commands or would respond improperly to them) or a high current startup situation (which may damage on-board circuits). And on the power down phase, inappropriate timing or voltages can cause interface logic to send a wrong "epitaph" command.

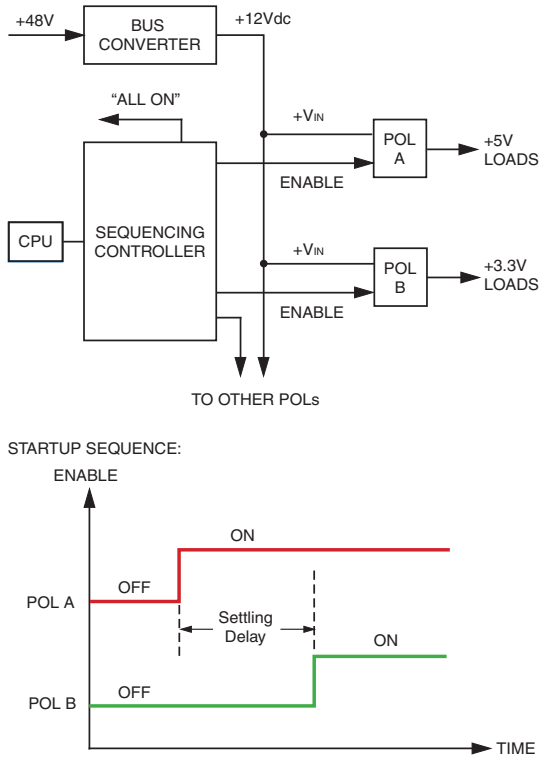


Figure 7. Power Up/Down Sequencing Controller

Two Approaches

There are two ways to manage these timing and voltage differences. Either the power up/down sequence can be controlled by discrete On/Off logic controls for each power supply (see Figure 7). Or the power up/down cycle is set by Sequencing or Tracking circuits. Some systems combine both methods.

The first system (discrete On/Off controls) applies signals from an already-powered logic sequencer or dedicated microcontroller which turns on each downstream power section in cascaded series. This of course assumes all POL's have On/Off controls. A distinct advantage of the sequencing controller is that it can produce an "All On" output signal to state that the full system is stable and ready to go to work. For additional safety, the sequencer can monitor the output voltages of all downstream POL's with an A/D converter system.

However the sequencer controller has some obvious difficulties besides extra cost, wiring and programming complexity. First, power is applied as a fast-rising, all-or-nothing step which may be unacceptable to certain circuits, especially large output bypass capacitors. These could force POL's into overcurrent shutdown. And some circuits (such as many linear regulators and some POL's) may not have convenient start-up controls. This requires designing and fabricating external power controls such as high-current MOSFET's.

If the power up/down timing needs to be closely controlled, each POL must be characterized for start-up and down times. These often vary—one POL may stabilize in 15 milliseconds whereas another takes 50 milliseconds. Another problem is that the sequencing controller itself must be "already running" and stabilized before starting up other circuits. If there is a glitch in the system, the power up/down sequencer could get out of step with possible disastrous results. Lastly, changing the timing may require reprogramming the logic sequencer or rewriting software.

Sequence/Track Input

A different power sequencing solution is employed on DATEL's LSN2 DC/DC converter. After external input power is applied and the converter stabilizes, a high impedance Sequence/Track input pin accepts an external analog voltage. The output power voltage will then track this Sequence/Track input at a one-to-one ratio up to the nominal set point voltage for that converter. This Sequencing input may be ramped, delayed, stepped or otherwise phased as needed for the output power, all fully controlled by the user's simple external circuits. As a direct input to the converter's feedback loop, response to the Sequence/Track input is very fast (milliseconds).

By properly controlling this Sequence pin, most operations of the discrete On/Off logic sequencer may be duplicated. The Sequence pin system does not use the converter's Enable On/Off control (unless it is a master emergency shut down system).

Power Phasing Architectures

Observe the simplified timing diagrams below. There are many possible power phasing architectures and these are just some examples to help you analyze your system. Each application will be different. Multiple output voltages may require more complex timing than that shown here.

These diagrams illustrate the time and slew rate relationship between two typical power output voltages. Generally the Master will be a primary power voltage in the system which must be present first or coincident with any Slave power voltages. The Master output voltage is connected to the Slave's Sequence input, either by a voltage divider, divider-plus-capacitor or some other method. Several standard sequencing architectures are prevalent. They are concerned with three factors:

- The time relationship between the Master and Slave voltages
- The voltage difference relationship between the Master and Slave
- The voltage slew rate (ramp slope) of each converter's output.

For most systems, the time relationship is the dominant factor. The voltage difference relationship is important for systems very concerned about possible latchup of programmable devices or overdriving ESD diodes. Lower slew rates avoid overcurrent shutdown during bypass cap charge-up.

In Figure 18, two POL's ramp up at the same rate until they reach their different respective final set point voltages. During the ramp, their voltages are nearly identical. This avoids problems with large currents flowing between

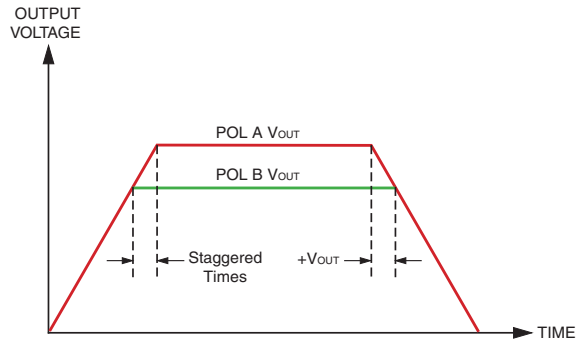


Figure 8. Coincident or Simultaneous Phasing (Identical Slew Rates)

logic systems which are not initialized yet. Since both end voltages are different, each converter reaches it's setpoint voltage at a different time.

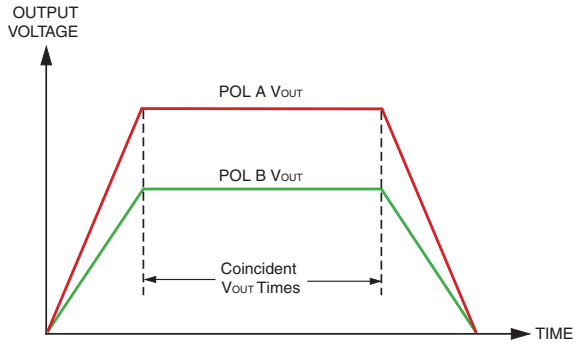


Figure 9. Proportional or Ratiometric Phasing (Identical V_{OUT} Time)

Figure 9 shows two POL's with different slew rates in order to reach differing final voltages at about the same time.

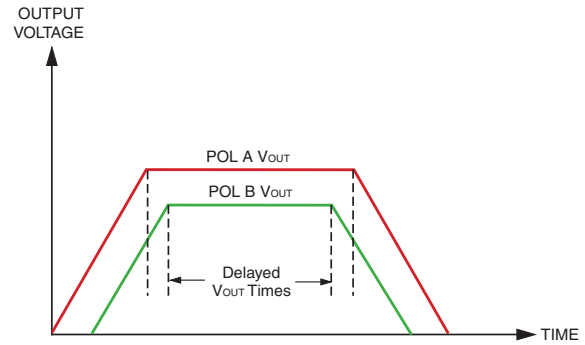


Figure 10. Staggered or Sequential Phasing—Inclusive (Fixed Delays)

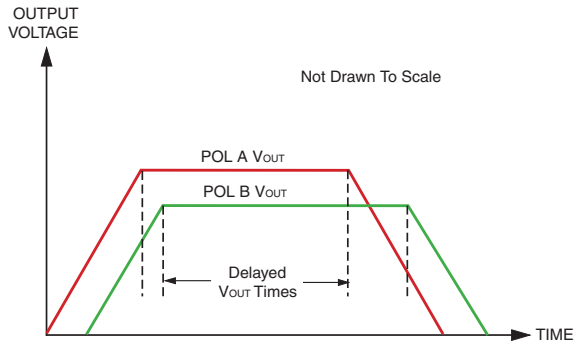


Figure 11. Staggered or Sequential Phasing—Exclusive (Fixed Cascaded Delays)

Figures 10 and 11 show both delayed start up and delayed final voltages for two converters. Figure 10 is called "Inclusive" because the later starting POL finishes inside the earlier POL. The timing in Figure 10 is more easily built using a combined digital sequence controller and the Sequence/Track pin.

Figure 11 is the same strategy as Figure 10 but with an "exclusive" timing relationship staggered approximately the same at power-up and power-down.

Operation

To use the Sequence pin after power start-up stabilizes, apply a rising external voltage to the Sequence input. As the voltage rises, the output voltage will track the Sequence input (gain = 1). The output voltage will stop rising when it reaches the normal set point for the converter. The Sequence input may optionally continue to rise without any effect on the output. Keep the Sequence input voltage below the converter's input supply voltage.

Use a similar strategy on power down. The output voltage will stay constant until the Sequence input falls below the set point.

Any strategy may be used to deliver the power up/down ramps. The circuits below show simple RC networks but you may also use operational amplifiers, D/A converters, etc.

Circuits

The circuits shown in Figures 12 through 14 introduce several concepts when using these Sequencing controls on Point-of-Load (POL) converters. These circuits are only for reference and are not intended as final designs ready for your application. Also, numerous connections are omitted for clarity.

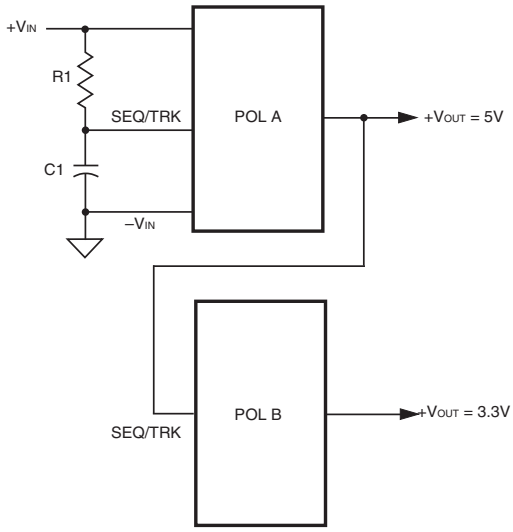


Figure 12. Wiring for Simultaneous Phasing

Figure 12 shows a basic Master (POL A) and Slave (POL B) connected so the POL B ramps up identically to POL A as shown in timing diagram, Figure 8. RC network R1 and C1 charge up at a rate set by the R1-C1 time constant, giving a roughly linear ramp. As POL A reaches 3.3VOUT (the setpoint of POL B), POL B will stop rising. POL A then continues rising until it reaches 5V. R1 should be significantly smaller than the internal bias current resistor from the Sequence pin. Start with a 20kΩ value. We assume that the critical phase is only on power up therefore there is no provision for ramped power down.

Figure 13 shows a single POL and the same RC network. However, we have added a FET at Q1 as an up/down control. When VIN power is applied to the POL, Q1 is biased on, shorting out the Sequence pin. When Q1's gate is biased off, R1 charges C1 and the POL's output ramps up at the R1-C1 slew rate. Note: Q1's gate would typically be controlled from some external digital logic.

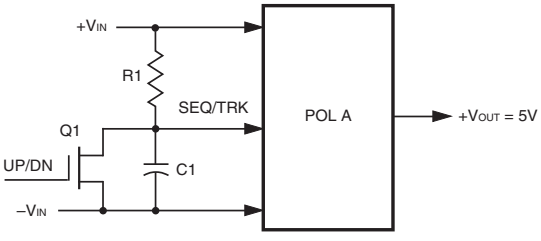


Figure 13. Self-Ramping Power Up

If you wish to have a ramped power down (rather than a step down), add a small resistor in series with Q1's drain.

Figure 14 shows both a RC ramp on Master POL A and a proportional tracking divider (R2 and R3) on POL B. We have also added an optional very small noise filter cap at C2. Figure 14's circuit corresponds roughly to Figure 9's timing for power up.

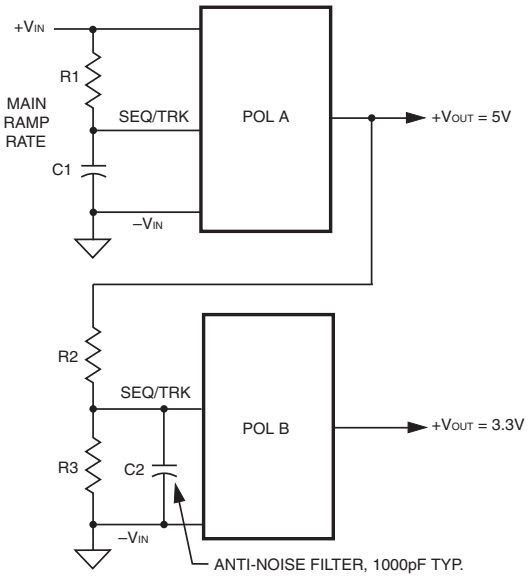


Figure 14. Proportional Phasing

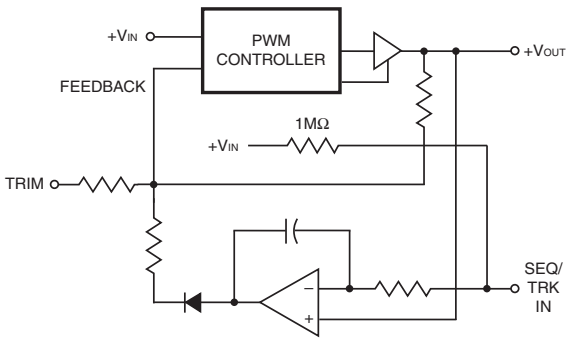


Figure 15. Sequence/Track Simplified Equivalent Schematic

Guidelines for Sequence/Track Applications

[1] Leave the converter's On/Off Enable control (if installed) in the On setting. Normally, you should just leave the On/Off pin open.

[2] Allow the converter to stabilize (typically less than 20 mS after +VIN power on) before raising the Sequence input. Also, if you wish to have a ramped power down, leave +VIN powered all during the down ramp. Do not simply shut off power.

[3] If you do not use the Sequence/Track pin, leave it open or tied to +VIN.

[4] Observe the Output slew rate relative to the Sequence input. A rough guide is 2 Volts per millisecond maximum slew rate. If you exceed this slew rate on the Sequence pin, the converter will simply ramp up at it's maximum output slew rate (and will not necessarily track the faster Sequence input). The reason to carefully consider the slew rate limitation is in case you want two different POL's to precisely track each other.

[5] Be aware of the input characteristics of the Sequence pin. The high input impedance affects the time constant of any small external ramp capacitor. And the bias current will slowly charge up any external caps over time if they are not grounded. The internal pull-up resistor to $+V_{IN}$ is typically 1MΩ.

Notice in the simplified Sequence/Track equivalent circuit (Figure 15) that a blocking diode effectively disconnects this circuit when the Sequence/Track pin is pulled up to $+V_{IN}$ or left open.

[6] Allow the converter to eventually achieve its full-rated setpoint output voltage. Do not remain in ramp up/down mode indefinitely. The converter is characterized and meets all its specifications only at the setpoint voltage (plus or minus any trim voltage). During the ramp-up phase, the converter is not considered fully in regulation. This may affect performance with excessive high current loads at turn-on.

[7] The Sequence is a sensitive input into the feedback control loop of the converter. Avoid noise and long leads on this input. Keep all wiring very short. Use shielding if necessary. Consider adding a small parallel ceramic capacitor across the Sequence/Track input (see Figure 14) to block any external high frequency noise.

[8] If one converter is slaving to another master converter, there will be a very short phase lag between the two converters. This can usually be ignored.

[9] You may connect two or more Sequence inputs in parallel from two converters. Be aware of the increasing pull-up bias current and reduced input impedance.

[10] Any external capacitance added to the converter's output may affect ramp up/down times and ramp tracking accuracy.

Power Good Output

The Power Good Output consists of an unterminated BSS138 small signal field effect transistor and a dual window comparator input circuit driving the gate of the FET. Power Good is TRUE (open drain, high impedance state) if the converter's power output voltage is within about ±10% of the setpoint. Thus, the PG TRUE condition indicates that the converter is approximately within regulation. Since an overcurrent condition occurs at about 2% output voltage reduction, the Power Good does not directly measure an output overcurrent condition at rated maximum output current. However, gross overcurrent or an output short circuit will set Power Good to FALSE (+0.2V saturation, low impedance condition).

Using a simple connection to external logic (and returned to the converter's Common connection), the Power Good output is unterminated so that the user may adapt the output to a variety of logic families. The PG pin may therefore be used with logic voltages which are not necessarily the same as the input or output power voltages. Install an external pullup resistor to the logic supply voltage which is compatible with your logic system. When the Power Good is out of limit, the FET is at saturation, approximately +0.2V output. Keep this LOW (FALSE) pulldown current to less than 10mA.

Please note that Power Good is briefly false during Sequence ramp-up. Ignore Power Good while in transition.

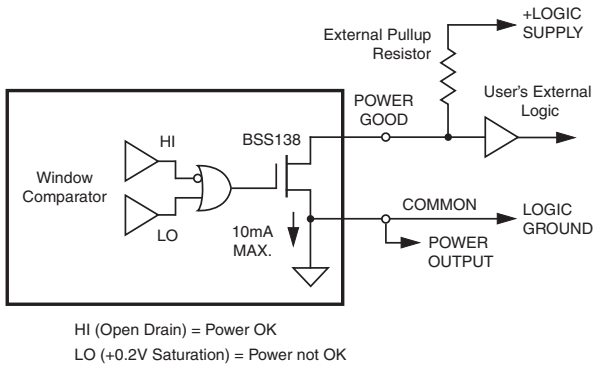
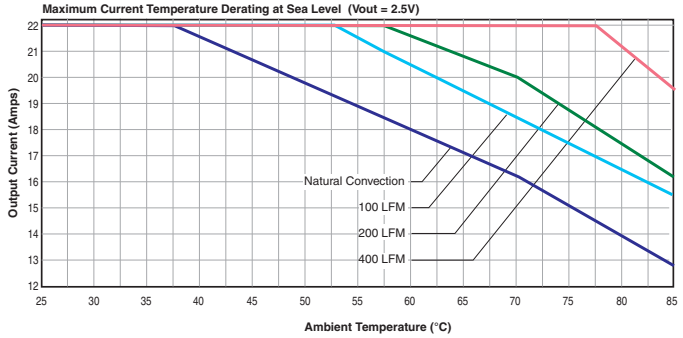


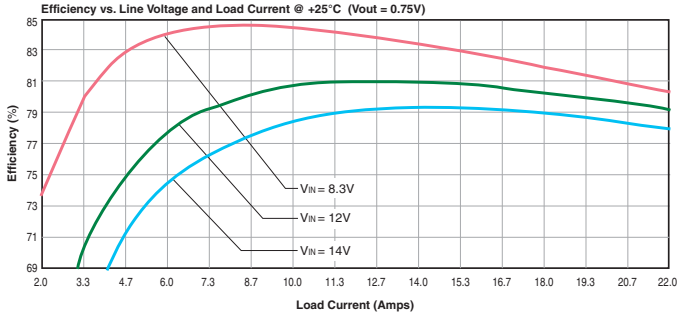
Figure 16. Equivalent Power Good Circuit

TYPICAL PERFORMANCE CURVES

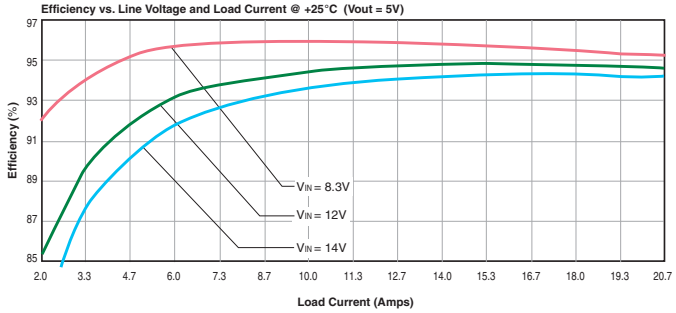
LSN2-T/22-D12
Maximum Current Temperature Derating at Sea Level (Vout = 2.5V)



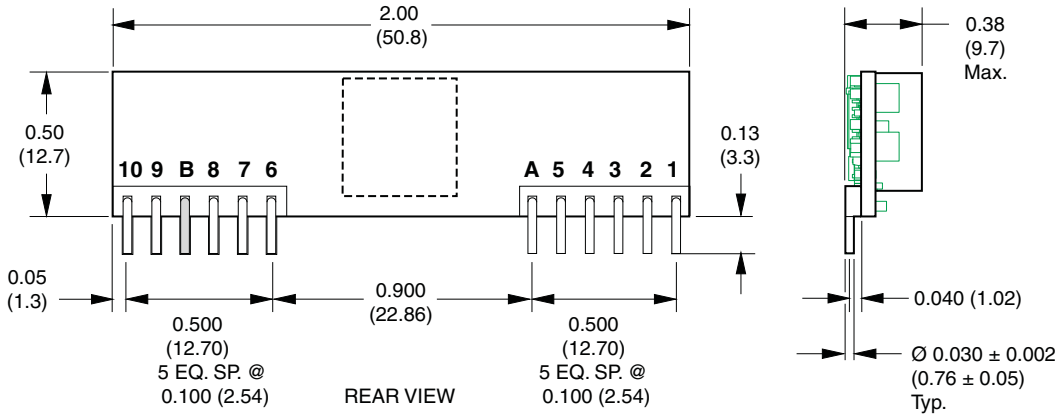
LSN2-T/22-D12
Efficiency vs. Line Voltage and Load Current @ +25°C (Vout = 0.75V)



LSN2-T/22-D12
Efficiency vs. Line Voltage and Load Current @ +25°C (Vout = 5V)



Case B14



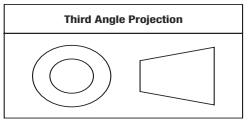
I/O CONNECTIONS			
Pin	Function P68	Pin	Function P68
1	+Output	6	Common
2	+Output	7	+Input
3	+Sense In	8	+Input
4	+Output	B	VTRACK/Sequence **
5	Common	9	Trim
A	Power Good Out *	10	On/Off Control

* Power Good output is optional.
If not installed, the pin is omitted.

** VTRACK/Sequence pin "B"
is not installed for parts ordered
with the "B" suffix.

Note: Because of the high currents, wire the appropriate input, output and common pins in parallel groups.

Dimensions are in inches (mm) shown for ref. only.



Tolerances (unless otherwise specified):
.XX ± 0.02 (0.5)
.XXX ± 0.010 (0.25)
Angles ± 2˚

Components are shown for reference only.