Product Description

The **ARC2C0608** is an ultra-high efficiency DC/DC converter solution with integrated programmable current sinks that drives up to six strings of LEDs. The ARC2C0608 integrates all MOSFETs and their control and driver circuitry. With a proprietary architecture, the ARC2C0608 provides the highest efficiency (>94%) possible in a compact WLCSP-35 package. The 0.4 mm pitch and high switching frequency enables small solution size aligned to the needs of the newest mobile products.

Features

- Synchronous DC/DC converter with integrated FETs
- 2-cell Li-Ion battery input voltage: 4.5V to 13.2V
- Patented architecture for ultra-high LED efficiency, above 90% over entire operating range
- Integrated output disconnect switch
- Up to 30V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- 12 bits hybrid (mixed) linear dimming mode and 10 bits logarithmic mapping
- Up to 12 bits resolution with DC or PWM dimming
- Supports direct PWM dimming for maximum flexibility and resolution
- LED brightness ramp up/down control with programmable ramp rate and linear/logarithmic ramp profiles
- Phase-shifted PWM dimming among active strings to minimize audible noise
- 1MHz I²C 6.0-compatible serial interface to program the brightness, or an external resistor on ISET to set the maximum brightness
- External PWM input for fine dimming resolution
- Six independently enabled current sinks, up to 30 mA per current sink–up to 40 mA for lower string counts or lower Vout
- 0.5% typical current matching accuracy at 30mA.
- Wide range of input and output voltages with 2x charge pump ratio
- Selectable boost switching frequency from 320 KHz to 3.4 MHz
- Extensive fault protection including boost over-current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Typical Applications

2-cell platforms including:

- Ultrabooks / ultraportable notebooks
- 2-in-1 / convertible / detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

Figure 1 shows ARC2C0608 typical boost efficiency.

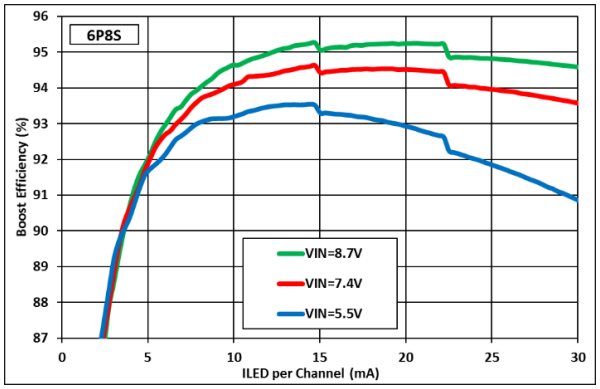

Figure 1. Typical Boost Efficiency--6P8S

Simplified Applications

Figure 2 shows a typical application circuit.

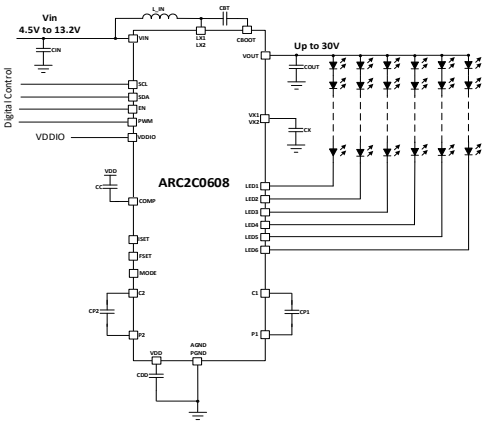

Figure 2. Typical Application Circuit

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Absolute Maximum Ratings[1,2]

The maximum voltages and temperatures to be used with this device are given in Table 1.

PARAMETER	MIN	MAX	UNITS
VIN to AGND	-0.3	17.6	V
VDD, VDDIO, PWM, COMP, EN, ISET, MODE, FSET, SCL, SDA to AGND	-0.3	6	V
VDDP to AGND	-0.3	8	V
VOUT, C1, C2 to PGND	-0.3	32	V
LEDx to AGND	-0.3	26.4	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1, P2 to PGND	-0.3	17.6	V
VX to LX	-0.3	17.6	V
CBOOT to VDD	-0.3	17.6	V
CBOOT to LX	-0.3	6	V
C1, C2 to VX	-0.3	17.6	V
VOUT to C1, C2	-0.3	17.6	V
Storage Temperature	-65°C	150 ° C	° C
PARAMETER	**VALUE**		
Junction Temperature	150°C		
Bump or Lead Temperature (soldering, reflow)	260 ° C		
ESD Tolerance, HBM[3]	2KV		
ESD Tolerance, CDM[4]	750V		

Notes:
The application of any stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, and exposure at any of these ratings for extended periods may reduce the reliability of the device.

1. *The above "Absolute Maximum Ratings" are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.*
2. *Human body model, per the JEDEC standard JS-001-2012.*
3. *Field-induced charge device model, per the JEDEC standard JESD22-C101.*

Table 1. Absolute Maximum Ratings

Recommended Operating Conditions

Details of the minimum and maximum voltages and temperature ranges for optimal use of this product are given in Table 2.

PARAMETER	MIN	MAX	UNITS
VIN Input Voltage Range	4.5	13.2	V
VOUT Output Voltage Range relative to AGND or PGND	18	30	V
VX Boost Output Voltage Range	1.2xVIN	16	V
VDDIO Voltage Range	1.08	3.63	V
Junction Temperature Range, T_J	-30	125	°C

Table 2. Recommended Operating Conditions

Package Thermal Characteristics[1,2]

Package thermal characteristics are given in **Table 3**.

PARAMETER	WLCSP-35	UNITS
Junction-to-Ambient Thermal Resistance (Θ_{JA}), soldered thermal pad, connected to ground plane	44.5	°C/W
Junction-to-Board Thermal Characterization (Ψ_{JB})	10.8	°C/W
Junction-to-Top Case Characterization (Ψ_{JC})	6.5	°C/W

Notes:
1. *Package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.*
2. *Junction-to-Ambient Thermal Resistance (Θ_{JA}) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.*

Table 3. Thermal Characteristics

Electrical Characteristics[1]

The electrical characteristics of the package are given in Table 4.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{VIN}	Full parametric performance	4.5		13.2	V
Voltage Regulator Output Voltage	V_{DD}			4.0	4.4	V
Undervoltage Lockout (UVLO) Threshold High	V_{UVLO_H}	VVIN rising		4.275	4.45	V
Undervoltage Lockout (UVLO) Hysteresis	V_{UVLO_HYST}			70		mV
Shutdown Supply Current	I_{VIN_SD}	IVIN with VEN=0V			1	µA
Standby Supply Current	$I_{VIN-STDBY}$	VEN = 1.8V I2C_STDBY=1			175	
Supply Voltage for Digital I/O	V_{DDIO}		1.08		3.63	V
Supply Current for Digital I/O	I_{VDDIO}	EN=0V or 1.8V, SDA=SCL=0V or VDDIO, measure at VDDIO=1.8V		8		µA
Thermal Shutdown Threshold[3]	T_{TSD}			150		°C
Thermal Shutdown Hysteresis[3]	T_{TSD_HYST}			20		°C
Soft Start Time-Out Duration				10		ms

Table 4. Electrical Characteristics

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP CONVERTER– BOOST							
Boost Switching Frequency Range	f_{SW_BOOST}	I²C interface only FSW_BOOST[4:0]	13h				MHz
			09h				
			05h				
			03h				
		Non-I²C interface only	FSET = VDD		2.56		
			FSET = open		1.024		
			FSET = AGND		0.512		
Boost Switching Frequency Accuracy				-10		+10	%
Boost Minimum Off-Time	$T_{OFF\_BOOST\_MIN}$				50		ns
Boost Minimum On-Time	$T_{ON\_BOOST\_MIN}$				50		ns
Boost Low-Side Switch Current Limit, Cycle-by-Cycle	I_{BOOST_LIMIT}	I_{LX} rising			2.9		A
VOUT-COMP Transconductance[2]	g_m	I_{LX} rising			1.56		µA/V
Gm Amplifier unity Gain Bandwidth	F_0	20KΩ on COMP pin			1.9		MHz
Gm Amplifier Max Source Current					8		µA
Gm Amplifier Max Sink Current					8		µA

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-UP CONVERTER – CHARGE PUMP							
Output Voltage Range[2,8]	V_{OUT}	V_{VIN} =4.5V~8.7V		18		30	V
Maximum Continuous Load Current	I_{OUT}			180			mA
Output Over-Current Threshold	I_{OUT_OC}	I_{OUT} rising		250			mA
Output Over-voltage Threshold	V_{OUT_OVP}	OVP_TH[1:0]	00		31.4		V
			01		24		
			10		20		
Output Over-voltage Hysteresis	$V_{OUT\_OVP\_HYST}$				0.5		V
Accuracy of Output Over-Voltage Protection Threshold				-4		4	%
LED CURRENT SINKS (LED1 to LED6)							
ISET Voltage	V_{ISET}				0.4		V
ISET Pin Voltage Accuracy[7]				-3.25		4.0	%
ISET Recommended Resistor Range	R_{ISET}	Excluding resistor tolerance		24.9		250	kΩ
Current Multiplier	K_{ISET}	I^2C Register Setting MAX_I[1:0]	00		937.5		A/A
			01		1250		
			10		1562.5		
			11		1875		
LED Current Full-Scale Output Range	I_{LED_MAX}	I^2C Register Setting MAX_I[1:0]	00		15		mA
			01		20		
			10		25		
			11		30		
Minimum Sink Current LED1-6	I_{LEDx_MIN}	I_{LED} programmed to 30mA			7.3		µA

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED CURRENT SINKS (LED1 to LED6)						
Leakage Current	$I_{LED\_LEAKAGE}$	LEDEN1,..,6=0, V_{OUT} = 26.4V			1	µA
LED Current Matching[4]	$I_{LED\_MATCHING}$	I_{LEDX} programmed to 30mA, T_A = 25°C, DC IDAC O/P		0.5		%
LED Current Accuracy[4]	$I_{LED\_ACCURACY}$	I_{LEDX} programmed to 30mA, T_A = 25°C, DC IDAC O/P	-3		+3	%
LED Dropout Voltag[5]	$V_{LED\_REGULATION}$	I_{LEDX} programmed to 30mA, T_A = 25°C, DC IDAC O/P		180		mV
LED Shorted String Detection Threshold		V_{LEDX} rising		6.3		V
Current Ripple[2]		I_{LED} programmed to 30mA, TA = 25°C, DC IDAC output			1	%

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL PWMM DIMMING							
Transition Point Between Internal PWM and Analog Dimming[6]		DIM_MODE=0			0%		
		DIM_MODE=1 PVWM-IX[1:0]	00		12.5%		
			01		25% (Default)		
			10		50%		
			11		100%		
		Non-I²C mode			25%		
LED PWM Output Frequency	fILEDX	Non-I²C mode with MODE pin floating			2.5		KHz
		DIMCODE[1:0]=00, 10, or 01 in I²C mode		2.5		40	kHz
LED Current Sink Minimum Output Pulse Width					200		ns
DIRECT PWMM DIMMING							
Direct PWM Input to Output Timing Skew					**-25**		**ns**

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INTERFACE (EN, PWM, FSET)						
EN Logic Input High Voltage	V_{IH_EN}		1.1			V
EN Logic Input Low Voltage	V_{IL_EN}				0.4	V
PWM Logic Input High Voltage	V_{IH_PWM}		0.9			V
PWM Logic Input Low Voltage	V_{IL_PWM}				0.5	V
Logic Input Current	I_{PWM} I_{EN}		-1.0		1.0	µA
FSET Input Resistance	$I_{\_FSET\_R}$	Non-I²C mode only		100		kΩ
FSET Input Low Voltage	V_{IL_FSET}	Non-I²C mode only			0.4	V
FSET Input High Voltage	V_{IH_FSET}	Non-I²C mode only	V_{DD}-0.4			V
MODE Pin Input Resistance	$I_{\_MODE\_R}$	Non-I²C mode only		100		kΩ
MODE Pin Input Low Voltage	V_{IL_MODE}	Non-I²C mode only			0.4	V
MODE Pin Input High Voltage	V_{IH_MODE}	Non-I²C mode only	V_{DD}-0.4			V
PWM Pin Input Frequency for Internal PWM mode	F_{IPWM}		0.2		40	KHz
PWM Pin Input Frequency for Direct PWM mode	F_{DPWM}		0.2		20	KHz
PWM Pin Minimum Input High Pulse			100			ns
PWM Pin Minimum Input Low Pulse			100			ns

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C SERIAL INTERFACE (SCL, SDA, VDDIO)						
VDDIO Supply Voltage Range	V_{DDIO}		1.08		3.63	V
SDA, SCL Input High Voltage	V_{IH}		0.7 x V_{VDDIO}			V
SDA, SCL Input Low Voltage	V_{IL}				0.3 x V_{VDDIO}	V
SDA, SCL Input Hysteresis	V_{HYS}		0.05 x V_{VDDIO}			V
SDA, SCL Input Current	I_{SCL}, I_{SDA}		-1		1	µA
SDA Output Low Level	V_{OL}	I_{SDA} = 20mA			0.4	V
I^2C Interface Initial Wait Time		Initial Wait time from EN logic high to 1st I^2C command	1000			µs
SDA, SCL Pin Capacitance[2]	$C_{I/O}$				10	pF

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I2C INTERFACE TIMING CHARACTERISTICS FOR STANDARD, FAST MODE AND FAST MODE PLUS					
Serial Clock Frequency	F_{SCL}	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
Clock Low Period	t_{LOW}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Clock High Period	t_{HIGH}	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
BUS Free Time between a STOP and a START condition	t_{BUF}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast mode plus	0.5		µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Standard mode	4.7		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Hold Time for a Repeated START condition	$t_{HD:STA}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Setup Time of STOP condition	$t_{SU:STO}$	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
Data Setup Time	$t_{SU:DAT}$	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD, FAST MODE AND FAST MODE PLUS					
Data Hold Time	t_{HD_DAT}	Standard mode	0		µs
		Fast mode	0		ns
		Fast mode plus	0		ns
Rise Time of SCL Signal	t_{RCL}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode		300	ns
		Fast mode		300	ns
		Fast mode plus		120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode		1000	ns
		Fast mode	20	300	ns
		Fast mode plus		120	ns
Fall Time of SDA Signa[2]	tFDA	Standard mode		300	ns
		Fast mode	20 x VDDIO/ 5.5V	300	ns
		Fast mode plus	20 x VDDIO/ 5.5V	120	ns
Data Valid Time	t_{VD}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns
Data Valid Acknowledge Time	t_{VDA}	Standard mode		3.45	µs
		Fast mode		900	ns
		Fast mode plus		450	ns

Table 4. Electrical Characteristics contd.

VIN = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C with 6p8s.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD, FAST MODE AND FAST MODE PLUS					
Capacitive Load for SDA and SCL	C_{BUS}	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF

Notes:

1. *Min/Max specifications are 100% production tested at TA=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.*
2. *Guaranteed by design.*
3. *Thermal shutdown is not production tested.*
4. *The LED current accuracy is defined/tested as: 100*(ILED_AVG-ILED_Target)/ILED_AVG. The sink current matching is defined/tested as (ILED_MAX-ILED_MIN)/ILED_AVG.*
5. *Dropout voltage is the LEDx voltage at which the current has decreased by 1% relative to its value when the LEDx voltage is 1V.*
6. *Default is 25%. Can be trimmed to 0, 12.5%, 50% or 100% if needed for non-I²C mode.*
7. *If ISET pin is used, the LED full scale current is trimmed to compensate for voltage variation.*
8. *At very light loads in DCM mode, VOUT may be higher than expected. However, LED current regulation is not adversely affected.*

Table 4. Electrical Characteristics contd.

I²C Timing Diagram

The ARC2C0608 serial interface timing for Standard Mode, Fast Mode, and Fast-Mode Plus is shown in Figure 3.

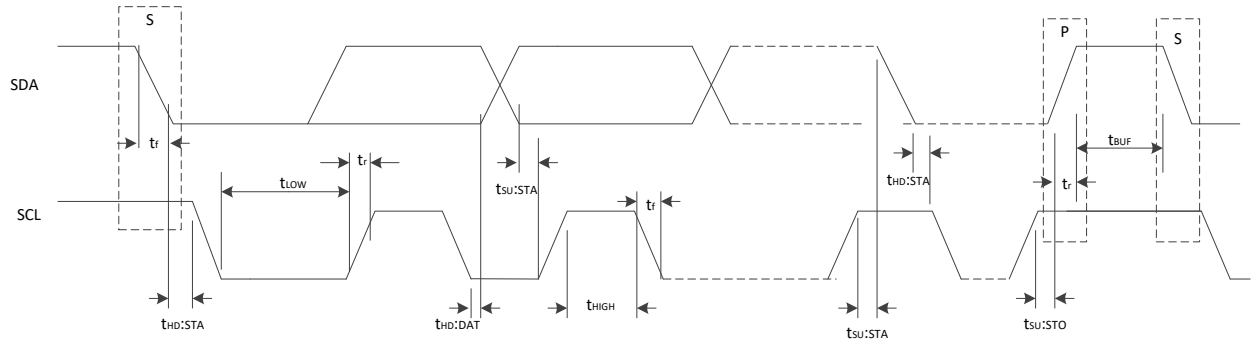

Figure 3. Serial Interface Timing Diagram for Standard-, Fast-, Fast-Mode Plus

Pin Function and Configurations

Pin function and configurations of the ARC2C0608 are shown in Figure 4.

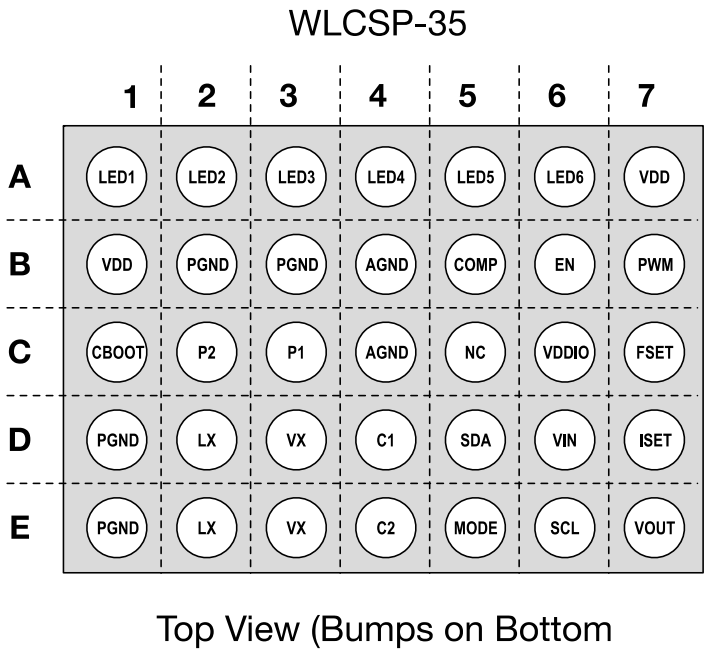

Figure 4. Package Drawing

Pin Descriptions

The ARC2C0608 pin descriptions are given in Table 5.

PIN NAME	PIN #	DESCRIPTION
VIN	D6	Input voltage, battery power supply pin.
LX	D2, E2	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage.
MODE	E5	Float this pin or tie it to ground or VDD (LDO output only) to select one of three LED current output options in non-I2C mode. See application section for more detail.
C1	D4	Charge pump fly capacitor to be externally connected between C1 and P1.
C2	E4	Charge pump fly capacitor to be externally connected between C2 and P2.
P1	C3	Phase node for charge pump fly capacitor C1.
P2	C2	Phase node for charge pump fly capacitor C2.
CBOOT	C1	Bootstrap capacitor for Boost stage high side FET.
VX	D3, E3	Charge pump input node, internally driven by output of boost converter. Connect externally to CX capacitor per application guidelines.
VOUT	E7	Power converter output voltage. Connect to the high side of all LED strings.
PWM	B7	PWM dimming input for brightness control. Connect to VDD if not used.
COMP	B5	Compensation pin.
LEDx	A1-A6	Individual LED current sink. Connect to low side of individual LED strings.
AGND	B4, C4,	Analog Ground, must tie externally to ground plane.
PGND	B2, B3, D1, E1	Power Ground, must tie externally to ground plane. High current path.
SCL	E6	Serial Clock for I2C bus. Also used in non-I2C mode for current setting using IMAXTUNE.
SDA	D5	Serial Data for I2C bus. Also used in non-I2C mode for current setting using IMAXTUNE.
ISET	D7	LED current setting pin. Connect a resistor from this pin to AGND to set the full scale LED current in non-I2C mode or when the ISET_EXT bit is set high in I2C mode.
VDDIO	C6	Digital IO supply voltage for I2C interface.
VDD	B1	Internal LDO output pin. Connect capacitor CVDD between this pin and AGND. Use this pin to power FSET, and MODE. Can also be used as pull up for PWM, (and SDA, SCL in non-I2C mode).
VDD	A7	This pin must be shorted to the VDD pin.
EN	B6	Enable input.

PIN NAME	PIN #	DESCRIPTION
FSET	C7	Float this pin or tie it to ground or VDD (LDO output only) to set the boost switching frequency in non-I2C mode. See application section for more detail.
NC	C5	Not connected internally. Can be connected to ground plane.

Table 5. Pin Description

Functional Block Diagram

The ARC2C0608 block diagram is given in Figure 5.

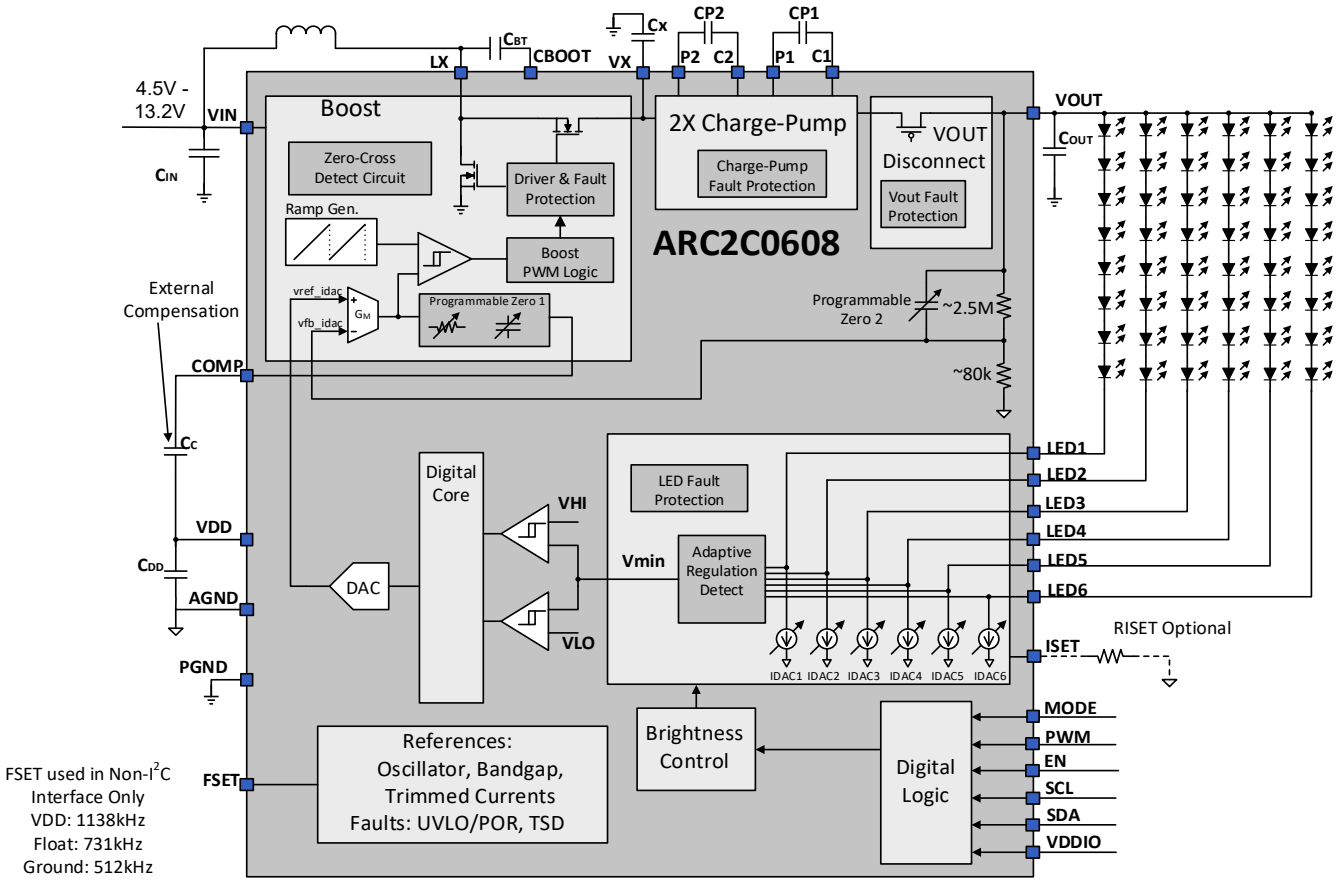

Figure 5. Block Diagram

Application Circuit

The schematic of the ARC2C0608 application circuit is shown in Figure 6.

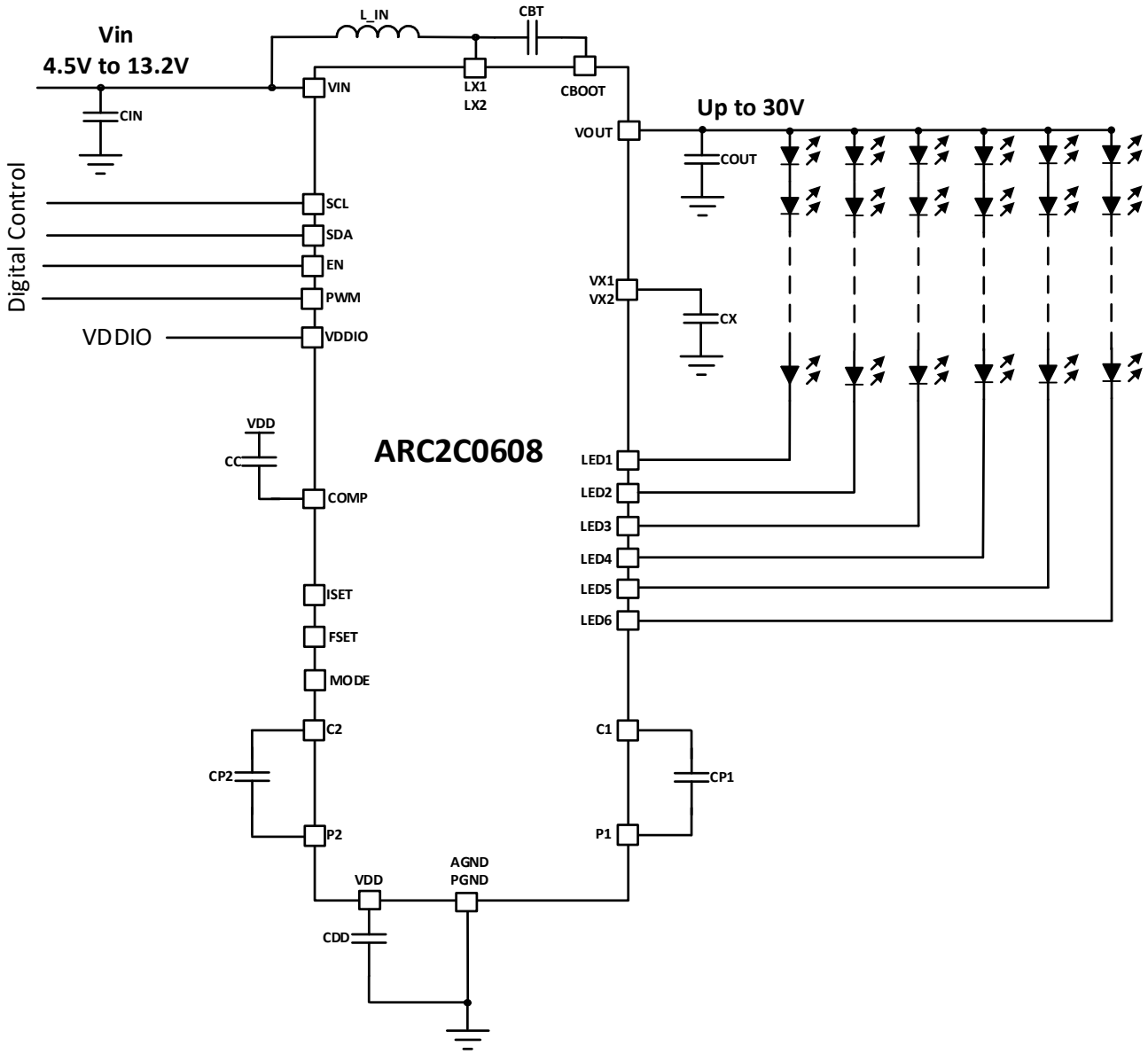

Figure 6. Application Schematic for I²C Interface

Typical Characteristics

Unless otherwise specified, VIN=7.4V, L=15 µH TDK VLF504015-150M, Cout=4.7 µF, LED V=2.85V (typ), 512 kHz boost frequency.

LED Efficiency

The figures that follow are a graphical representation of LED efficiency.

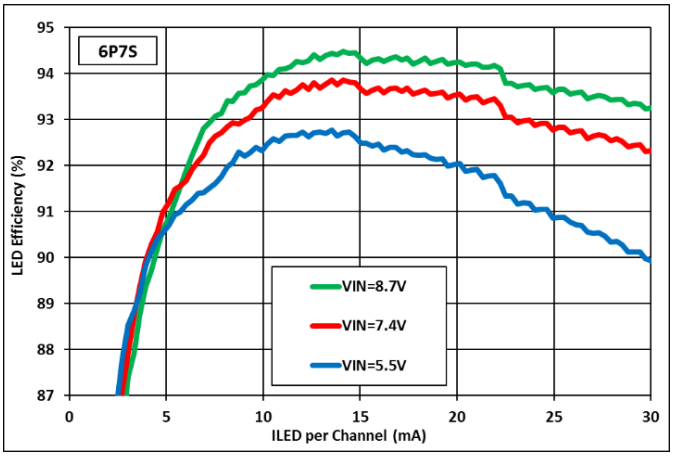

Figure 7. 6p7s LED Efficiency

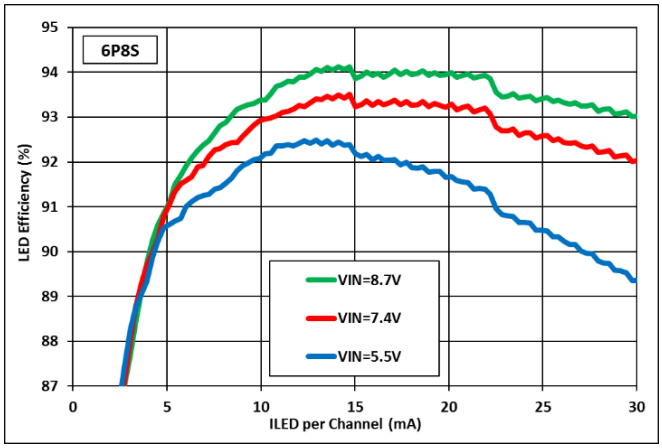

Figure 8. 6p8s LED Efficiency

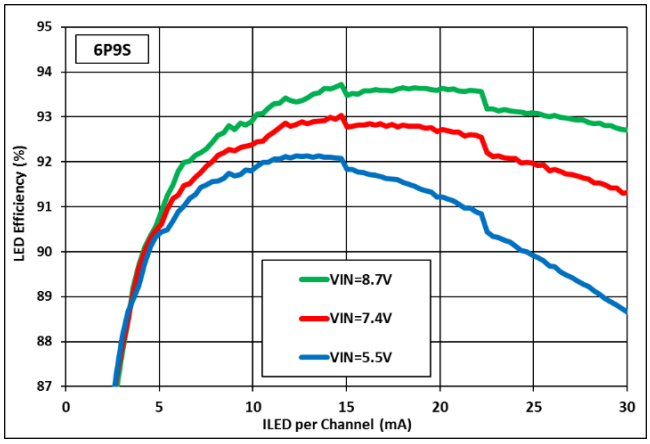

Figure 9. 6p9s LED Efficiency

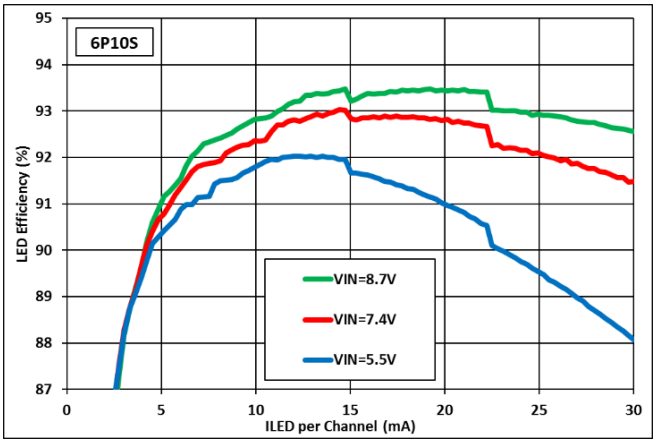

Figure 10. 6p10s LED Efficiency

LED Current Sinks

Unless otherwise specified, VIN=7.4V, L=15 µH TDK VLF504015-150M, Cout=4.7 µF, LED V=2.85V (typ), 512 kHz boost frequency.

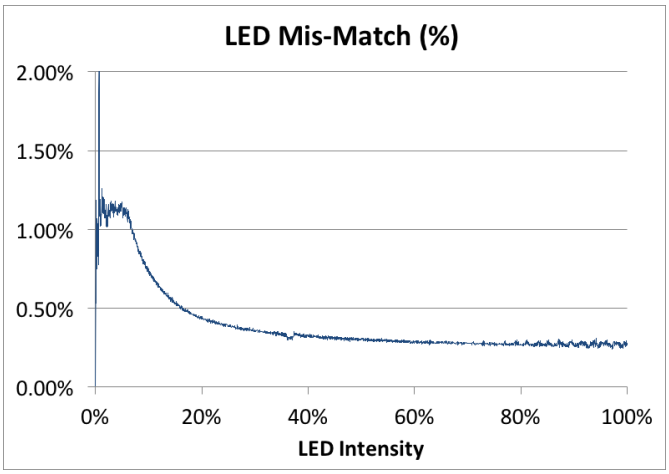

Figure 11. LED Mismatch—Linear Mode

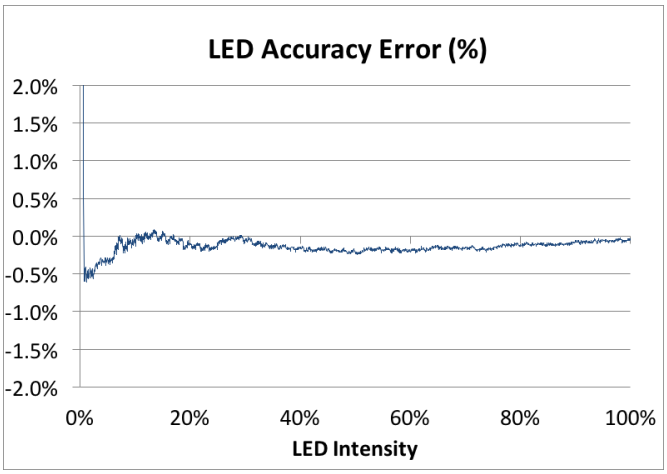

Figure 12. LED Accuracy—Linear Mode

Typical Characteristics (cont'd.)

Unless otherwise specified, VIN=7.4V, L=15 µH TDK VLF504015-150M, Cout=4.7 µF, LED V=2.85V (typ), 512 kHz boost frequency.

Startup Waveforms (non-I²C mode)

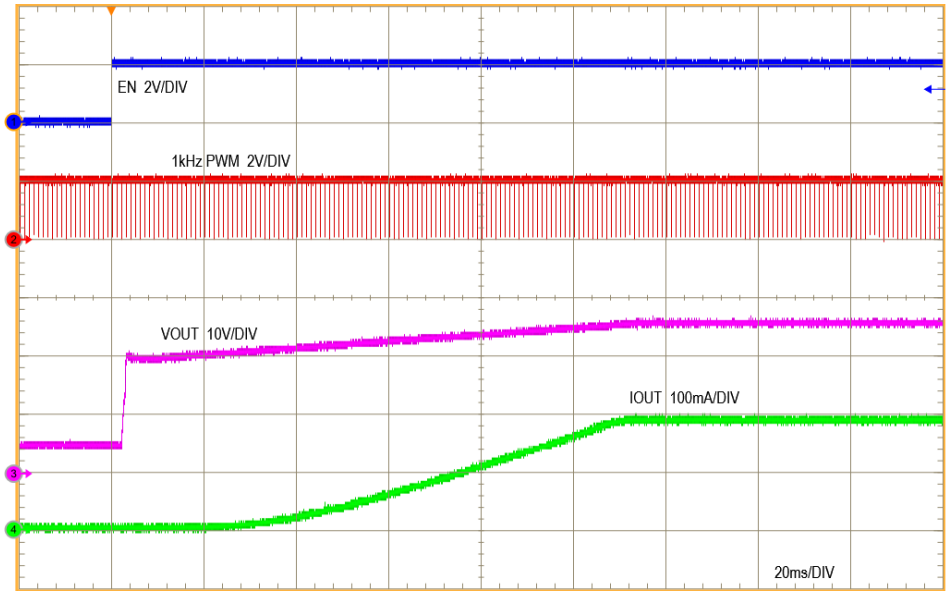

Figure 13. Startup Under 99% PWM Conditions. 6p8s Configuration

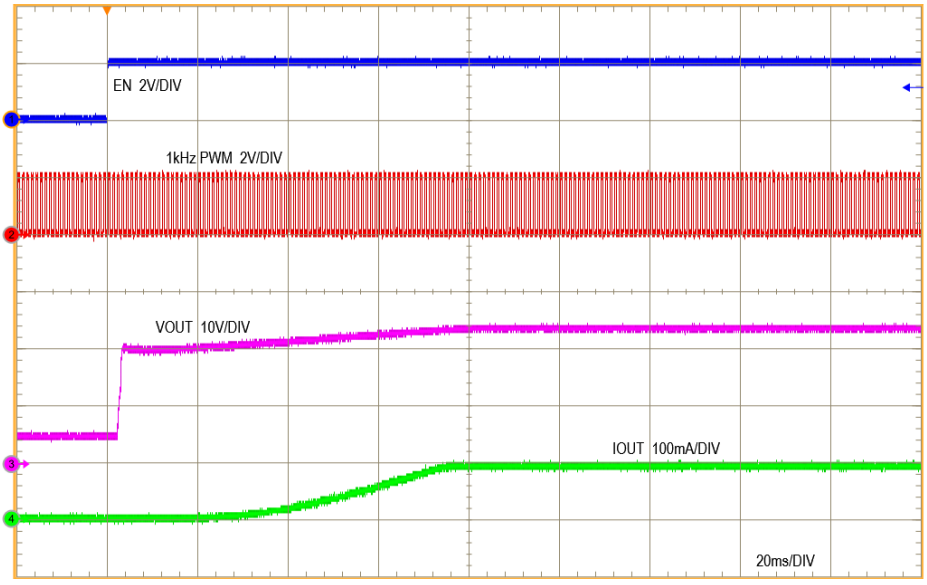

Figure 14. Startup Under 50% PWM Conditions. 6p8s Configuration

Typical Characteristics (cont'd.)

Unless otherwise specified, VIN=7.4V, L=15 µH TDK VLF504015-150M, Cout=4.7 µF, LED V=2.85V (typ), 512 kHz boost frequency.

Startup Waveforms (non-I²C mode)

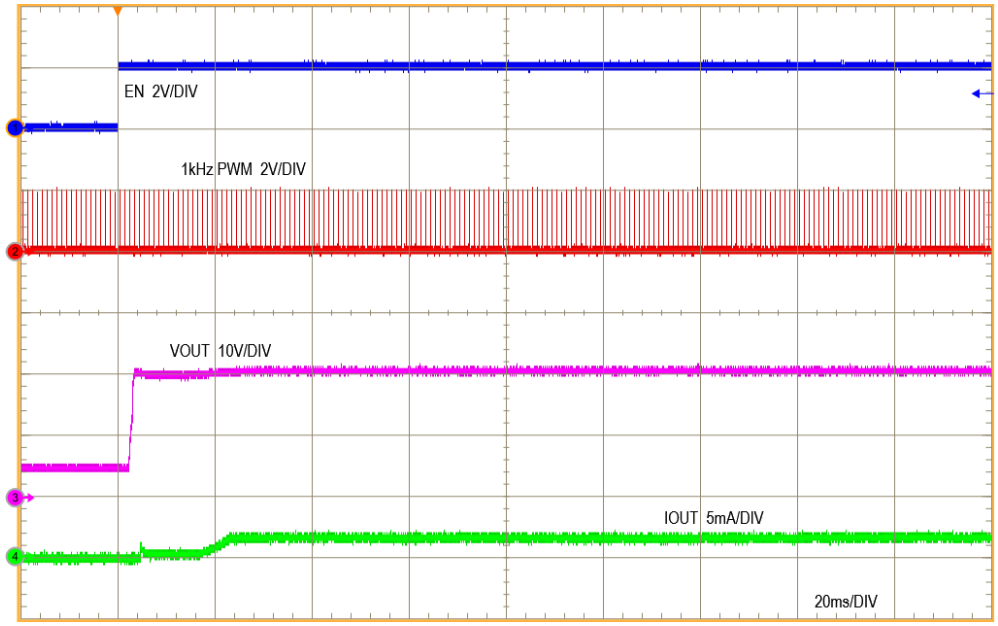

Figure 15. Startup Under 1% PWM Condition. 6p8s Configuration

Thermal Performance

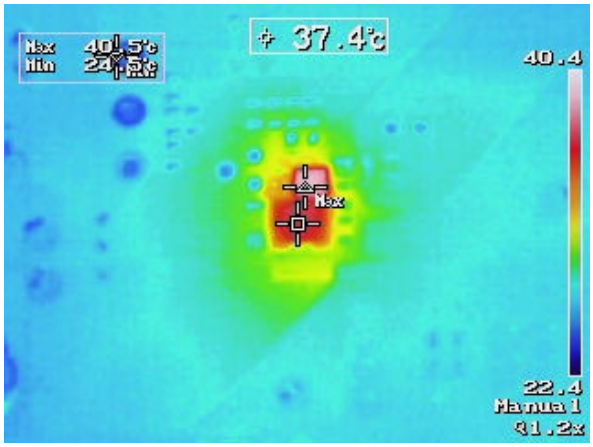

Figure 16.Thermal Performance
6p9s configuration, 180 mA, 7.4 VIN, 1.5 mm 15 µH Inductor. Board Temperature 24.5°C. Ambient Temperature 22.3°C. Maximum Temperature is 40.5°C Close to Center of ARC2C0608 Die

Detailed Description

The ARC2C0608 utilizes a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve very high peak efficiencies and superior efficiency over the dual-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the selection of LEDs.

The ARC2C0608 supports 1 to 6 LED strings. Unused LEDx pins should be tied to ground. This provides maximum design flexibility for wide variety of LCD screens.

The ARC2C0608 supports both I²C and non-I²C operation. It can be configured through I²C interface or external settings and allows combined I²C command settings with the PWM signal to adjust LED brightness.

The ARC2C0608 provides a full set of protection features to guarantee robust system operation, which include: input battery voltage under-voltage lockout (UVLO), thermal shutdown (TSD), boost and charge pump over-current protection (OCP), boost and charge pump output over-voltage and under-voltage protection (OVP and UVP), and LED open and short detection.

Input Sequencing Requirements

VDDIO determines if the device starts up in I2C or non-I2C mode. This input can be applied before or after VIN or EN, but it should be taken high (for I2C mode) or low (for non-I2C mode) before both VIN and EN are asserted. VDDIO should not be left floating. With VDDIO already established, both VIN and EN have to be asserted high before VDD comes up and the ARC2C0608 becomes operational. In I2C mode the first command can be given 1ms after both VIN and EN are asserted.

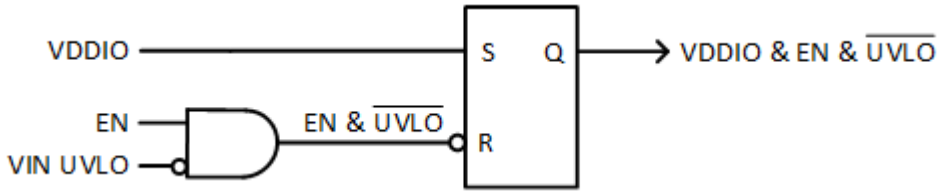

Figure 17. Input Sequencing Logic Diagram

If the part is enabled in non-I2C mode, VDDIO needs to be connected to the GND plane with a low inductance trace. In I2C mode, VDDIO can vary within its allowable voltage range. If this voltage drops too low, I2C communication will stop; however, the device will retain all its register values. I2C communication can resume 5µs after VDDIO becomes stable within its allowable voltage range.

In I2C mode, SCL and SDA serve as clock and data lines. In non-I2C mode SCL and SDA can be used to select between four IMAXTUNE settings depending on whether the pins are logic low or high.

The sequence for PWM does not matter. It can be switching according to the application requirements while all other signals are being turned on and off. For further clarification on various ARC2C0608 input signals, see Table 6.

VIN	EN	VDDIO	SCL	SDA	PWM	DEVICE STATUS
Low	-	-	-	-	Switching	Non-operational
High	Low	-	-	-	Switching	Non-operational
High	High	Low	IMAXTUNE setting	IMAXTUNE setting	Switching	Non-I²C operation
High	High	High	Clock	Data	Switching	I²C operation
Note: " Denotes level can be either High or Low and does not affect operation.						

Table 6. ARC 2C0608 Input Signals

Under-Voltage Lockout (UVLO)

ARC2C0608 provides continuous monitoring of the VIN input. When VIN voltage drops below approximately 4.3V, the ARC2C0608 will be immediately shut down.

Output Over-Voltage and Under-Voltage Protection

The ARC2C0608 protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is updated to a 1, and the ARC2C0608 turns off the boost converter. The boost converter automatically restarts after an OVP event when VOUT decreases below the threshold plus 0.5V typical hysteresis.

The over-voltage threshold can be configured through OVP_TH[1:0] bits in COMMAND register. The accuracy of each over-voltage threshold is +/-5%.

OVP_TH[1:0]	VOUT OVER-VOLTAGE THRESHOLD (V)
00	31.4
01	24
10	20

Table 7. Over Voltage Protection and OVP Threshold

In non-I2C mode, the OVP threshold is fixed at 31.4V.

The user should select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application to guarantee proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

The following explains all RESET and Standby states when the part uses the I²C interface:

For All Modes: UVLO high = POR IC (entire chip shut-down).

EN PIN LOGIC LEVEL	I²C_STANDBY BIT	LEDEN[6:1] BITS	RESET BIT	DEVICE STATUS	DEVICE CIRCUIT BLOCK STATUS	I²C REGISTERS
0	-	-	-	OFF	None	Cleared
1	0	0	0	Ready	References ON, Boost/CP off, LED Drivers on Standby.	I²C Accessible
1	0	>0	0	ON	All ON	I²C Accessible
1	1	-	-	Standby	All off except UVLO + critical reference circuits	I²C Accessible
1	0	-	1 (self-clearing)	Reset -> Ready (self-clearing)	Ready state after self-clearing reset	cleared
Note: "-" Denotes level can be either High or Low and does not affect operation						

Table 8. Reset and Standby States when I²C Interface is Used

The STATUS1 register bits are all cleared upon read, so repeated read-back of a logic-high fault bit indicates the fault event remains persistent. The LED_OPEN and LED_SHORT bits of STATUS2 register require the faulted string's LEDEN[n] or all enabled LEDEN[n] to be reset low, and then the bits to be read for them to be cleared.

Boost Output Over-Voltage and Under-Voltage Protection

The ARC2C0608 monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above a typical over-voltage threshold of 17V. When a VX OV occurs, the VX_OV bit of the STATUS1 register is updated to a 1, and the ARC2C0608 turns off the boost converter. The boost converter automatically restarts after a VX_OV event when VX decreases below the VX_OV threshold.

If the boost output voltage (VX) falls below (VIN-1.5)V, after the LED current sinks have turned on, the ARC2C0608 will shut down the switching converter and the LED current sinks immediately and register bit of VX_UV in STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and will not start unless the part is shutdown or reset as explained in Table 8.

Soft-Start Time-Out

The ARC2C0608 implements a soft-start time-out fault. If the output voltage does not rise above 2x the input voltage within 10ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in STATUS1 register is set to 1. This is a latched fault. The ARC2C0608 will not start up until a reset event occurs, i.e. by toggling EN low or setting the RESET bit in the COMMAND register (which clears itself).

Charge Pump Flying Capacitor Over-Voltage

The ARC2C0608 monitors the flying capacitor voltage relative to the VOUT voltage. When the voltage between the flying capacitor pins C1, C2 and VOUT exceed 18V typical, the switching converter and the LED current sinks are disabled immediately. The CAP_OVP bit of STATUS1 register is set to 1. The ARC2C0608 will not start up until a reset event occurs, for example, by toggling EN low or setting the RESET bit in the COMMAND register (which resets itself).

LED Short Protection

The ARC2C0608 includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator detects when the LEDx voltage rises above 6.3V typical, indicating a shorted LED fault. This fault condition may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings. The reduced forward voltage causes the current sink attached to that string to have a higher voltage on the LEDx pin than other current sinks, which could cause over-heating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED_SHORT fault is recorded in the STATUS2 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output will rise until it crosses OVP threshold. Any string whose LED pin is below the regulation point is blocked from controlling VOUT. Next, the output starts to decrease, and it is now controlled by the string with the lowest LED pin voltage. An LED_OPEN fault is recorded in STATUS2 register.

If the open LED string is re-connected, the LED current sink will re-establish current to the level it is able based on the output voltage, but it will not be allowed to control the Boost voltage. The LEDEN(n) corresponding to the string with the LED_OPEN fault needs to toggled low first, and then re-enabled in order to re-establish Boost control for that string.

Over-Current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit of 2.3A typically, but starts up initially with a derated over-current limit of 1.0A typically for soft-start. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults where the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds 3.9A, the converter and the LED current sinks are disabled immediately. The BST_ILIM_SEC bit in the STATUS1 register will be set and is cleared upon read. The switching converter and LED current sinks remain latched off and will not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented where if the current drawn out of the VOUT pin exceeds more than 250 mA, the LED current sinks are disabled and the output is disconnected from the charge-pump. The DISC_OCP bit in the STATUS1 register will be set. The LED current sinks are enabled again when the fault at the VOUT pin is removed.

Current Setting

In I^2C mode, the maximum current of the LED outputs is set by the MAX_I[1:0] register bits in the ILED_CONFIG register. The default maximum current is 30mA per LED string with 3 further settings available: 25 mA, 20 mA and 15 mA.

Fine tuning of the maximum current of the LED outputs can be set in I^2C mode by the IMAXtune[5:0] register bits in the ILED_CONFIG register. This allows incremental increases in the maximum output current from the MAX_I[1:0] setting mentioned above, in 6-bit resolution (64 steps) over a range from 0% to 41.5%, and at an average increase of 0.55% per step.

In non-I2C mode, the SDA and SCL pins can be used to select four of the trim levels from the IMAXtune[5:0] register as described in Table 9.

SDA	SCL	IMAX PER STRING INCREASE	CORRESPONDING IMAXTUNE[5:0] REGISTER VALUE
0	0	MAX_I + 0%	0x00
0	1	MAX_I + 2.41%	0x05
1	0	MAX_I + 4.96%	0x0a
1	1	MAX_I + 7.64%	0x0f

Table 9. Four Trim Levels from IMAXtune[5.0] Register

In addition, the maximum current can be adjusted by an external resistor, R_{ISET} connected between ISET pin and ground, when the ISET bit is set to 1 in the LEDEN register. R_{ISET} controls the full scale LED current in conjunction with the current determined by the MAX_I register bits as follows:

$$I_{LED\_FULL} = \frac{0.4}{R_{ISET}} * K_{ISET}$$

The R_{ISET} range is between 24.9 KΩ to 250 KΩ. In PWM mode, the output current of the LED can be calculated from the duty cycle of the PWM input as follows:

$$I_{LED} = \frac{0.4}{R_{ISET}} * K_{ISET} * PWM\ Duty\ Cycle$$

In non-I²C mode, the above formula applies with K_{ISET} = 1875. This value is factory trimmed, contact pSemi for other options.

Boost Converter Switching Frequency

In I²C mode, the ARC2C0608's boost converter provides wide frequency selection to meet different users' requirements. Five bits are used to set the boost switching frequency, which are the FSW_BOOST[4:0] bits in the CONFIG register. See Table 10.

In non-I²C mode, the boost switching frequency is set by the FSET pin, which is sampled once at startup. Changing the FSET pin bias after boost switching has started will not change the boost switching frequency. The table below shows the boost switching frequency settings through I²C register value. It also shows how FSET determines the boost frequency in non-I²C mode.

The choice of inductor, charge pump fly capacitors and compensation components is dependent on the selected boost switching frequency for proper part operation. Contact pSemi for recommended component types and values.

DIVISION OF MASTER	FREQ (KHZ)	FSW_BOOST[4:0]		NON-I²C
		HEX CODE	BINARY CODE	
3	3413.33	2	00010	
4	2560.00	3	00011	
5	2048.00	4	00100	
6	1706.67	5	00101	
7	1462.86	6	00110	
8	1280.00	7	00111	
9	1137.78	8	01000	Tie to VDD
10	1024.00	9	01001	
11	930.91	A	01010	
12	853.33	B	01011	
13	787.69	C	01100	
14	731.43	D	01101	Floating
15	682.67	E	01110	
16	640.00	F	01111	
17	602.35	10	10000	
18	568.89	11	10001	
19	538.95	12	10010	
20	512.00	13	10011	Tie to GND
21	487.62	14	10100	
22	465.45	15	10101	
23	445.22	16	10110	
24	426.67	17	10111	
25	409.60	18	11000	
26	393.85	19	11001	
27	379.26	1A	11010	
28	365.71	1B	11011	
29	353.10	1C	11100	
30	341.33	1D	11101	
31	330.32	1E	11110	
32	320.00	1F	11111	

Table 10. FSW_BOOST[4:0] Bits in the CONFIG Register

FSET shorted to V=	1138 kHz
FSET open	731 kHz
FSET shorted to ground	512 kHz

Charge Pump Switching Frequency

The relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency is given in Table 11.

LED CURRENT SETTING	CHARGE PUMP FREQUENCY RATIO
100% - 75%	/2
75% - 50%	/4
50% - 0%	/8

Table 11. LED Current Settings and Charge Pump Frequency Ratio

Switching Converter Compensation

The switching converter operates in voltage-mode control and uses external compensation. Type-III compensation is recommended which requires 3 components as shown in Figure 18.

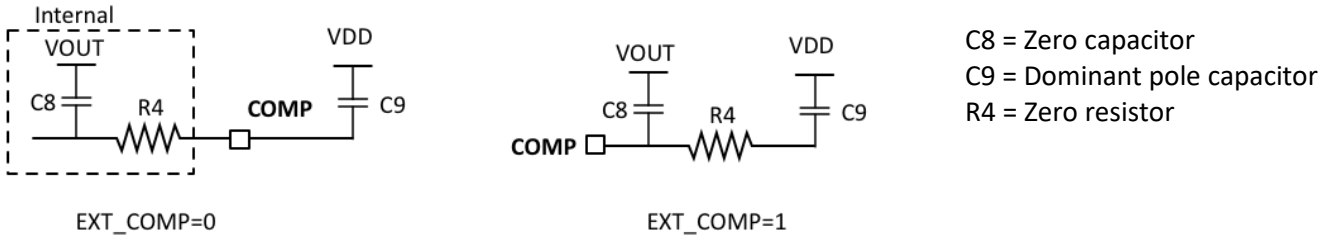

Figure 18. Compensation Components

When the I²C register bit EX_COMP=0, the ARC2C0608 has the Zero components C8 and R4 populated internally and only requires the dominant pole C9 connected to the COMP pin. Additional I²C register bits SEL_ZERO2[1:0] and SEL_ZERO1[1:0] can adjust the values of C8 and R4 internally over a limited range.

More compensation control can be obtained by setting the register bit EXT_COMP=1 which requires all 3 components to be populated externally.

The default compensation mode when using a non-I²C interface is with internal Zero components only (EXT_COMP=0). Contact pSemi for compensation recommendations for your application.

LED Current Output Dimming

The ARC2C0608 supports four LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency and minimal WLED color shift at low brightness levels. These options are Analog, Phase Shift PWM, Hybrid PWM (Mixed-Mode), and Direct PWM (DPWM) dimming.

Analog Dimming

In I²C mode, when ILED_CONFIG bit 6, DIM_MODE is set to 0, dimming is set to analog only. In analog dimming, the LED current sink output is always a dc current across the entire brightness range. As brightness is reduced, the LED current sink output dc level decreases which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the VOUT voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a dc current output also minimizes noise in the system. When using a non-I²C interface, the full-scale output current per channel can be scaled using an external resistor, R_{ISET}, connected between the ISET pin and analog ground. The tolerance of the external resistor R_{ISET} directly affects the accuracy of the LED current sink output, so using a precision resistor is recommended. The recommended R_{ISET} resistor range is 24.9kΩ to 250kΩ, with 25kΩ corresponding to a 30mA full-scale current output per channel when the register bits MAX_I[1:0]=11.

Phase Shift PWM Dimming

In I²C mode, when ILED_CONFIG register bit 6, DIM_MODE bit is set to 1, dimming is set to mixed dimming. Under this mode, the mixed dimming block generates phase shifted PWM signals to dim active LED strings when the required LED current is below the threshold set by PWM_IX register bits. The phase difference between active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

Since the input code is a 12 bit value, the PWM Generator uses the 8 bits of the register 0x08 for the msb portion mapped as bits WLED_ISET[11:4] and the upper nibble of register 0x07 for the lsb portion mapped as bits WLED_ISET[3:0] in the 12 bit value. Depending on the PWM frequency selected, the lower bits are truncated. Figure 19 shows how the register bits are used.

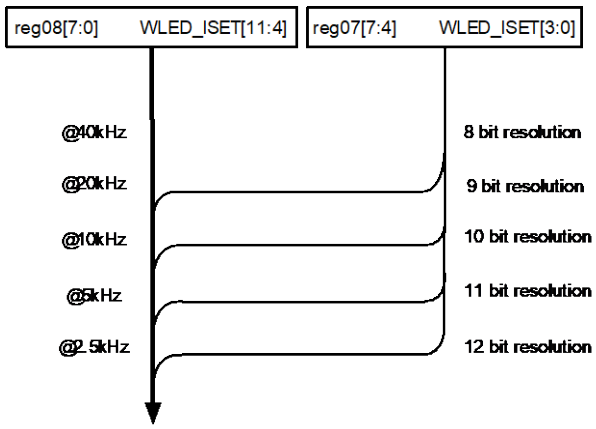

Figure 19. Relationship Between Frequency and Resolution in Phase Shift PWM Dimming

The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

If the PWM frequency is set at 40 kHz only the WLED_ISET_MSB register at address 0x08 is considered. For a higher resolution and lower frequencies, the user needs to write first to the upper 4 bits of the WLD_ISET_LSB register at address 0x07, and then the WLED_ISET_MSB register. The minimum PWM pulse width is typically 200ns with a resolution of 97.66ns.

In non-I²C mode, when the MODE pin is floating, the phase-shifted PWM scheme is enabled.

Hybrid PWM (Mixed) Dimming

The ARC2C0608 allows a mixed dimming control scheme for better optical efficiency. The switch point from analog to PWM control is set by register bits DIM_MODE and PWM IX[1:0], and can be 0%, 12.5%, 25%, 50% or 100% of the brightness range. 0% means the analog dimming is used across the whole brightness range and 100% means PWM dimming is used across the whole brightness range. In the brightness range above the switch point analog dimming is adopted, and below the switch point PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved.

PWM_IX[1:0]=11 results in a dc output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.

PWM_IX[1:0]=10 results in a dc output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.

PWM_IX[1:0]=01 results in a dc output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.

PWM_IX[1:0]=00 results in a dc output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

An example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting is shown in Figure 20.

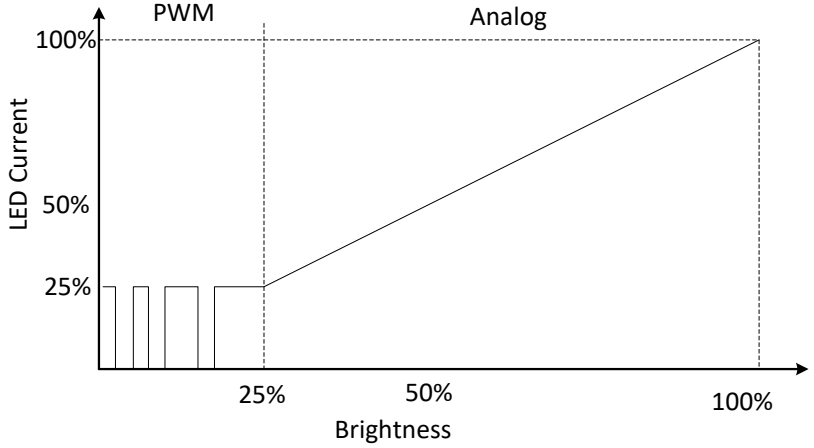

Figure 20. Mixed Dimming Control

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Since the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also has to scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0]=01 (25% transition point) is four times longer than at PWM_IX[1:0]=11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is 200ns typically.

When using a non-I²C interface, the brightness transition point between analog dimming and PWM dimming is fixed at 25%. Contact pSemi for alternate transition point options.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of 5 frequency settings between 2.5kHz and 40kHz using the PWM_DIM_FREQ[2:0] register bits. When using a non-I²C interface, the PWM dimming frequency of the LED current outputs is fixed at 2.5kHz. Contact pSemi for alternate frequency options.

In general, the dimming resolution at the LED current output is related to the PWM dimming frequency and the hybrid transition point, with a higher resolution achieved with a lower PWM dimming frequency and lower transition point. For example, for a 25% transition point, a 12-bit resolution is possible at the 10kHz PWM_DIM_FREQ[2:0]=010 setting or lower, an 11-bit resolution is possible at the 20kHz PWM_DIM_FREQ[2:0]=011 setting, and so forth.

To help reduce audible noise, the LED current pulses during PWM dimming are always phase-shifted, which reduces the current and voltage ripple on the output capacitor. The equivalent PWM frequency seen by this output capacitor is increased by the number of enabled LED channels. The phase shift between each LED channel is equal to 360° divided by the number of enabled LED channels. This phase shift is automatically adjusted as the number of enabled LED channels is changed during operation.

Direct PWM (DPWM) Dimming

The brightness is directly proportional to the duty cycle applied at the PWM pin. The LED current outputs are no longer phase-shifted but are synchronized with the timing edges at the PWM pin.

In I²C mode, when the DIMCODE register bits are set to 11, the direct PWM dimming mode is selected. In non-I²C mode, tying the MODE pin to the VDD pin will select direct PWM dimming.

In direct PWM dimming mode, the input PWM signal switches the LED strings on and off directly, with the LED current on when PWM is high. The mixed dimming block is bypassed, and there is no phase shift among the LED strings. The minimum PWM pulse width allowed under direct PWM dimming is 200ns. The PWM input frequency range is from 200 Hz to 20 KHz in this mode.

LED Current Full-Scale or 100% Brightness

The maximum LED Current full-scale can be programmed using either I²C or an external resistor, both of which provide for fine tuning. In non-I²C mode the current set by the ISET resistor can be trimmed upwards by four set levels using the SDA and SCL pins. Details of these options can be found under the section titled Current Setting on page 29.

LED Brightness Control

The LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET[11:0] bits written via the I²C interface, or both. The register bits DIMCODE[1:0] sets up different dimming schemes:

DIMCODE=00

When DIMCODE=00, the LED current is controlled by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate the brightness code. The resulting code goes into the mixed dimming block to generate a DC current level or six phase-shifted PWM signals to control the LED strings.

In non- I²C mode, the LED dimming is controlled by the PWM input only, with the full scale current set by the resistor on the ISET pin.

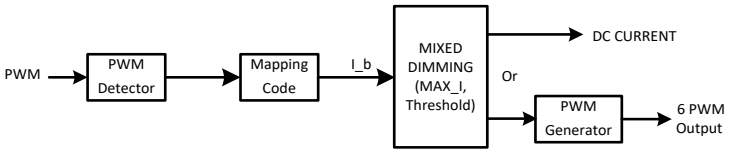

Figure 21: DIMMCODE=00

DIMCODE=01

When DIMCODE=01, the LED current is controlled by the WLED_ISET[11:0] bits via I²C. The register codes go through a mapping first, then through the mixed dimming block to generate DC current or six phase-shifted PWM signals to control the LED strings.

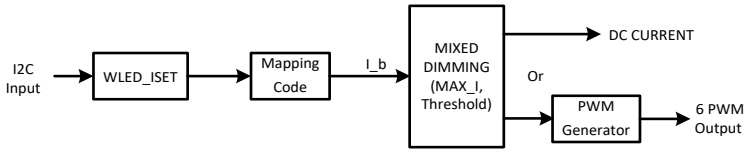

Figure 22: DIMMCODE=01

DIMCODE=10

When DIMCODE=10, the LED current is controlled by both the PWM input duty cycle and the WLED_ISET[11:0] bits via I²C. The WLED_ISET[11:0] bits go through a mapping and then are multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate DC current or six phase-shifted PWM signals to control the LED strings.

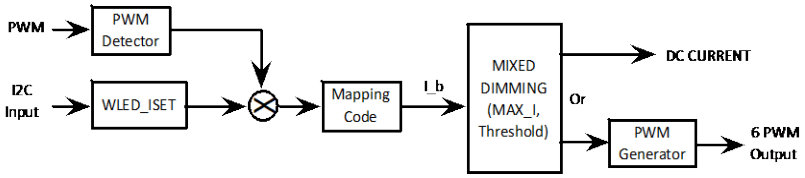

Figure 23: DIMMCODE=01

DIMCODE=11

When DIMCODE=11, direct PWM dimming is enabled. Under this setting, the input PWM signal turns the active LED strings on and off directly and the internal decoding circuitry and mixed dimming block are bypassed. The minimum input PWM pulse width is limited to 200ns under direct PWM dimming.

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either via the PWM input or WLED_ISET[11:0] bits are translated linearly into the time-averaged LED current. This is the default setting.

For a better visual experience, ARC2C0608 can also translate the dimming settings via a logarithmic mapping to produce the LED current. The user can set the LOG_MODE bit to 1 in the ILED_CONFIG register to enable this feature. There are only 1023 possible brightness states in this mode.

Operation with DIMCODE=00 or 10

In these modes, the ARC2C0608's PWM input frequency range is from 200 Hz to 40 KHz. The input frequency is independent of the PWM output frequency which is the six phase LED current switching frequency. In I^2C mode, the PWM output frequency is set by the PWM_DIM_FREQ register. In non-I^2C mode, the PWM output frequency is fixed at 2.5 kHz.

Note that since the on-chip clock is 10.24MHz, the full 12 bit dimming resolution can only be implemented with a 2.5 KHz PWM input signal or lower ($10.24MHz/2^{12}$ = 2.5KHz). Higher PWM input frequencies will have reduced dimming resolution, with 8 bits of dimming resolution available at 40 KHz.

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0]=11). When 25% PWM dimming is used, a 40 KHz PWM output frequency provides 10 bits of dimming resolution relative to the full-scale LED output current ($10.24\ MHz/2^{10}/25\%$ = 40 KHz).

MODE Pin

In non-I^2C mode, the MODE pin is used to enable analog, phase-shifted PWM dimming or direct PWM dimming. This pin is sampled once at startup. Changing its bias after startup will not change the dimming scheme. See Table 12 for details.

MODE PIN	DIMMING SCHEME
Tied to ground	Analog dimming
Floating	Mixed dimming with a phase-shifted 2.5KHz internally-generated PWM frequency. Transition point is 25%.
Tied to VDD pin	Direct PWM dimming

Table 12. Mode Pin and Dimming Scheme

Fade In/Out Control

The Fade In/Out control makes a smooth transition from one brightness value to another for a better human eye experience. ARC2C0608 provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED[7:0] bits in the WLED_FADING_CTRL register. This register can set the speed from 50us/step (0x01) to 12.75ms/step (0xFF) or disabled (0x00) based on user preference. See the Register WLED_FADING_CTRL section for detailed description.

In non-I²C mode, FADING_SPEED[7:0] is set to 0x00 to give users full control via the PWM input.

Digital R-C Filter for Non-DPWM Mode Brightness Changes

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to pick a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC-filter is used to filter the output brightness change response to each input brightness change.

2 bits RCFILTER[1:0] control the coefficient of this RC time constant as shown in Table 13 for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings. The RCFILTER[1:0] bits are available in I²C mode through register 0Bh bits[3:2]. Note that this setting can only be changed when the LED strings are off.

RCFILTER[1:0]	FILTER FUNCTION / LEVEL	TIME TO REACH NEW STEADY-STATE OUTPUT GIVEN A BRIGHTNESS CHANGE BETWEEN 1% AND 99%
00	Disabled	0s or one PWM_DIM_FREQ[2:0] period(*)
01	Low	~3.7s
10	Medium	~1.7s
11	High	~0.8s
*Note: * Depending on how the brightness change command lines up with the internal PWM clock edge.*		

Table 13. RC Filter and Time to Reach Steady State Output

Input PWM Filter for Non-DPWM Mode

When a duty cycle is applied at the PWM pin to control brightness in non-DPWM mode, the on-time and period are sampled by the internal 10.24MHz master clock to translate time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by +/-1 LSB at steady-state, which translates into jitter on the final brightness result and this can be visible as flicker. Adding some basic filtering to this sampled system can help eliminate this flicker at steady-state.

2 register bits PWMFILTER[1:0] enable/disable this filter as well as control the amount of filtering. Furthermore, the filtering is dependent on the direction of the sampled PWM time-step as follows: if the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold. Conversely, if the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.

PWMFILTER[1:0]	MINIMUM PWM TIME STEP SIZE
00	Disabled
01	2 steps
10	4 steps
11	8 steps

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and managing device slave addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The ARC2C0608 operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps), fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long VIN voltage remains above 4.45V, the EN pin remains logic high, and the VDD regulator output voltage remains above 3.0V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The ARC2C0608 supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as '0110000'. The lower 3-bits are programmable as described below.

Programming I²C Slave Address - Multiple Parts on One I²C Bus

To enable multiple ARC2C0608 parts to be addressed on one I²C bus, the lower 3 bits of the I²C slave address are I²C-accessible registers and allow the I²C slave address for each part to be customized during startup. This is done by enabling each ARC2C0608 in sequence. A special code equal to 6Ch must first be written to register 1Ah before the lower three bits of the I²C slave address can be written to a non-zero code in register 1Bh.

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 24. All I²C-compatible devices should recognize a start condition.

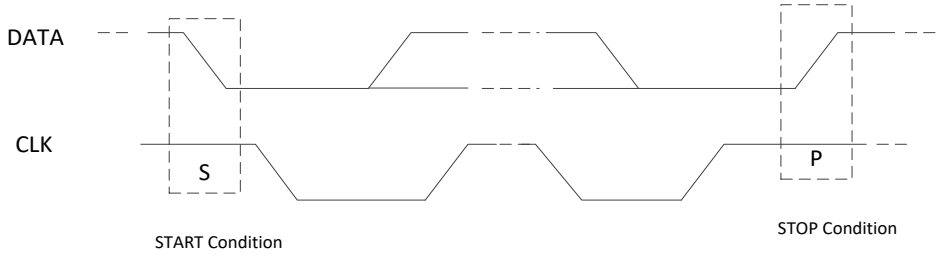

Figure 24. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (Figure 25). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 26), by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that a communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 27). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

ARC2C0608 I²C Update Sequence

The ARC2C0608 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, ARC2C0608 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the ARC2C0608. The ARC2C0608 performs an update on the falling edge of the acknowledge signal that follows the LSB.

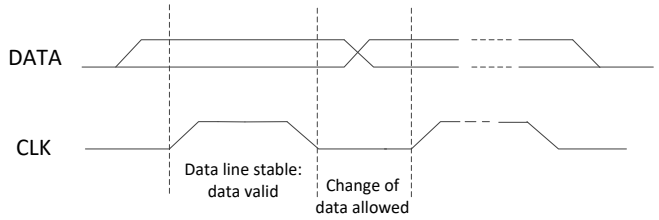

Figure 25. Bit Transfer on the Serial Interface

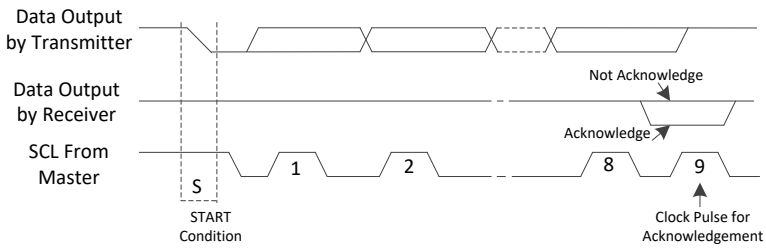

Figure 26. Acknowledge on the I²C Bus

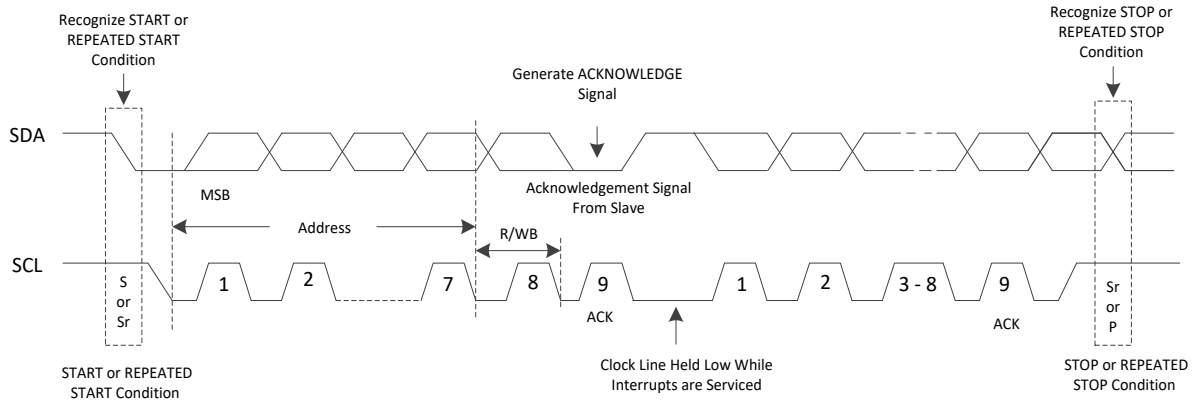

Figure 27. Bus Protocol

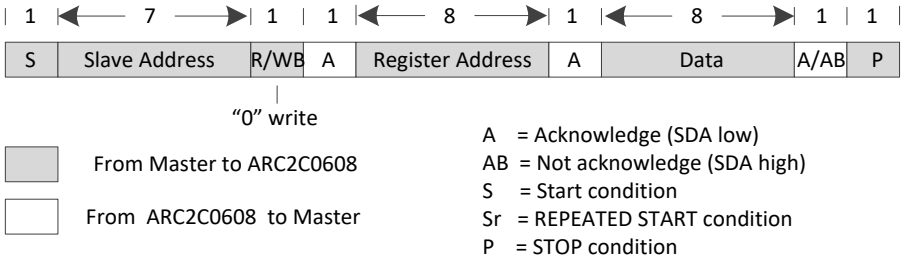

Figure 28. "Write" Data Transfer Format in Standard-, Fast, Fast-Mode Plus

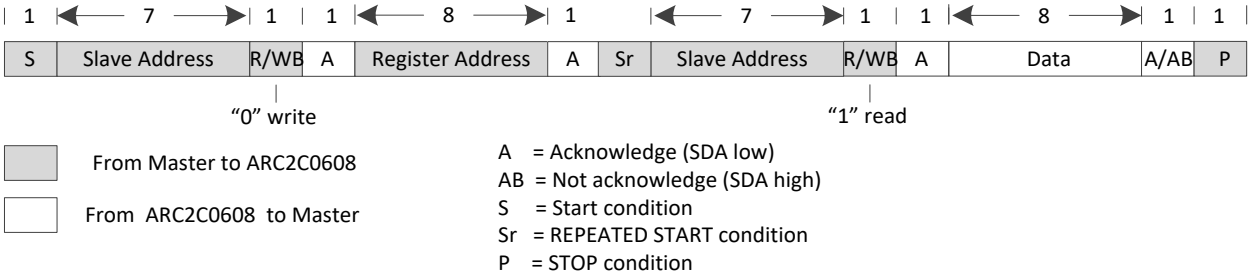

Figure 29. "Read" Data Transfer Format in Standard-, Fast, Fast-Mode Plus

Register Map

Slave Address: 0110000 (0x30) (1)

Register Configuration Parameters

REGISTER	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	I2C_Standby	RESET	Reserved	Boost_mode	OVP_TH[1:0]		Reserved	EXT_COMP
CONFIG	0x01	Reserved[7:5]			FSW_BOOST[4:0]				
STATUS1	0x02	BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	CAP_OVP	DISC_OCP	TSD	SS_TIMEOUT
STATUS2	0x03	Reserved [7:2]						LED_OPEN	LED_SHORT
WLED_ FADING_CTRL	0x04	FADING_SPEED[7:0]							
ILED_CONFIG	0x05	LOG_MODE	DIM_MODE	PWM_IX[1:0]		DIM_CODE[1:0]		MAX_I[1:0]	
LEDEN	0x06	ISET_EXT	Reserved	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]
WLED_ISET_ LSB	0x07	WLED_ISET[3:0]				Reserved [3:0]			
WLED_ISET_ MSB	0x08	WLED_ISET[11:4]							
PWM_DIM_ FREQ	0x09	Reserved [7:3]					PWM_DIM_FREQ[2:0]		
CONFIG_ COMP	0x0A	LEDVREGCNTINIT[7:4]				SEL_ZERO2[1:0]		SEL_ZERO1[1:0]	
FILTER_SETTINGS	0x0B	Reserved				RCFILTER[1]	RCFILTER[1]	PWMFILTER[1]	PWMFILTER[0]
IMAXTUNE	0x0C	Reserved		IMAXTUNE[5]	IMAXTUNE[4]	IMAXTUNE[4]	IMAXTUNE[2]	IMAXTUNE[1]	IMAXTUNE[0]
I2C PASSWORD	0x1A	I2CPASS[7]	I2CPASS[6]	I2CPASS[5]	I2CPASS[4]	I2CPASS[3]	I2CPASS[2]	I2CPASS[1]	I2CPASS[0]
I2C LOWER 3 BITS	0x1B						I2CADDR[3]	I2CADDR[1]	I2CADDR[0]

*Note: *. Excluding read/write bit. 01100000 (0x60) if including read/write bit.*

Detailed Register Description

Register COMMAND

ADDRESS	NAME	POR VALUE
0x00	COMMAND	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C Standby	RESET	Reserved	BOOST_MODE	OVP_TH[1:0]		Reserved	EXT_COMP

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
I²C Standby	[7]	R/W	0x0	Standby low-power mode with I²C interface and registers accessible.
RESET	[6]	R/W	0x0	Write 1 to reset the device. This bit is self-clearing.
Reserved	[5]	R/W	0x0	
BOOST_MODE	[4]	R/W	0x0	Boost converter operating mode 0=Discontinuous conduction mode (DCM) (Default) 1=Continuous conduction mode (CCM)
OVP_TH[1:0]	[3:2]	R/W	0x0	Output over-voltage protection threshold 00 = 31.4V (Default) 01 = 24V 10 = 20V 11 = reserved
Reserved	[1]	R/W	0x0	
EXT_COMP	[0]	R/W	0x0	0=use partially external compensation network 1=use 100% external compensation network

Register CONFIG

ADDRESS	NAME	POR VALUE
0x01	CONFIG	0x29

Bit Assignment

7	6	5	4	3	2	1	0
			FSW_BOOST[4:0]				

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
Reserved	[7:5]	R/W	0x1	
FSW_BOOST[4:0]	[4:0]	R/W	0x09	Boost switching frequency. See Boost Converter Switching Frequency section for full frequency chart. 13h = 512KHZ 09h = 1.024MHz (Default) 04h = 2.048MHz 03h = 2.56MHz

Register STATUS1

ADDRESS	NAME	POR VALUE
0x02	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	CAP_OVP	DISC_OCP	TSD	SS_TIMEOUT

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
BST_ILIM_SEC	[7]	RO	0b	Status bit to flag a secondary boost current limit condition 0=no secondary current limit 1=Boost current exceeds secondary current limit
VOUT_OVP	[6]	RO	0b	Status bit to flag an output over-voltage condition 0=no OVP condition 1= Output voltage is above OVP threshold
VX_OV	[5]	RO	0b	Status bit to flag a VX node over-voltage condition 0=no VX over-voltage condition 1= VX voltage is above OVP threshold
VX_UV	[4]	RO	0b	Status bit to flag a VX node under-voltage condition 0=no VX under-voltage condition 1= VX voltage is below UVP threshold
CAP_OVP	[3]	RO	0b	Status bit to flag a charge pump capacitor over-voltage condition 0=no charge pump capacitor over-voltage 1= charge pump capacitor voltage is above OVP threshold
DISC_OCP	[2]	RO	0b	Status bit to flag a disconnect switch over-current condition 0=no disconnect switch over-current 1= current through the disconnect switch is above over-current threshold
TSD	[1]	RO	0b	Status bit to flag a thermal shutdown condition 0=no thermal shutdown condition 1= part exceeds the thermal shutdown threshold
SS_TIMEOUT	[0]	RO	0b	Status bit to flag a soft start timeout condition 0=no soft start timeout condition 1= soft start hasn't finished within the pre-defined time

Register STATUS2

ADDRESS	NAME	POR VALUE
0x03	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved [7:2]						LED_OPEN	LED_SHORT

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
Reserved	[7:2]	RO	0b	
LED_OPEN	[1]	RO	0x0	An LED OPEN condition was detected on one or more strings. Status bit to flag an LED OPEN condition: 0 = No LED open 1 = LED open condition detected on one or more strings. Once set, this bit will stay set until the STATUS2 register is read and the individual LEDEN[n] corresponding to the open string is reset low.
LED_SHORT	[0]	RO	0x0	An LED SHORT condition was detected on one or more strings* Status bit to flag an LED SHORT condition: 0 = No LED short 1 = LED short condition detected on one or more strings. Once set, this bit will stay set until the STATUS2 register is read and all LEDEN[6:1] are reset low.
*Note: * If only one string is operating, then it is not possible to detect a LED SHORT condition.*				

Register WLED_FADING_CTRL

ADDRESS	NAME	POR VALUE
0x04	WLED_FADING_CTRL	0x00

Bit **Assignment**

7	6	5	4	3	2	1	0
FADING_SPEED[7:0]							

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
FADING_SPEED	[7:0]	R/W	0x00	Sets the fading counter from 50 µs to 12.75 ms in 50 µs steps. This is the period between each intensity step. 0x00 = Fading disabled 0x01 = 50us/step … 0xFF = 12.75ms/step

Register ILED_CONFIG

ADDRESS	NAME		POR VALUE
0x05	ILED_CONFIG		0x53

Bit Assignment

7	6	5	4	3	2	1	0
LOG_MODE	DIM_MODE	PWM_IX[1:0]		DIMCODE[1:0]		MAX_I[1:0]	

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
LOG_MODE	[7]	R/W	0b	LED brightness control profile 0 = linear (default) 1 = logarithmic
DIM_MODE	[6]	R/W	1b	LED Current Output Dimming mode 0 = Analog dimming only 1 = Hybrid PWM dimming mode (default)
PWM_IX[1:0]	[5:4]	R/W	01b	Hybrid PWM dimming transition point between PWM dimming and analog dimming 00 = 12.5% of full scale current 01 = 25% of full scale current (default) 10 = 50% of full scale current 11 = 100% of full scale current or PWM dimming only
DIMCODE[1:0]	[3:2]	R/W	00b	LED brightness control 00 = PWM input duty cycle dimming (default) 01 = WLED_ISET[11:0] 10 = both PWM duty cycle and WLED_ISET[11:0] 11 = Direct PWM Dimming
MAX_I[1:0]	[1:0]	R/W	11b	WLED full scale current (100% brightness). 00 = 15 mA 01 = 20 mA 10 = 25 mA 11 = 30 mA (default)

Register LEDEN

ADDRESS	NAME	POR VALUE
0x06	LEDEN	0x00

Bit **Assignment**

7	6	5	4	3	2	1	0
ISET_EXT	Reserved	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
ISET_EXT	[7]	R/W	0b	LED full scale current setting pin 0 = MAX_I bits in ILED_CONFIG register set full scale LED current 1 = External resistor RISET and current multiplier KISET program the full scale LED current
Reserved	[6]	R/W	0b	
LEDEN[6], …, LEDEN[1]	[5:0]	R/W	0x0	LED string enables 0 = string is disabled 1 = string is enabled

Register WLED_ISET_LSB

ADDRESS	NAME	POR VALUE
0x07	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				Reserved[3:0]			

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
WLED_ISET[3:0]	[7:4]	R/W	0x00	LED output current setting Bits 3-0. For details please refer to the WLED section. If changing the LSB bits, these must be written before the MSB bits. Changes to these bits are only implemented when the next register is written, which is typically the MSBs but could be any register.
Reserved	[3:0]			

Register WLED_ISET_LSB

ADDRESS	NAME	POR VALUE
0x08	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[11:4]							

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
WLED_ISET[11:4]	[7:0]	R/W	0x00	The MSB bits of the WLED_ISET[11:0] brightness code. For details please refer to the WLED section.

Register PWM_DIM_FREQ

ADDRESS	NAME	POR VALUE
0x09	PWM_DIM_FREQ	0x01

Bit Assignment

7	6	5	4	3	2	1	0
Reserved					PWM_DIM_FREQ[2:0]		

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
Reserved	[7:3]	R/W		
PWM_DIM_FREQ	[2:0]	R/W	001b	PWM_DIM_FREQ (KHz) 000=2.5 001=5 (default) 010=10 011=20 100 =40 101, …, 111= reserved

Register CONFIG_COMP

ADDRESS	NAME	POR VALUE
0x0A	CONFIG_COMP	0x70

Bit Assignment

7	6	5	4	3	2	1	0
LEDVREGCNTINIT[7:4]				SEL_ZERO2[1:0]		SEL_ZERO1[1:0]	

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
LEDVREGCNTINIT	[7:4]	R/W	0x07	Initial count for setting VOUT target voltage at startup 0x00=8.9V … 0x07=19.1V … 0x0F=30.8V
SEL_ZERO2[1:0]*	[3:2]	R/W	00b	Selects internal feed forward zero frequency 00=11.6KHz 01=8.4KHz 10=7.1KHz 11=6.1KHz
SEL_ZERO1[1:0]*	[1:0]	R/W	00b	Selects internal zero resistance 00=0Ω 01=4.2kΩ 10=8.4kΩ 11=16.8kΩ
*Note: * The SEL_ZERO2[1:0] and SEL_ZERO1[1:0] bits are active only when the EXT_COMP bit from register 00h is 0. When EXT_COMP=1, the SEL_ZERO2[1:0] and SEL_ZERO1[1:0] bits are ignored.*				

Register FILTER_SETTINGS

ADDRESS	NAME	POR VALUE
0x0B	FILTER_SETTINGS	0x00

Bit **Assignment**

7	6	5	4	3	2	1	0
Reserved				RCFILTER[1]	RCFILTER[0]	PWMFILTER[1]	PWMFILTER[0]

Bit **Description**

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
Reserved	[7:4]			
RCFILTER[1:0]	[3:2]	R/W	00b	Status 00 = RC filter OFF (default) 01 = LOW 10 = MEDIUM 11 = HIGH
PWMFILTER[1:0]	[1:0]	R/W	00b	Status 00 = OFF (default) 01 = 2 STEPS 10 = 4 STEPS 11 = 8 STEPS

Register IMAXTUNE

ADDRESS	NAME	POR VALUE
0x0C	IMAXTUNE	0x00

Bit **Assignment**

7	6	5	4	3	2	1	0
Reserved		IMAXTUNE[5]	IMAXTUNE[4]	IMAXTUNE[3]	IMAXTUNE[2]	IMAXTUNE[1]	IMAXTUNE[0]

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
Reserved	[7:6]			
IMAXTUNE [5:0]	[5:0]	R/W	00b	Sets percentage increase of Maximum LED Current MAX_I[0:1] (non-linear but monotonic increase vs code): 0x00 = 0% increase …. 0x20 = 20.2% increase …. 0x3F = 41.5% increase

Register I2C_PASSWORD

ADDRESS	NAME	POR VALUE
0x1A	I2C_PASSWORD	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2CPASS[7]	I2CPASS[6]	I2CPASS[5]	I2CPASS[4]	I2CPASS[3]	I2CPASS[2]	I2CPASS[1]	I2CPASS[0]

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
I2CPASS[7:0]	[7:0]	R/W	00b	I²C Password setting for lower 3 bits = 0x6C

Register I2C_LOWER_3_BITS

ADDRESS	NAME	POR VALUE
0x1B	I2C_LOWER_3_BITS	0x00

Bit Assignment

7	6	5	4	3	2	1	0
					I2CADDR[3]	I2CADDR[2]	I2CADDR[1]

Bit Description

FIELD NAME	BITS	TYPE	POR	DESCRIPTION
I2CADDR[3:1]	[2:0]	R/W	00b	Lower 3 bits enable assignment of unique I2C address in multi-part applications

Application Schematic

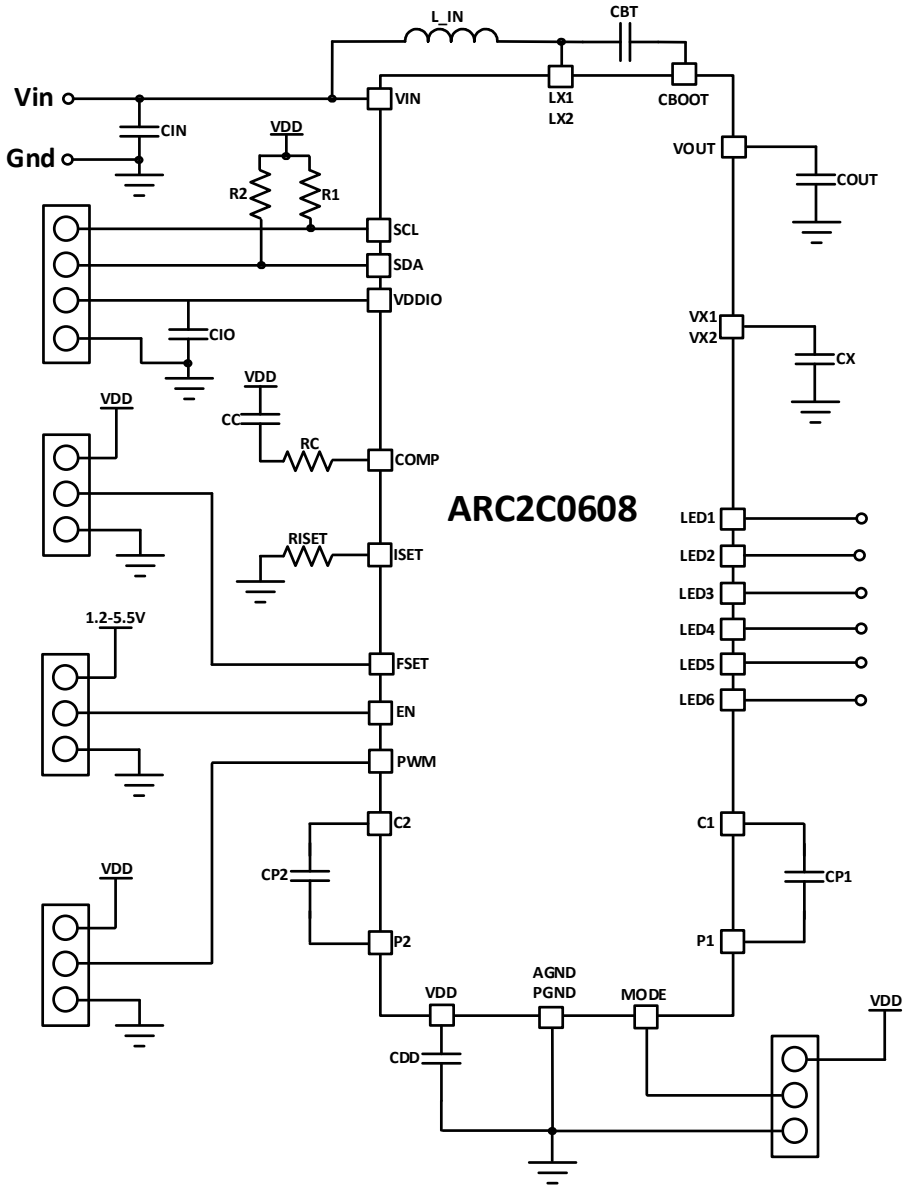

Figure 30. Detailed Application Schematic

Application Circuit Part List

(Reference to Figure 30 Detailed Application Schematic)

COMPONENT NAME	VALUE	PART SIZE	MANUFACTURER'S PART NUMBER
CBT	22nF 50V X7R	C0402	GRM155R71H223KA12D
CX	470nF 25V X5R	C0402	GRM155R61E474KE01
CP1, CP2	2.2uF 25V X7R	C0805	GRM21BR71E225KA73
CIN (1)	1.0uF 16V X5R	C0603	GRM188R61C105KA12D
CC	5.6nF X5R	C0201	GRM033R61E562KA12D
COUT	4.7uF 35V X7S	C0805	GRM21BC7YA475KE11
CDD	1uF 10V X5R	C0402	GRM155R61A105KE15D
CIO	1uF 10V X5R	C0402	GRM155R61A105KE15D
L_IN	6.8uH	3.2 x 2.5 x 1.2mm	DFE322512F-6R8M
RISET	24.9 kΩ	R0402	Use tighter than 1% tolerance
RC	0 Ω	R0201	Generic
R1, R2	1 kΩ	R0201	Generic
U1		WLCSP-35	ARC2C0608

*Note: * Value may need to be adjusted based on proximity of the input source to eliminate input voltage ringing.*

Component Selection

Users of the ARC2C0608 should adhere closely to the parts selected for the Application Demo Bill of Materials (BOM). Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact pSemi for guidance.

Layout Example

Below is an example of a compact 6 WLED string converter layout. Solution size is ~56 mm2.

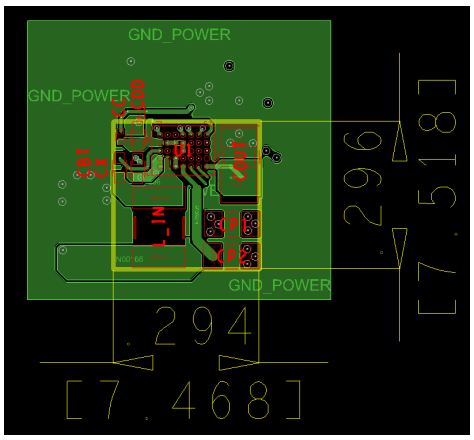

Figure 31. Layout Example

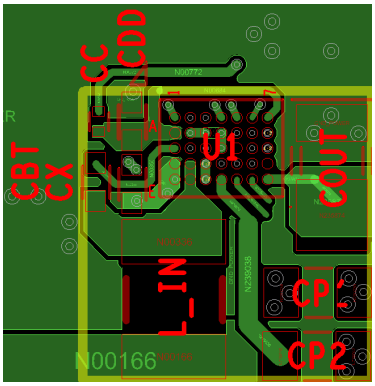

Figure 32. Top Layer

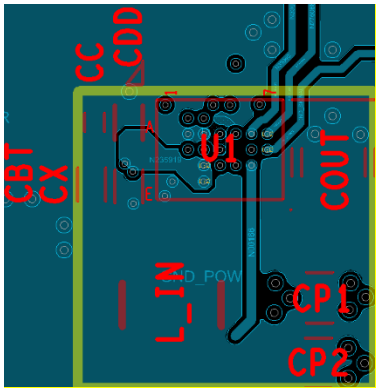

Figure 33. Layer 2

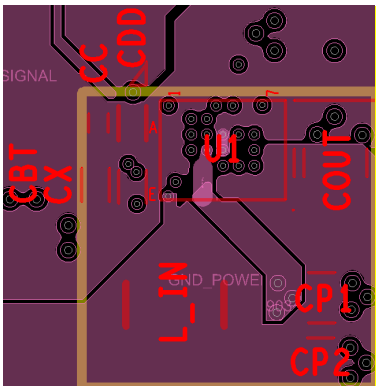

Figure 34. Layer 3

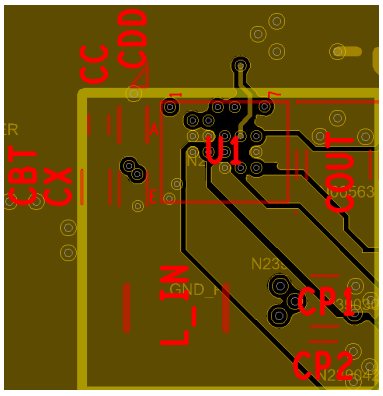

Figure 35. Bottom Layer

Mechanical Details

Device Dimensions

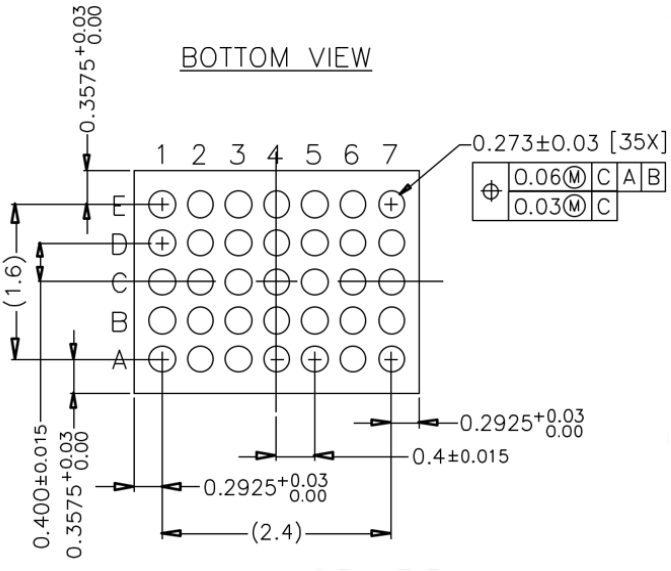

Figure 36. Bottom View and Dimensions

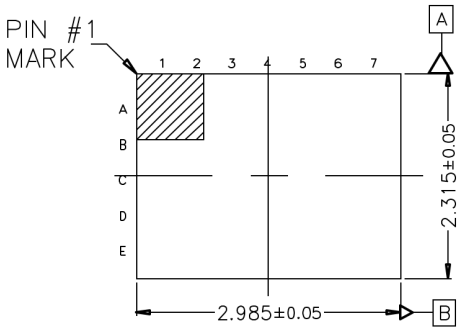

Figure 37. Top View and Dimensions

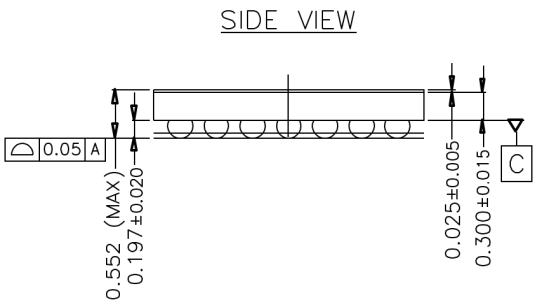

Figure 38. Side View and Dimensions

Guidelines for PCB Land Design

Recommended PCB Pad and Stencil Parameters

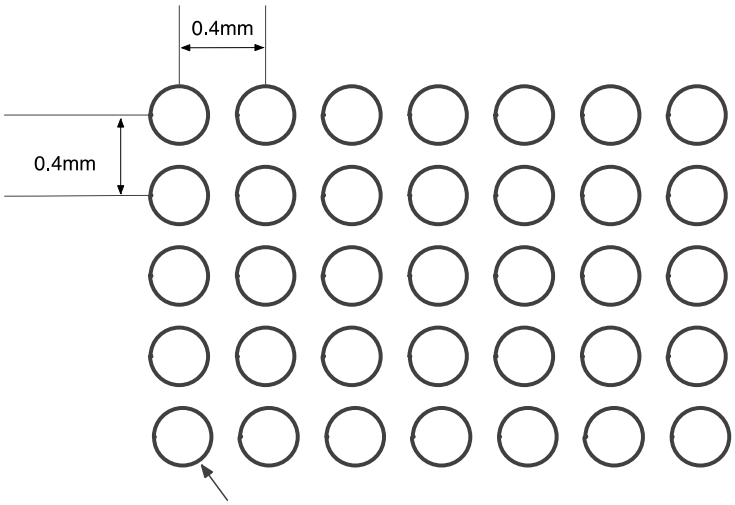

Figure 39. Bottom View and Dimensions

Ordering Information

TA	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM ORDER QUANTITY
-30....+85°C	WLCSP	ARC2C06081W-R	35	Large tape-and-reel	5000
		ARC2C06081W-V		Small tape-and-reel	250
		ARC2C06081W-G		Sample waffle tray	10

Tape & Reel Information

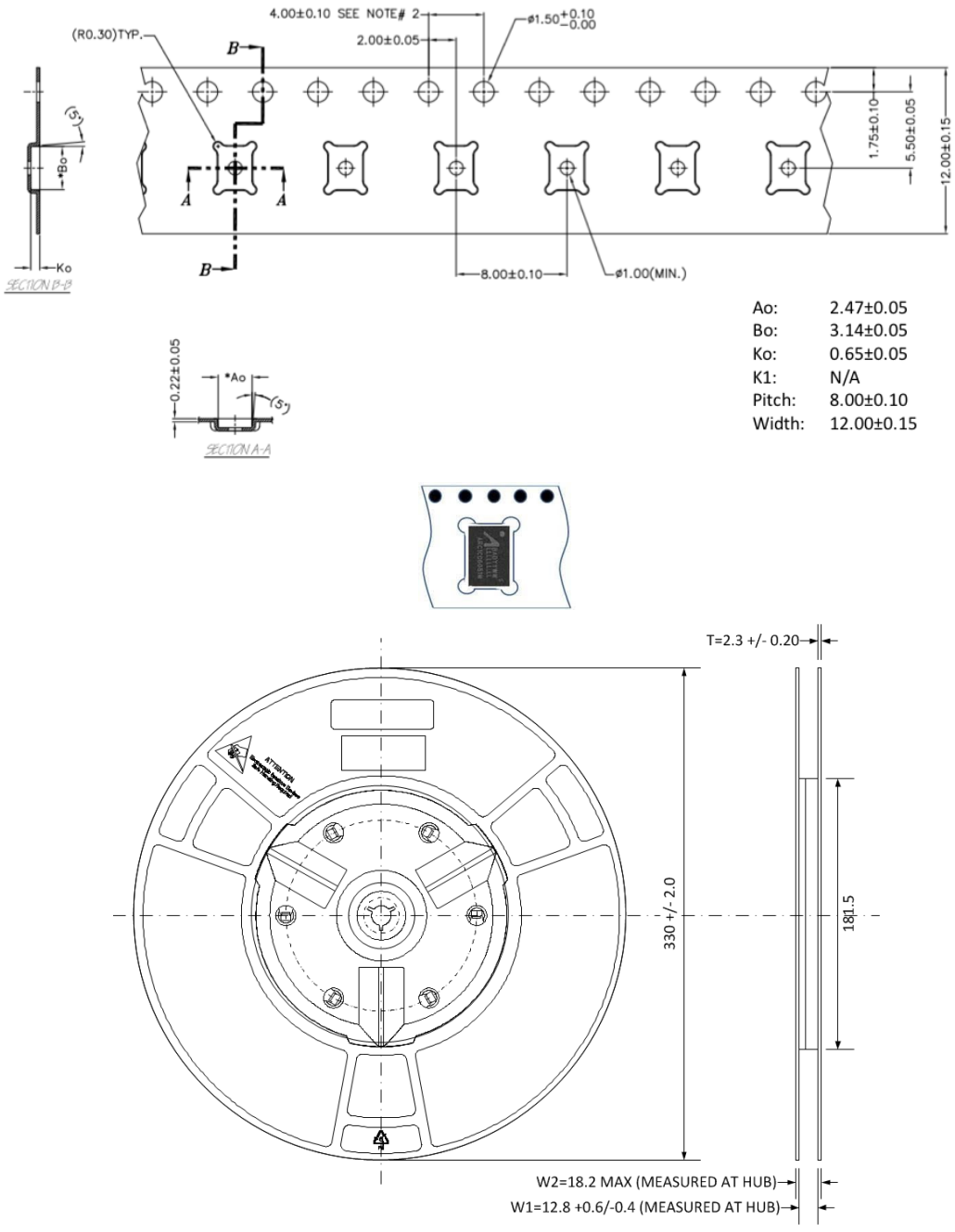

Figure 40. Tape and Reel Information

Notices

⚠ CAUTION

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might directly cause damage to the third party's life, body or property.

Aircraft equipment

Aerospace equipment

Undersea equipment

Power plant control equipment

Medical equipment

Transportation equipment (vehicles, trains, ships, etc.)

Traffic signal equipment

Disaster prevention / crime prevention equipment

Data-processing equipment

Application of similar complexity and/or reliability requirements to the applications listed in the above

⚠ NOTE

1. Please make sure that your product has been evaluated and confirmed against your specifications when our product is mounted to your product.
2. All the items and parameters in this approval sheet for product specification have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment agreed upon between you and us. You are requested not to use our product deviating from such agreement.
3. If you have any concerns about materials other than those listed in the RoHS directive, please contact us.

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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