

muRata

Bias-T Inductor Design Support Tool

Operation Manual

May 2020 Murata Manufacturing Co., Ltd.

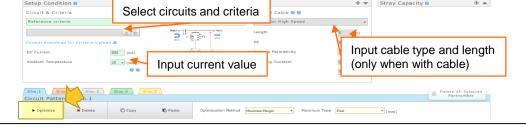
Tool Overview



Find optimal products combination for PoC bias-T inductors by simple operations.

Operations

- setting conditions (circuit, criteria, current, cable (In case selected "with cable "))
- pressing the Optimize button to discover



Result

- optimal products combination
- the graph display of S21 (IL), S11 (RL), S21/S11, Z
- Pass/Fail for standards that are to be cleared
- the smallest margin, total DCR/area of filters, largest height

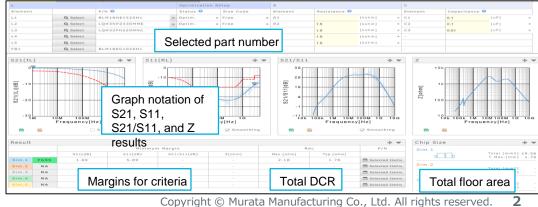


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- 6. Use Case 6 (Reduce parallel R)



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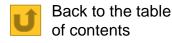
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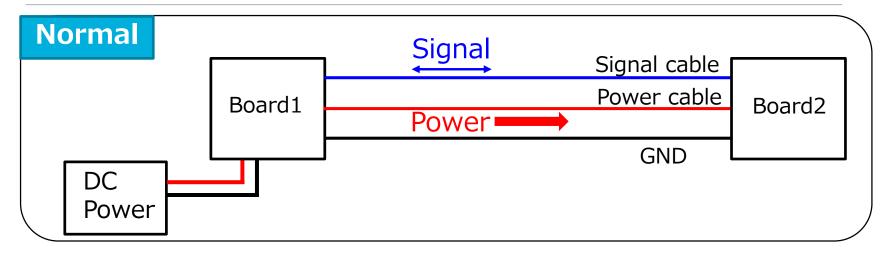
4, Tool Use Cases

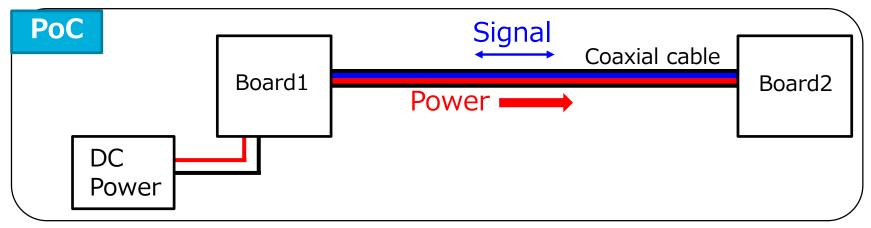
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1-1, What Is PoC



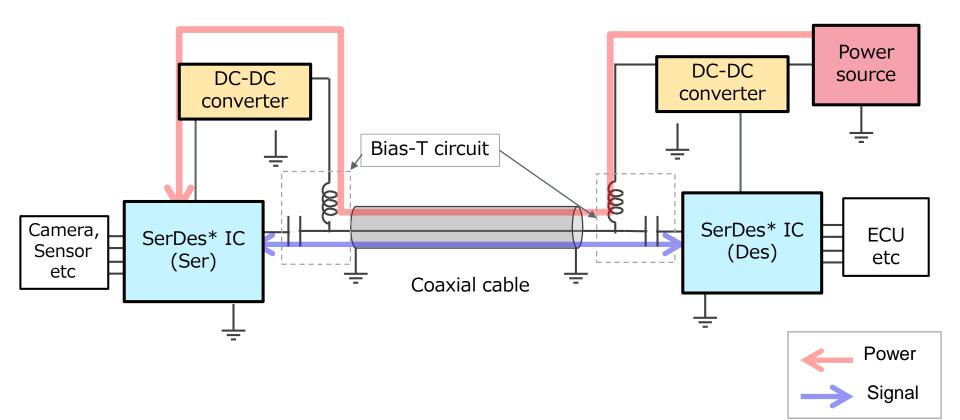




PoC (power over coaxial) is a technology that transmits both power and signal simultaneously through 1 coaxial cable. (This contributes to reduce the number of cables)

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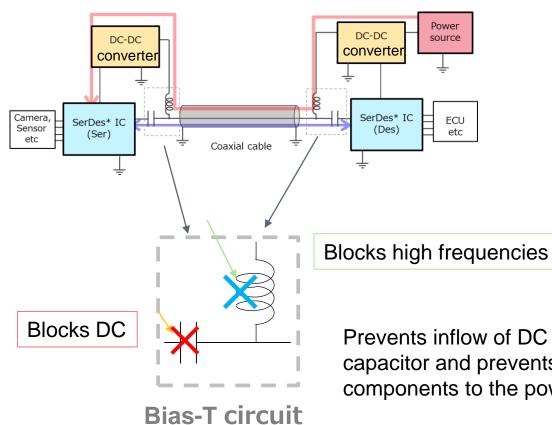
1-2, Typical Circuit Diagram of PoC Systems **muRata**



The high frequency signal and DC power are separated through the Bias-T circuit.

1-3, Roles of PoC System Bias-T Inductors



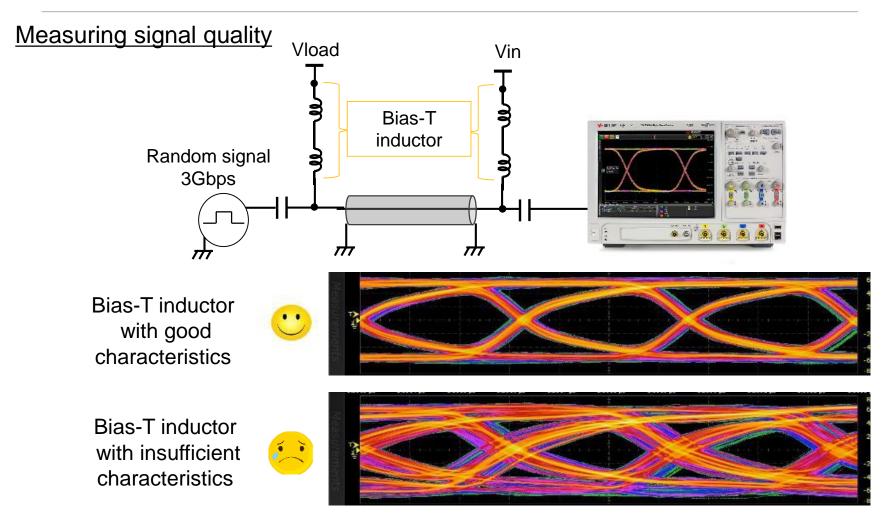


Prevents inflow of DC components to the IC with the capacitor and prevents inflow of high frequency components to the power line with the inductor.

It is particularly necessary to select a Bias-T inductor since it greatly affects transmission characteristics.

1-4, Effects Bias-T Inductor Characteristics Apply on Signal Quality

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It is required to select a Bias-T inductor that can ensure signal quality.



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2-1, Circuits That Can Be Simulated



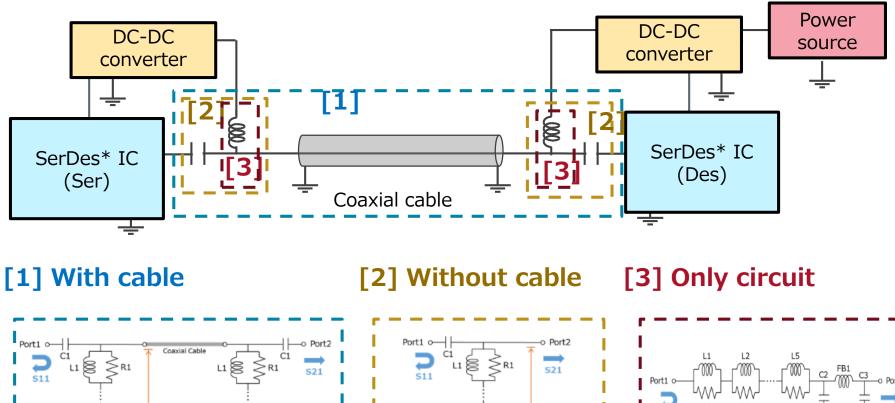
Simulation with 3 types of circuits available.

L5 🚫

FB1

15 8

FB1



L5 😂

FB1

Z

S11

S21





S21, S11, S21/S11 criteria values that must be cleared to ensure signal quality are set by each IC manufacturers or customers.

Automatically selects products combinations that clear these criteria.

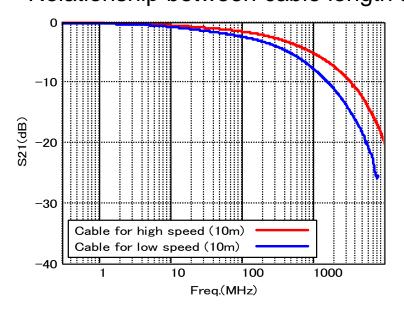
This tool can be selected from the following.

- Select the IC manufacturer recommended criteria
- Select the criteria set by MURATA
- Upload your criteria

2-3, Coaxial Cable

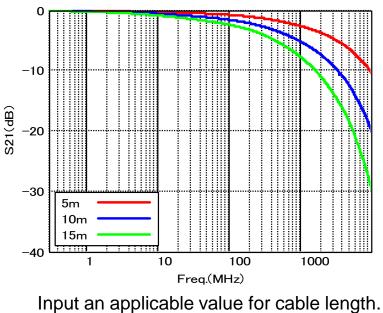


Loss varies by cable type and length. To run simulations on circuits with cables, settings considering cable characteristics must be applied.



Relationship between cable length and S-parameter

2 types of cables can be selected on this simulator.

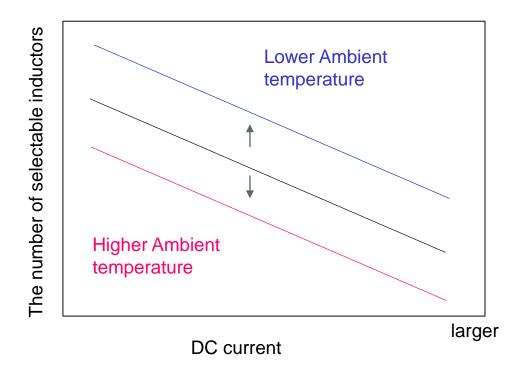


(Usually about 15 m or less)

2-4, Current, Temperature, and Size SettingsmuRata

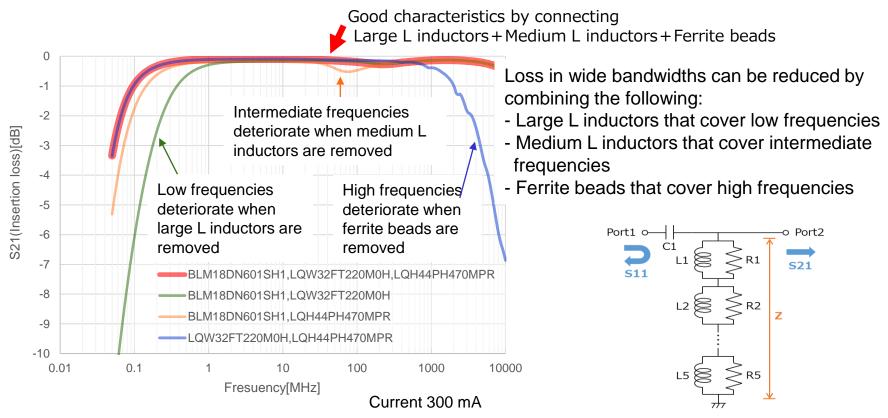
Inductors that match the conditions set in condition settings are provided.

Applying less options for ambient temperature conditions and current conditions provide more inductors that can be selected.



2-5, Serial Connection of Bias-T Inductors

In Bias-T circuits, to ensure signal quality by reducing loss in wide bandwidths ranging from low frequencies to high frequencies, **Multiple inductors must be used in series.**



Simulations with up to 5 parallelly connected inductors are available on this tool. Bias-T inductors are automatically selected.

2-6, How to Select Parallel Resistances

Anti-resonance will occur when several Bias-T inductors are connected serially. By adding a parallel resistance to each inductor, anti-resonance can be suppressed.

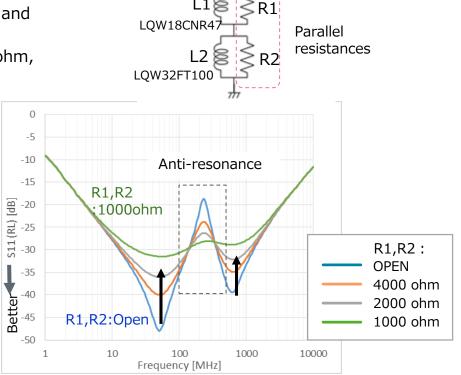
On the other hand, characteristics other than anti-resonance will deteriorate. By selecting a suitable resistance value, a filter characteristic that fulfills the target characteristic will be achieved.

The following are results when "L1: LQW18CNR47" and "L2: LQW32FT100" are used, and their parallel resistances R1 and R2 are Open, 1000 ohm, 2000 ohm, or 4000 ohm.

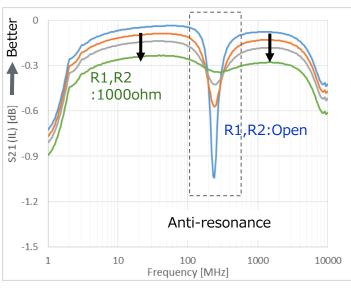
Better -0.3 R1,R2 :1000ohm 9.0- **S21(IL) [dB]** 6.0- 8.0-R1,R2:Open -1.2 Anti-resonance -1.5 1 10 100 1000 10000 Frequency [MHz]



S21



S11

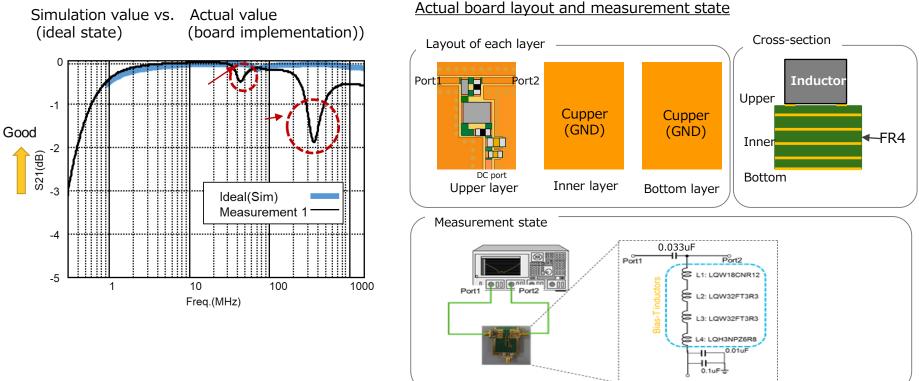




2-7, Effects of Board Stray Capacitance 1

A difference in characteristic results occurs between the simulation value (ideal state) and actual value (board implementation).

Anti-resonance is present more noticeably in the actual value.



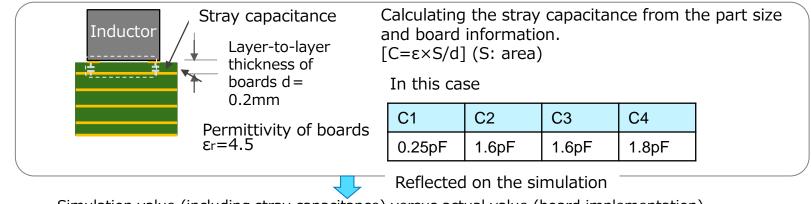
Actual board layout and measurement state

2-7, Effects of Board Stray Capacitance 1

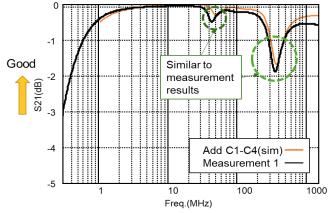


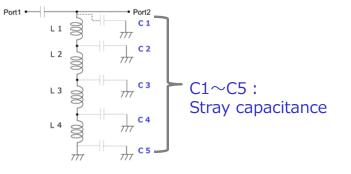
In the actual state, the stray capacitance that occurs between the inductor and inner layer of PCB is present on the characteristic.

If simulations are performed considering the stray capacitance, the calculated value becomes closer to the actual value.



Simulation value (including stray capacitance) versus actual value (board implementation)



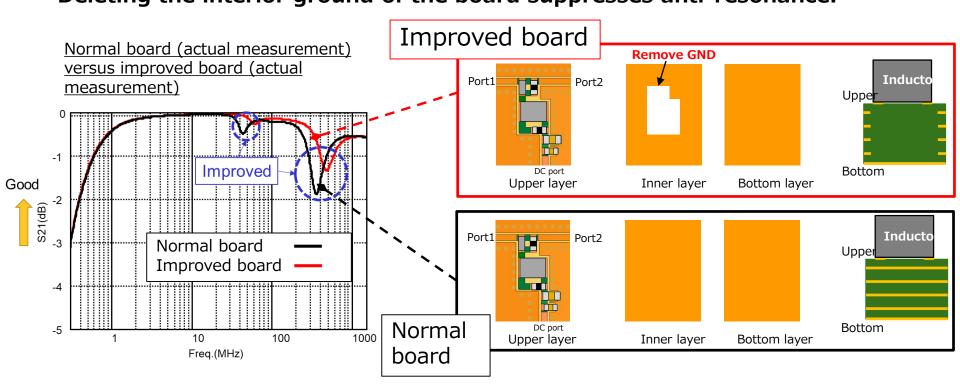


This simulator enables stray capacitance setting that allows calculation of results close to the actual characteristic.

2-7, Effects of Board Stray Capacitance 2

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The smaller stray capacitance is, anti-resonance becomes smaller as well. **Deleting the interior ground of the board suppresses anti-resonance.**



The stray capacitance value of the improved board is set as the default value on this simulator. Since the values change depending on the part size and board characteristics, simulations can be performed with the users freely changing the values.



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3-1, User Interface

im.4

NA

NA

-

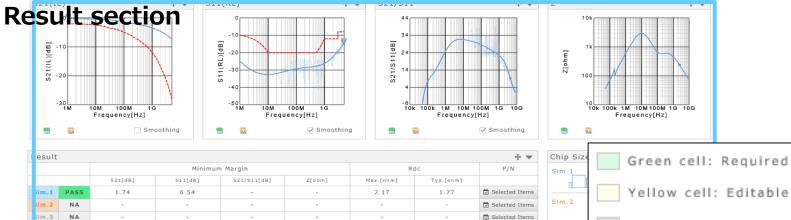
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-



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	on s	etting	a up	sec	tion		÷ •	Stray	Capacity		÷ 🔺	+
ircuit & Criteri	a				Coaxi	ial Cable 😢 😮						
Reference criteri	а				- Cable	e for High Speed	*					
		1 D Port	ti online t		Part2 Length	n	5 [m]					
ownload Sample D	Data 📥			u∰ Š®i"	521 Z0		51.5 [ohm]					
C Current	:	300 [mA]	LS 2 765 Z	u Sala	Relati	ve Permittivity	1.6					
mbient Temperatu	re .	25 🔺 [degC]			Dampi	ing Constant	0.56 [dB/m]					
		0 0	Ĵ-li=⊧ ↓	귀명	at		1000 [MHz]					
	emen	sim.4 s	tting a	and	selec	ted par	t num	nber	disp	olayi	te All Select Partnumber	sed
sim.1 sim	Sim.3	sim.4 s	tting a	and	Selec	ited par	't num mum Tsize Free	nber	disp	olayi	te All Select Partnumber	sed
ch ele	emen	its set	ng Paste	and Optimiz	ation Method Maxim	ited par Maxi	r t num mum Tsize Free	nber	disp	olayi	te All Select Partnumber	sed
ch ele	emen × Delete	its set	Opt	Optimiz	ation Method Maxim	R R	r t num mum Tsize Free Resistance @		* [mm]	Capacitan	ng .	sed
	Emen × Delete		Opt	imization Set	tup	R R	mum isize Free		• [mm]	olayi	ng .	sed
Cht Pete	× Delete		Opt Stat	imization Set tus ?	tup Size Code (mm/inc	R R Element	mum isize Free	[kohm]	C Element	Capacitan	ce O	ed SC
Cont Period	x Delete Q Select Q Select	P/N BLM18EG471SH1	Opti Stat	imization Set tus 🖓	tup Size Code (mm/inc Free	R R Element R1	Resistance 🕯	[kohm] [kohm]	C Element C1	Capacitan 0.1	ce O [uF]	sed SC
Chi Pein optimize	x Delete Q Select Q Select	P/N • BLM18EG471SH1 LQH44PH470MPR	Opt Stat X Opti X Opti	imization Set tus 🕜 im. 🍝 im. 🍝	tup Size Code (mm/inc Free Free	R R Element R1 R2	Resistance C	[kohm] [kohm] [kohm]	C Element C C C C C C C C C C C C C C C C C C C	Capacitan 0.1 0.1	ce • [uF] [uF]	sed
Cont Person Control Co	× Delete A Select A Select A Select	P/N • BLM18EG471SH1 LQH44PH470MPR	Opt Stat X Opti X Opti X Opti X Opti X Opti	imization Set tus ? im. ^ im. ^ im. ^	tup Size Code (mm/inc Free Free	R R Element R1 R2 R3	Resistance C 1.5 1.5	[kohm] [kohm] [kohm] [kohm]	 [mm] C Element C1 C2 C3 	Capacitan 0.1 0.1	ce • [uF] [uF]	sed



-

🛱 Selected Items

🛱 Selected Items

Sim.3

T Max.[mm]

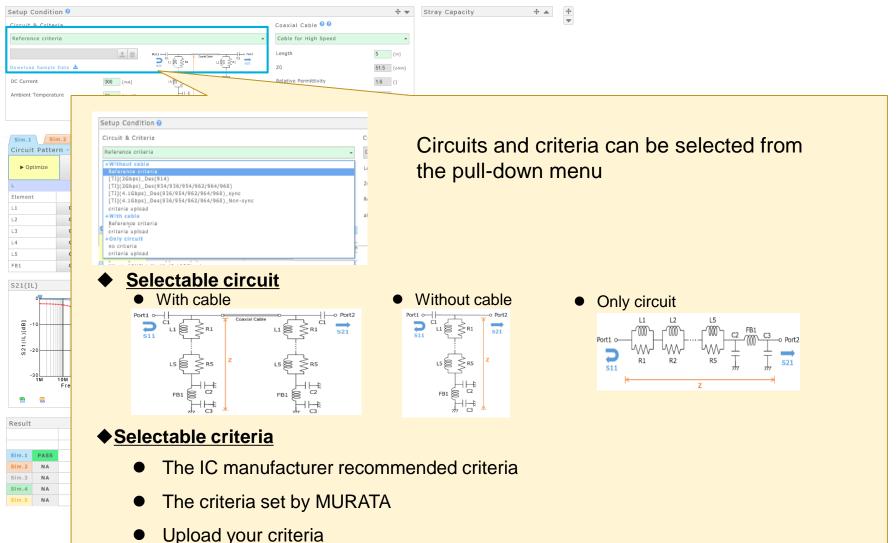
Gray cell: Uneditable

3-2, Details of each sections



Condition setting up section

Circuit and criteria

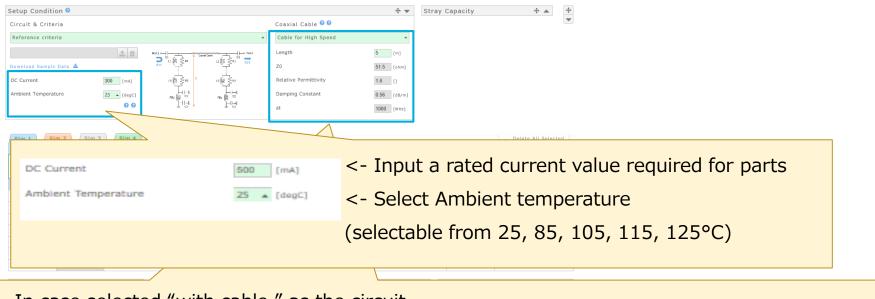


3-2, Details of each sections



Condition setting up section

Current and Ambient temperature, cable conditions



In case selected "with cable " as the circuit

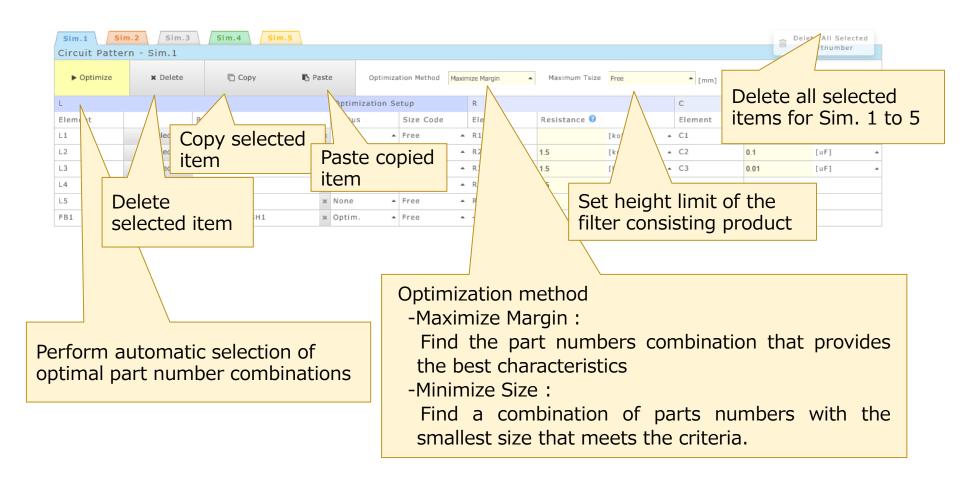
Cable for High Speed		< Select cable (High speed:Max20GHz, Low speed:Max8.5GHz)
Length	5 (m)	< Input cable length
zo	51.5 [ohm]	Cable factor (editing available if "Edit" is selected in cable selection)
Relative Permittivity	1.6 []	•Z0: Characteristic impedance
Damping Constant	0.56 [dB/m]	• Relative permittivity: Cable permittivity ϵ Z0
at	1000 (MHz)	Damping constant: Cable loss
		Damping constant

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3-2, Details of each sections



Each elements setting and selected part number displaying section INNOVATOR IN ELECTRONICS



3-2, Details of each sections

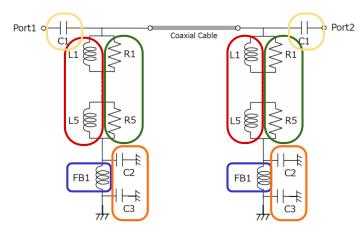


Each elements setting and selected part number displaying section INNOVATOR IN ELECTRONICS

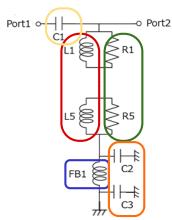
Sim.1 Sin Circuit Patter		Sim.4 Sim.	5							Û	Delete All Sele Partnumber	
► Optimize	🗙 Delete	Сору	🖪 Paste	Optimi	zation Method Ma	ximize Margin	 Maximum Tsiz 	e Free	^ [mm]			
L			C	Optimization :	Setup	R			с			
Element		P/N 🕜	5	Status	Size Code	Element	Resistance 🕝		Element	Capacitan	ce 🕜	
L1	Q Select	BLM18AG102SH1	≫ C	Optim.	Free	▲ R1		[kohm]	▲ C1	0.1	[uF]	
L2	Q Select	LQW32FT100M0H	» C	Optim.	Free	▲ R2	1.5	[kohm]	▲ C2	0.1	[uF]	
L3	Q Select	LQH3NPZ680MME	≫ C	Optim.	Free	▲ R3	1.5	[kohm]	▲ C3	0.01	[uF]	
L4	Q Select		⇒ N	lone	Free	▲ R4	1.5	[kohm]	A -			
L5	Q Select		≫ N	lone	Free	▲ R5	1.5	[kohm]	A -			
FB1	Q Select	BLM18KG102SH1	× C	Optim.	▲ Free	^ -			-			

- L1 L5 : Part number that consist of the Bias-T filter
- R1 R5 : Parallel resistance
- C1 : DC cut capacitor
- C2, C3 : Decoupling capacitor
- FB : Ferrite Beads as a noise filter

With cable



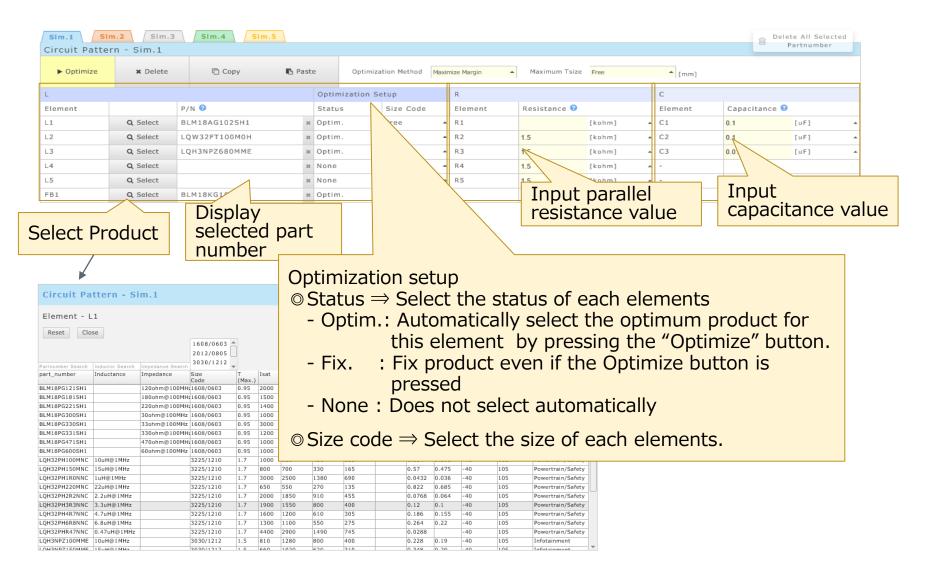
Without cable



3-2, Details of each sections



Each elements setting and selected part number displaying section INNOVATOR IN ELECTRONICS



3-2, Details of each sections Result section



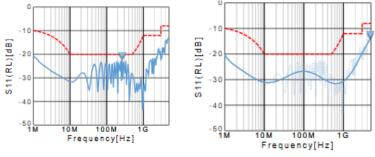
÷ • + -Ζ + -S21(IL) ÷ • S11(RL) S21/S11(IRR) RR)[dB] Ξ S21(IL)[dB] Display S21, S11, Z[ohm] Export graph S21/S11, Z graphs -20 Total DC resistance data as CSV -30 2M value of selected part 20M 2005 200 N 10M 100M 10 G v[Hz] Frequency[Hz] Frequency[Hz] number(Max and typ.) Smoothing Smoothing 顤 Chip Size Result + -Minimum Margin Sim.1 al [mm2] 19.56 IL[dB] IRR[dB] Z[ohm] Max.[ohm] Typ.[ohm] Total size and 💆 Sele Sim.1 PASS 1.78 2.48 1.98 10 im.2 Sim.3 NA 🗟 Sele maximum height of Sim.3 ΝA 🖾 Sele Minimum margin value against the 🗟 Selec NA selected part Selec NA criteria (Displaying markers in a graph) numbers Judgment Graph smoothing function (Pass/Fail) When "With cable" is selected, the influence for criteria

List of selected part numbers and links

Element	P / N		Link		
L1	BLM18AG10	ZSH1	Reference Spec	Product Detail	SimSurfing
L2	LQW32FT10	Like	to select	ed art nu	Imber
L3	LQH3NPZ68		ference s		
L4			oduct det	•	
L5				(enables	characteristic

Frequency[Hz]

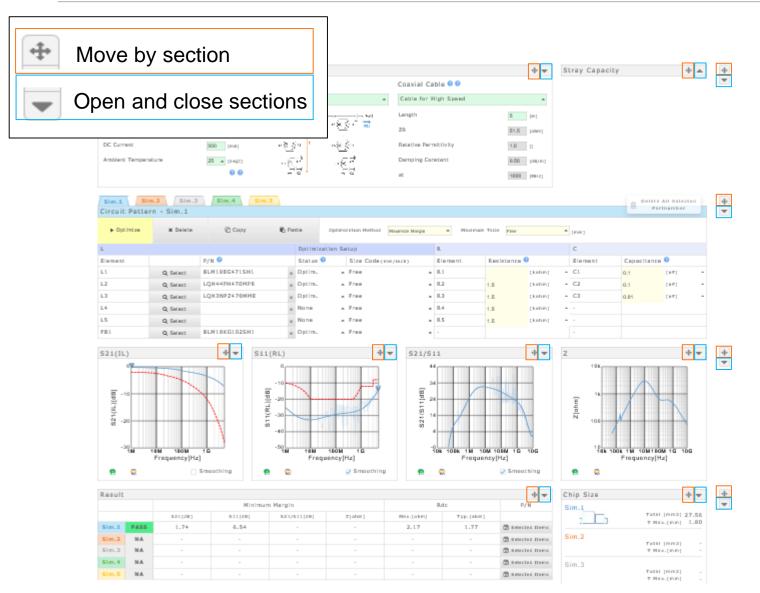
When "With cable" is selected, the influence of the reflection due to the cable is applied on the calculation result graph. The graph can be smoothed with the smoothing button.



3-2, Details of each sections



Other features





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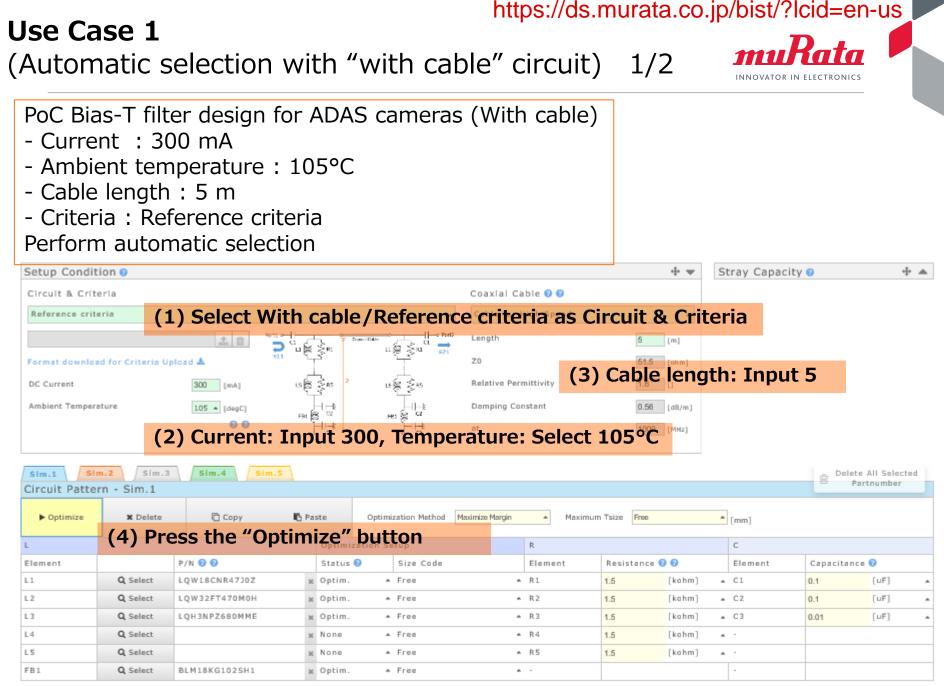
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- 6. Use Case 6 (Reduce parallel R)



Chip Size + -

si

Selected Items

(m.1	
	Total [mm2] 19.56
	T Max.[mm] 2.50

T Max.[mm] 2.50

Pass or Fail against selected criteria, minimum margin value, total DCR, and total area are displayed

Typ.[ohm]

2.47

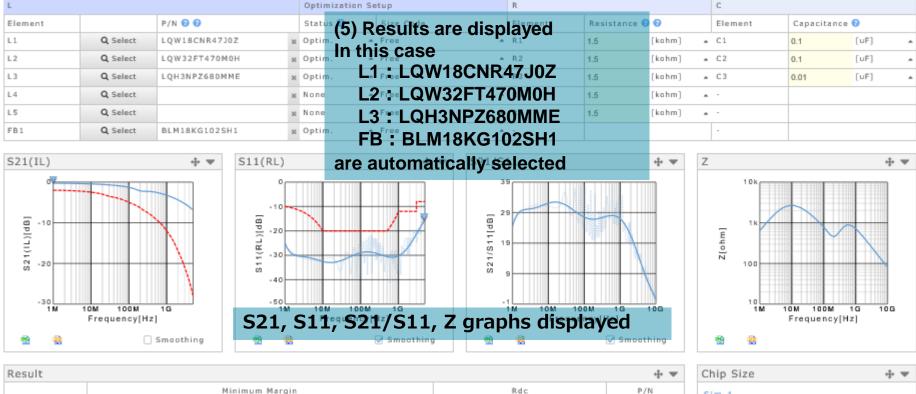
Max.[ohm]

2.93

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https://ds.murata.co.jp/bist/?lcid=en-us

(Automatic selection with "with cable" circuit) 2/2



Use Case 1

S21[dB]

1.73

Sim.1

PASS

S11[dB]

7.51

S21/S11[dB]

Z[ohm]

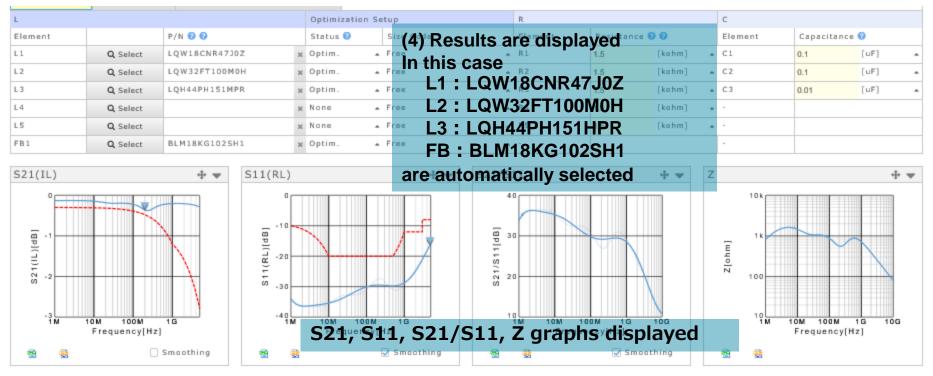
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Circuit Pattern - Sim.1 Poptimize X Delete Copy C Paste Optimization Method Maximize Margin A Maximum Tsize Free (mm)	en-us
 Current : 300 mA Ambient temperature : 85°C Criteria : Reference criteria Perform automatic selection Setup Condition • • • Stray Capacity • Circuit & Criteria (1) Select Without cable/Reference criteria as Circuit & Criteria	
Circuit & Criteria Reference criteria (1) Select Without cable/Reference criteria as Circuit & Criteria Format download for Criteria Upload & DC Current Ambient Temperature Sim.1 Sim.2 Sim.3 Sim.4 Sim.5 Circuit Pattern - Sim.1 Poptimize X Delete Copy Paste Optimization Method Meximum Tsize Pres Meximum Tsize	
Reference criteria (1) Select Without cable/Reference criteria as Circuit & Criteria Format download for Criteria Upload & Image: Select Sime and Select Select Sime and Select S	÷
(1) Select Without cable/Reference criteria as Circuit & Criteria Format download for Criteria Upload & DC Current Ambient Temperature S (degC) C) Current: Input 300, Temperature: Select 85°C Sim.1 Sim.2 Sim.3 Sim.4 Sim.5 Circuit Pattern - Sim.1 > Optimize X Delete Copy Paste Optimization Method Maximize Margin Maximum Tsize Free (mm)	
Format download for Criteris Upload ▲ Image: Constant for Criteris Upload ▲ I	
Format download for Criteris Upload A Z0 DC Current 300 [mA] Ambient Temperature 85 • [degC] #S • [degC] Barping Constant 0.56 [dB/m] 0.1 Sim.1 Sim.2 Sim.3 Sim.4 Sim.4 Sim.5 Optimization Method Maximize Margin Maximum Tsize Free (mm)	
DC Current Ambient Temperature BS (degC) C Current: Input 300, Temperature: Select 85°C Sim.1 Sim.2 Sim.3 Sim.4 Sim.5 Circuit Pattern - Sim.1 Poptimize X Delete Copy Paste Optimization Method Maximum Tsize Free (mm)	
Ambient Temperature B5 (degC) C1 Current: Input 300, Temperature: Select 85°C Sim.1 Sim.2 Sim.3 Sim.4 Sim.5 Circuit Pattern - Sim.1 Poptimize X Delete Copy Paste Optimization Method Maximum Tsize Free (mm)	
(2) Current: Input 300, Temperature: Select 85°C	
(2) Current: Input 300, Temperature: Select 85°C	
Sim.1 Sim.2 Sim.3 Sim.5 Circuit Pattern - Sim.1 Optimize X Delete Copy Paste Optimization Method Maximum Tsize Free (mm) 	
	elete All Selected Partnumber
(3) Press the "Optimize" button	
Element P/N 0 0 Status 0 Size Code Element Resistance 0 0 Element Capaci	ance 😗
L1 L1 LQW18CNR4730Z x Optim. • Free • R1 1.5 [kohm] • C1 0.1	[uF]
L2 Q Select LQW32FT100M0H * Optim. * Free * R2 1.5 [kohm] * C2 0.1	[uF]
L3 Q Select LQH44PH151MPR x Optim. Free A R3 1.5 [kohm] A C3 0.01	[uF]
L4 Q Select x None Free R4 1.5 [kohm] - L5 Q Select x None Free R5 1.5 [kohm] -	
FB1 Q Select BLM18KG102SH1 & Optim. • Free • • · · · · · · · · · · · · · · · · ·	

(Automatic selection with "without cable" circuit)

Use Case 2





Result							+ +	Chip Size	+ -
		Minimum	n Margin		R	d c	P/N	Sim.1	
	S21[dB]	S11[dB]	S21/S11[dB]	Z[ahm]	Max.[ohm]	Typ.[ohm]			Total [mm2] 26.56 T Max.[mm] 2.50
Sim.1 PASS	0.12	7.91	-	-	3.69	3.06	Selected Items		1 Max.[IIIII] 2.50

Pass or Fail against selected criteria, minimum margin value, total DCR, and total area are displayed

https://ds.murata.co.jp/bist/?lcid=en-us Use Case 3 (Change optimization method and Compare) 1/2INNOVATOR IN FLECTRONIC PoC Bias-T filter design for ADAS cameras (with cable) - Current :500 mA - Ambient temperature : 105°C - Cable length : 10 m - Criteria : Reference criteria Compare the results when "maximum margin" and "minimum size" are selected as the "Optimization method " Setup Condition 0 Stray Capacity + 🔺 + -Coaxial Cable 🛛 Circuit & Criteria (1) Select With cable/Reference criteria as Circuit & Criteria Reference criteria Download Sample Data 🛓 (3) Cable length: Input 10 DC Current 500 [mA] **Relative Permittivity** Ambient Temperature 85 🔺 [degC] (2) Current: Input 500, Temperature: Select 105°C Sim.3 Sim.4 Sim.1 Delete All Selected Partnumber Circuit Pattern - Sim.1 * (mm) ► Optimize × Delete Copy Paste Maximize Margin Maximum Tsize Free Blas-T Inductor Selection Tool Green cell: Required Yellow cell: Editable Grav cell: Unedi Element Error *A message is displayed if the Setup Condition 🛛 **Over Rated Current** current value before input is Circuit Pattern A: Circuit & Criteria L3 BLM18AG102SH1, LQH3NPZ680MME smaller than 500 mA. Reference criteria 1.4 1.5 please choose action: Select the "Delete items that do FB1 Delete items that do not meet the condition Download Sample Data 📥 not meet the condition" option Restore the conditions DC Current 500 [mA] and then click OK. Ambient Temperature 25 🔺 [degC]

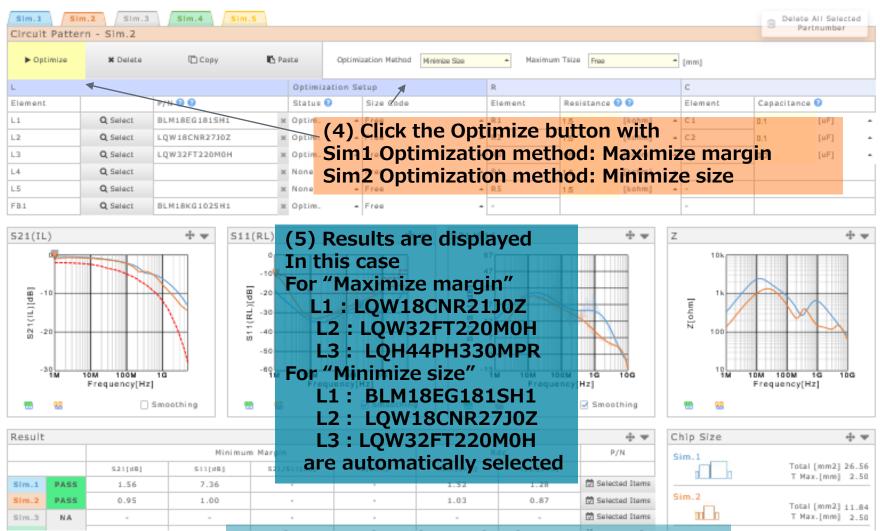
at

1000 [MHz]

Use Case 3 (Change optimization method and Compare) 2/2



INNOVATOR IN ELECTRONICS



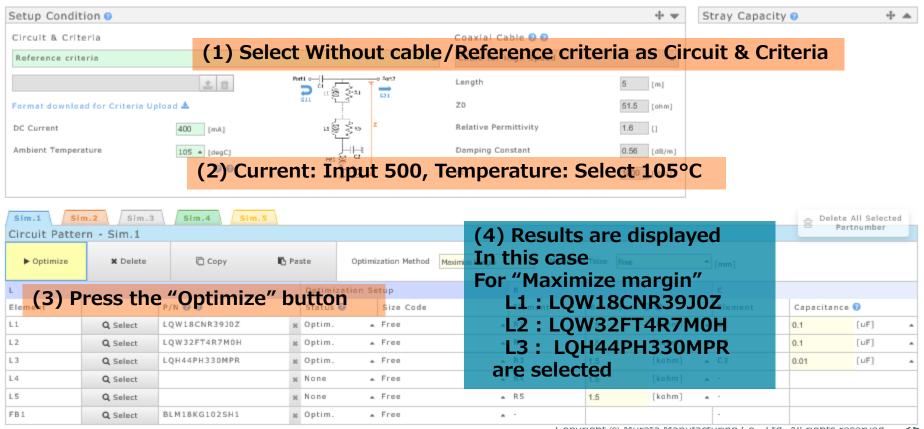
Graphs, margin values, size images, total DCR values, and total size values can be compared

Use Case 4 (Reselect L from inductor list) 1/3



- PoC Bias-T filter design for ADAS cameras (without cable)
- Current : 400mA
- Ambient temperature :105°C
- Criteria : Reference Criteria

Reselect the L1 element after automatic selection and compare.



Use Case 4 (Reselect L from inductor list) 2/3

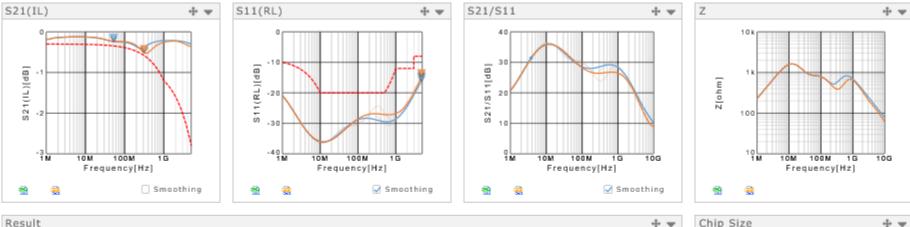


Sim.3 Sim.4 Sim.1 Sim.2 Delete All Selected Partnumber Circuit Pattern - Sim.1 Copy * (mm) Paste Maximum Tsize Free Optimize X Delete Optimization Method Maximize Margin . (5) Copy product names selected in "Sim1" C L P/N 🔞 Element Capacitance 🔞 Element L1 Q Select BLM18HE102SH1 Free R1 [kohm] C1 0.1 [uF] Optim. L2 Q Select LQW32FT220M0H Optim. Free R2 1.5 [kohm] C2 0.1 [uF] 58 L3 Q Select LQH3NPZ220MME R3 1.5 [kohm] C3 [uF] Optim. Free 0.01 L4 Q Select Free R4 1.5 [kohm] . -None L5 Q Select R5 1.5 [kohm] × None Free ÷ -FB1 Q Select BLM18KG102SH1 x Optim. Free ÷ -

					Αιια	ch the	5111	тра	ILII	un	IDC		Jyv	unu	NIII	ig i	r as	sie		
otimize	X Delete	Сору	R Feste	.e 0	ptimization	Method Minimi	ze Size		Maximum	Tsize	Free			* [1	mm]					
				Optimizat	tion Setup	Circuit Pa	ittern - S	im.2												
t		P/N 😧		Status	Siz	Element - I	_3													
	Q Select	BLM18HE102SH1	×	Optim.	▲ Fre	Reset Clo	ose		1608/0603					DC Curren	500	Imál				Infotainment
	Q Select	(8) Click	"Selec	ct" of	- Fre	C Partnumber Search	10		2012/0805		-				_	[degC]	1			Powertrain/
	Q Select	QH3NPZ220MME		Optim.	+ Fre	part number	Inductarie S) Se	lect	an (Max.)	Isit	(BSdegC)		(temp)(115degC)	Itemp (125degC	Rdc (Max.)	Rdc (Typ.)	Operating Temp.(Min)	Operating Temp.(Max)	Application
	Q Select		×	None	▲ Fre	BLM18PG300SH1 BLM18PG330SH1		30ohm@100MHz 33ohm@100MHz	z 1608/0603 z 1608/0603	0.95	1000 3000	1000 3000	1000 2000		1000	0.05	0.02	-55 -55	125 125	Powertrain/S Powertrain/S
	Q Select		×	None	+ Fre	BLM18PG331SH1 BLM18PG471SH1		330ohm@100MH 470ohm@100MH	H:1608/0603	0.95	1200	1200 1000	1100 1000	1000	1000 1000	0.15	0.08	-55 -55	125 125	Powertrain/S Powertrain/S
	Q Select	B 18KG102SH1	×	Optim.	▲ Fre			60ohm@100MHz	3225/1210	1.7	3000	2500	1000	690	1000	0.1	0.04	-55 -40 -40	125	Powertrain/S Powertrain/S
						LQH32PH2R2NNC LQH32PH3R3NNC LQH32PH4R7NNC	3.3uH@1MHz		3335/1310	1.7		1200	610	9 J0		0.186	0.064	-40	105 105 105	Powertrain/S Powertrain/S Powertrain/S
						LQH32PH6R8NNC	-		322 R 210	M 1	81	+ D	152	2SH	1	0.264	0.22	-40	105	Powertrain/S
						LQH32PHR47NNC			3223/1210	1.7	4400	2900	1490	745	-	0.0288		-40	105	Powertrain/!
					_	LQH3NPZ100MME LOH3NPZ150MME	10uH@1MHz 15uH@1MHz		3030/1212 3030/1212	1.5	810	1280	620	310		0.228	0.19	-40	105	Infotainmen
						LQH3NPZ1R0MME	1uH@1MHz		3030/1212	1.5		3000	1600	800		0.03	0.025	-40	105	Infotainmen
						LQH3NPZ220MME	22uH@1MHz		3030/1212	1.5	570	860	540	270		0.48	0.4	-40	105	Infotainmen
						LQH3NPZ1R0MME	1uH@1MHz 22uH@1MHz		3030/1212	1.5	2350 570	3000	1600	800		0.03		-40		105

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Use Case 4 (Reselect L from inductor list) 3/3



Result								÷ +	Chip Size	÷ •
			Minimun	n Margin		R	d c	P/N	Sim.1	
		S21[dB]	S11[dB]	S21/S11[dB]	Z [a h m]	Max.[ohm]	Typ.[ohm]			Total [mm2] 26.56 T Max.[mm] 2.50
Sim.1	PASS	0.11	7.75	-	-	1.31	1.09	Selected Items		1 Max.[IIIII] 2.50
Sim.2	PASS	0.07	6.31	-	-	1.53	1.26	Selected Items	Sim.2	Total [mm2] 26.56
Sim.3	NA	-	-	-	-	-	-	Selected Items		T Max.[mm] 2.50
Sim.4	NA	-	-	-	-	-	-	Selected Items	Sím.3	
Sim.5	NA	-	-	-	-	-	-	Selected Items		Total [mm2] - T Max.[mm] -

(10) Results are displayed Comparison of results when LQW18CNR39J0Z or BLM18HE152SH1 is used for L1

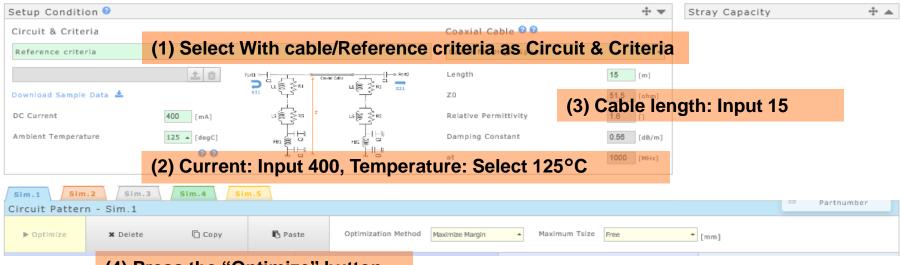
Use Case 5

(Relax the set up condition after the result become "Fail") 1/3

PoC Bias-T filter design for ADAS cameras (With cable)

- Current : 400 mA
- Ambient temperature : 125°C
- Cable length : 15 m
- Criteria : Reference criteria

Relax the set up condition after the result become "Fail"



(4) Press the "Optimize" button

Result		🕂 🔻 Chip Size	÷ •
		(5)Result become "Fail" Rdc P/N Cim 1	
	\$21[d8	In this case, since the temperature condition is 125 ° C and the	Total [mm2] 5.12
Sim.1 FAIL	0.70	cable length is 15 m, the condition is severe, so there is no combination that passes the criteria.	T Max.[mm] 0.95

Use Case 5

Sim.1

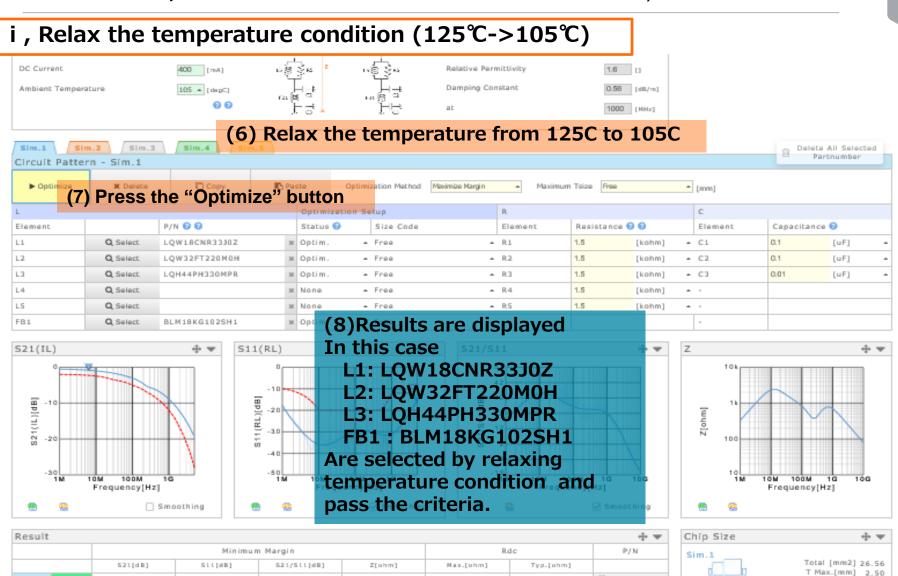
PASS

1.44

7.42

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(Relax the set up condition after the result become "Fail") 2/3



1.62

1.37

2 Selected Items

Use Case 5

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(Relax the set up condition after the result become "Fail") 3/3

ii , Relax the temperature condition (125 $^{\circ}$ ->105 $^{\circ}$)+add element in series

DC Current Ambient Temper	rature	400 [mA]		-	Relative Pe Damping C		1.6 0.56 /					
ircuit Patte	im.2 Sim.3	€ €	•	e is no ria just	comb	inatio	n that p	ass		- Dele	ate All Select Partnumber	ted
▶ Optimize	* Detete 8) Press	the "Op	timize" b	Optimization Method	Minimiza Siza	• Maxim	um Tsize Ree		• [mm]			
ement	P	/N 0 0	Status 📦	Size Code		Element	Resistance 🔞	0	Element	Capacitar	100 🕤	
	Q Select B	LM18HE152SH1	× Optim.	+ Free		- R1	1.5 [kohm]	- C1	0.1	[uF]	
	Q Select	QW32FT100M0H	× Optim.	+ Free		- R2	1.5	kohm]	• C2	0.1	[uF]	
	Q Select	QM21PH2R2NGC	× Optim.	- Free		+ R3	1.5	kohm]	• C3	0.01	[uF]	
	Q Select	QW32FT100M0H	# Optim.	- (7)5	elect	"Ontir	n." as L	4°4° ct	atus			
	Q Select		* None									
1	Q Select B	LM18KG102SH1	× Optim.	- Free	series	eieme	ents nu	mpe	r becc	ome 4	pcs)	
21(IL)		⊕ ▼ S1	1(RL)	+	▼ 521/5	511		÷ 👻 🔅	z		4	• •
0			0			50		1	10k			
S21(IL)[dB]	10M 100M 10 Frequency[Hz]			100M 1G ency[Hz]	11	In this L1: E L2: L	sults are case 3LM18H QW32I QM21F	IE15 FT10	52SH1 00M0H		14 10 y[Hz]	G
	Frequency[Hz]	anoothing	BD -20 -30 -40 -50 M 10M		S21(811[d	In this L1: E L2: L L3: L L4 :	case 3LM18H QW32I QM21F LQW32	IE15 T10 PH2F 2FT1	2SH1 00M0H R2NGC .00M0	16M 188M Frequence	(HZ]	_
BPI(1);22 -2 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3	Frequency[Hz]	a noothing	B) -20 -20 -30 -50 -50 -50 Frequ	ency[Hz]	52118111d	In this L1: E L2: L L3: L L4 : Are se	Case 3LM18H QW32I QM21F LQW32 lected l	1E15 FT10 PH2F 2FT1 Dy re	52SH1 00M0H R2NGC .00M0 elaxing	Tom 100M Frequency	(HZ]	G
-3 -3 -3	Frequency[Hz]	a noothing	BD -20 -30 -40 -50 M 10M	ency[Hz]	52118111d	In this L1: E L2: L L3: L L4 : Are se	case 3LM18H QW32I QM21F LQW32	1E15 FT10 PH2F 2FT1 Dy re	52SH1 00M0H R2NGC .00M0 elaxing	Tom 100M Frequency	y[Hz] 4 1tal (mm2] 1	8.56
-3 -3 -3	Frequency[Hz]Sn	a Minimu	m Margin	ency[Hz]	Mas-[0102]	In this L1: E L2: L L3: L L4 : Are se tempe	Case BLM18H QW32I QM21F LQW32 lected l rature	HE15 FT10 PH2F 2FT1 Dy recond	52SH1 00M0H R2NGC .00M0 elaxing	Tom 100M Frequency	y[Hz] 4 1tal (mm2] 1	• •
-3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -3 -	Frequency[Hz]Sn	C Minimu StileD	m Margin	ency[Hz]	Mas-[0102]	In this L1: E L2: L L3: L L4 : Are se tempe	Case 3LM18H QW32I QM21F LQW32 lected l	HE15 FT10 PH2F 2FT1 Dy recond	52SH1 00M0H R2NGC .00M0 elaxing	Tom 100M Frequency	y[Hz] 4 1tal (mm2] 1	8.56

Use Case 6 (Reduce parallel R) 1/2



- PoC Bias-T filter design for ADAS cameras (Without cable)
- Current : 400 mA
- Ambient temperature : 105°C
- Criteria : Reference criteria Reduce parallel R

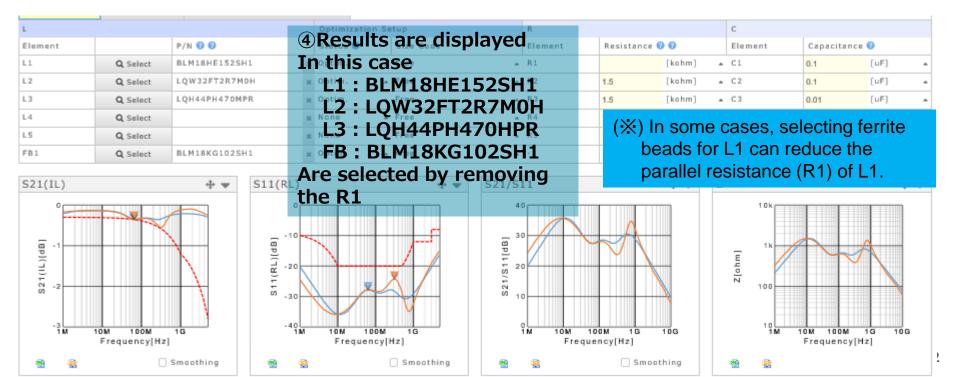
Setup Conditi	ion 🛛						+ +	Stray Capac	ity 📀	+
Circuit & Crite Reference crite	eria (1	.) Select Wi	ithout cable	/Referenc	e criteria a	as Circ	uit & O	Criteria		
Reference crite			Porti c	- 2-12			_			
		1	De la constante da la constant	Leng	jth	5	[m]			
format download	d for Criteria U	pload 📥		Z0		51	5 [ohm]			
DC Current		400 [mA.]	u 🗐 🕺 vo	z Relat	tive Permittivity	1.6] []			
Ambient Temperat	sture	105 • [degC]		Dam	ping Constant	0.6	6 [dB/m]			
		(2) Curre	ent: Input 4	00 Tomno	ratura: Sa	loct 1	1500			
		(2) curre	ant. Input 4	oo, iempe	lature. Se	ICCL I				
Sim.1 Sim	n.2 Sim.3	1 Sim.4 Sim.	5						o Del	lete All Selecte
				on					Del	lete All Selecto Partnumber
Circuit Patte	(3) Pre	ss the "Opt	imize" butt						E De	
			imize" butt	mization Method Maximize	Margin 🔺 Maxim	um Tsize Fre	2	• (mm)	Del	
Circuit Patte	(3) Pre	ss the "Opt	imize" butto		r na ga r	num Tsize Fre	2	* (mm)	Del	
Circuit Patte	(3) Pre	ss the "Opt	imize" butto	esults are d	r na ga r	num Tsize Free Resistance			Capacita	Partnumber
Circuit Patte	(3) Pre	ss the "Opt	Timize" butto Paste Optim Op (4)Re Sta In this	sults are d				с		Partnumber
Circuit Patte	(3) ^{SI} Pres * Delete	ss the "Opt © Copy	Paste Optim Paste Optim op (4)Re staIn this x Optim. L1	sults are d scase LQW18C	lisplayed Element NR39J0Z	Resistant	:e 🛛 🖸	C Element	Capacita	Partnumber
lement 1	(3) Pres * Delete	SS the "Opt Copy P/N © © LQW18CNR39J0Z	Cimize" butto Paste Optim op(4)Re StaTn this x Optim. L1 x Optim. L2	esults are d is case : LQW18CI : LQW32F1	lisplayed Element NR39J0Z F2R7M0H	Resistant	:a 🕢 🕑 [kahm]	C Element • C1	Capacita 0.1	Partnumber
Circuit Patte	(3) Pres * Delete Q Select Q Select	ss the "Opt © Copy P/N © © LQW18CNR3930Z LQW32FT2R7MDH	Cimize" butto Paste Optim op(4)Re StaTn this x Optim. L1 x Optim. L2	sults are d scase LQW18C	lisplayed Element NR39J0Z F2R7M0H	Resistant 1.5 1.5	2 😧 😧 [kahm] [kahm]	C Element C1 C2	Capacita 0.1 0.1	Partnumber
Circuit Patte	(3) Pres × Delete Q Select Q Select Q Select	ss the "Opt © Copy P/N © © LQW18CNR3930Z LQW32FT2R7MDH	cimize" butto Paste Optim op(4)Re StaIn this x Optim. L1 x Optim. L2 x None L3	esults are d is case : LQW18CI : LQW32F1	lisplayed Element NR39J0Z F2R7M0H I330HPR	Resistant 1.5 1.5 1.5	e 😧 😧 [kahm] [kahm]	C Element • C1 • C2 • C3	Capacita 0.1 0.1	Partnumber

Use Case 6 (Reduce parallel R) 2/2



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Sim.1 Sim Circuit Patter		Select Sim2							ji De	lete All Selected Partnumber	
► Optimize	X Delete	🔁 Сору 🖪 Р	aste	Optimization Method	Maximize Margin 🔺	Maximum Tsize	Free	• [mm]			
L (8)	Press t	ne "Optimize	" bu	Size Code			laximize	e margin' method	Capacita	ance 😯	
L1	Q Select		e Optim.	.▲ Free	# R1	1.5	[kahm]	* C1	0.1	[uF]	-
L 2	Q Select	1	e Optim.	.▲ Free	. R2	1.5	[kahm]	▲ C2	0.1	[uF]	*
L 3	Q Select	1	e Optim.	.▲ Free	. R3	1.5	[kohm]	• C3	0.01	[uF]	*
L.4	Q Select	1	e None	. Free	(6)	Delete	the value	e of R1			
L 5	Q Select	1	e None	.▲ Free	a R5	1.5	[kahm]	A 1			
FB1	Q Select	1	e Optim.	🔺 Free	A 1			-			





End