W-LAN+Bluetooth® Combo Module Data Sheet

Infineon CYW4373 Chipset
for 802.11a/b/g/n/ac + Bluetooth® 5.2

Design Name: Type2BC
Tentative P/N : LBEE5PK2BC-771
Sample P/N : LBEE5PK2BC-SMP

This Datasheet is preliminary version, and subject
to change without notice
## Revision History

<table>
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<tr>
<th>Revision Code</th>
<th>Date</th>
<th>Description</th>
<th>Comments</th>
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<td>-</td>
<td>July 17th 2020</td>
<td>First Issue</td>
<td></td>
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<td>A</td>
<td>Apr 30th 2021</td>
<td>- Scope&lt;br&gt;- Part Number&lt;br&gt;- Dimensions, Marking and Terminal Configurations&lt;br&gt;- DC / RF Characteristics&lt;br&gt;- Tape and Reel Packing</td>
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<td>B</td>
<td>Dec 29th 2021</td>
<td>- DC / RF Characteristics&lt;br&gt;- Module height&lt;br&gt;- Bandgap reference resistor to 4.75K ohm +/-1%</td>
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<td>C</td>
<td>Feb 16th 2022</td>
<td>- Scope BT 5.2&lt;br&gt;- Bluetooth® QDID</td>
<td>Update</td>
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<td>D</td>
<td>May 5th 2022</td>
<td>- terminal configuration&lt;br&gt;- DC / RF Characteristics</td>
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<td>E</td>
<td>June 14th 2022</td>
<td>- Scope IC P/N</td>
<td>Update</td>
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Preliminary
< Specification may be changed by Murata without notice >
Murata(China) Investment Co., Ltd.
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⚠️Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.
1. Scope
This specification is applied to the IEEE802.11a/b/g/n/ac W-LAN + Bluetooth® 5.2 combo module.

- Host Interface
  - WLAN : SDIO or USB(shared)
  - BT/BLE : UART or USB(shared)
- IC P/N : Infineon / CYW4373
- Reference Clock : Reference clock embedded
- Weight : 0.2g
- RoHS : This component can meet with RoHS compliance.
- MSL* : Level 3
  *This product is moisture sensitive. Please check the detail in 15.1 Storage Condition section.

2. Part Number

<table>
<thead>
<tr>
<th>Ordering Part Number</th>
<th>Description</th>
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<td>LBEE5PK2BC-EVB</td>
<td>In case of EVB order</td>
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<td>LBEE5PK2BC-SMP</td>
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<tr>
<td>LBEE5PK2BC-771</td>
<td>Mass Produced Product</td>
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*Type2BC* is design name of this module. Design name may be used in certification test report.

3. Block Diagram
4. **Certification Information**

4.1. **Radio Certification**

**USA/Canada**
- FCC ID: T.B.D.
- IC: T.B.D
- *Please follow installation manual of Appendix*

**Europe**
- T.B.D.

4.2. **Bluetooth® Qualification**
- QDID: 173411
5. Dimensions, Marking and Terminal Configurations

Marking | Meaning
---|---
A | Pin 1 Marking
B | Murata Logo
C | Module Type
D | Inspection Number
E | 2D Code (Internal use)

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<th>Dimension (unit: mm)</th>
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<td>a4</td>
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<tr>
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Structure

Shield Filter Matching SW CYW4373 Resin Mold

DIPLEX PWB Substrate

Preliminary

< Specification may be changed by Murata without notice >
Murata(China) Investment Co., Ltd.
<TOP View>

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<td>BT_UART_RXD</td>
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<td>WL_HOST_WAKE</td>
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<td>Type</td>
<td>Connection to IC Terminal</td>
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<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SR_VLX</td>
<td>PO</td>
<td>SR_VLX</td>
<td>CBUCK switching regulator output. Refer to Reference circuit for details of the inductor and capacitor required in this output.</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>VBAT</td>
<td>PI</td>
<td>SR_VDDBAT5V/LOD_VD/DBAT5V</td>
<td>Supply to internal Power source of VBAT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>WL_REG_EN</td>
<td>I</td>
<td>WL_REG_ON</td>
<td>Used by PMU to power-up or power down the internal CYW8x373 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>LPO_IN</td>
<td>I</td>
<td>LPO_IN</td>
<td>External Sleep clock input(32.768kHz)</td>
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<td>6</td>
<td>BT_PCM_IN</td>
<td>I</td>
<td>BT_PCM_IN</td>
<td>PCM data input.</td>
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<td></td>
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<td>7</td>
<td>BT_PCM_CLK</td>
<td>I/O</td>
<td>BT_PCM_CLK</td>
<td>PCM clock; can be master(output) or slave(input).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>BT_PCM_SYNC</td>
<td>I/O</td>
<td>BT_PCM_SYNC</td>
<td>PCM sync; can be master(output) or slave(input).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>BT_PCM_OUT</td>
<td>O</td>
<td>BT_PCM_OUT</td>
<td>PCM data output</td>
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</tr>
<tr>
<td>10</td>
<td>BT_UART_TXD</td>
<td>O</td>
<td>BT_UART_TXD</td>
<td>UART serial output. Serial data output for the HCI UART interface.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>BT_UART_CTS_N</td>
<td>I</td>
<td>BT_UART_CTS_N</td>
<td>UART clear – to send. Active - low clear – to - send signal for the HCI UART interface.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>BT_UART_RXD</td>
<td>I</td>
<td>BT_UART_RXD</td>
<td>UART serial input. Serial data input for the HCI UART interface.</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>13</td>
<td>BT_UART_RTS_N</td>
<td>O</td>
<td>BT_UART_RTS_N</td>
<td>UART request – to send. Active - low request - to-send signal for the HCI UART interface.</td>
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<tr>
<td>14</td>
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<td>16</td>
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<tr>
<td>17</td>
<td>BT_HOST_WAKE</td>
<td>I/O</td>
<td>BT_HOST_WAKE</td>
<td>Host wake-up. Signal from the CYW4373 to the host indicating that the CYW4373 requires attention. The polarity of this signal is software configurable and can be asserted high or low.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>BT_GPIO_2</td>
<td>I/O</td>
<td>BT_GPIO_2</td>
<td>Bluetooth® general-purpose I/O.</td>
<td></td>
<td></td>
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<tr>
<td>19</td>
<td>BT_GPIO_3</td>
<td>I/O</td>
<td>BT_GPIO_3</td>
<td>Bluetooth® general-purpose I/O.</td>
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<td>20</td>
<td>BT_GPIO_5</td>
<td>I/O</td>
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<td>Bluetooth® general-purpose I/O.</td>
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<td>22</td>
<td>WL_ANT</td>
<td>RF</td>
<td>-</td>
<td>RF output for WLAN/BT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>RF_SW_CTRL_5</td>
<td>O</td>
<td>RF_SW_CTRL_5</td>
<td>Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Preliminary Specification Number: SP-ZZ2BC-E

#### Description

**Programmable RF switch control lines.** The control lines are programmable via the driver and NVRAM file.

**SDIO command line**

**SDIO data line 1**

**SDIO data line 0**

**SDIO data line 2**

**SDIO clock input**

**Supply for PMU, BT, WLAN, SDIO.**

**1.2V supply for the PCIe.**

**Programmable GPIO Pin**

**Data minus of shared USB2.0 port.**

**Data plus of shared USB2.0 port.**

**Power Supply for shared USB2.0. When VBAT is between 3.6V to 4.8V connect to VOUT_3P3 i.e. 3.3V output of LDO3P3. When VBAT is 3.3V connect directly to VBAT.**

**Bandgap reference resistor; 4.75K ohm +/-1% for USB. DNI for SDIO.**

**Bluetooth® device wake-up: Signal from the host to the CYW4373 indicating that the host requires attention. The polarity of this signal is software configurable and can be asserted high or low.**

**Programmable GPIO Pin**

**JTAG select. This pin must be kept NO CONNECT if the JTAG interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL = 1:**

- GPIO_2 is TCK
- GPIO_3 is TMS
- GPIO_4 is TDIO
- GPIO_5 is TDO
- GPIO_6 is TRST_L

---

<table>
<thead>
<tr>
<th>No.</th>
<th>Terminal Name</th>
<th>Type</th>
<th>Connection to IC Terminal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>RF_SW_CTRL_0</td>
<td>O</td>
<td>RF_SW_CTRL_0</td>
<td>Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.</td>
</tr>
<tr>
<td>27</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>28</td>
<td>SDIO_CMD</td>
<td>I/O</td>
<td>SDIO_CMD</td>
<td>SDIO command line</td>
</tr>
<tr>
<td>29</td>
<td>SDIO_DATA_1</td>
<td>I/O</td>
<td>SDIO_DATA_1</td>
<td>SDIO data line 1</td>
</tr>
<tr>
<td>30</td>
<td>SDIO_DATA_0</td>
<td>I/O</td>
<td>SDIO_DATA_0</td>
<td>SDIO data line 0</td>
</tr>
<tr>
<td>31</td>
<td>SDIO_DATA_3</td>
<td>I/O</td>
<td>SDIO_DATA_3</td>
<td>SDIO data line 3</td>
</tr>
<tr>
<td>32</td>
<td>SDIO_DATA_2</td>
<td>I/O</td>
<td>SDIO_DATA_2</td>
<td>SDIO data line 2</td>
</tr>
<tr>
<td>33</td>
<td>SDIO_CLK</td>
<td>I</td>
<td>SDIO_CLK</td>
<td>SDIO clock input</td>
</tr>
<tr>
<td>34</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>35</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>36</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>37</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>38</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>39</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>40</td>
<td>NC</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>41</td>
<td>GND</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>42</td>
<td>VDDIO</td>
<td>PI</td>
<td>VDDIO/BT_VDDO</td>
<td>Supply for PMU, BT, WLAN, SDIO.</td>
</tr>
<tr>
<td>44</td>
<td>VOUT_BBPLL</td>
<td>PO</td>
<td>VOUT_HLD0</td>
<td>1.2V supply for the PCIe.</td>
</tr>
<tr>
<td>45</td>
<td>GPIO_1</td>
<td>I/O</td>
<td>GPIO_1</td>
<td>Programmable GPIO Pin</td>
</tr>
<tr>
<td>46</td>
<td>USB2_DM</td>
<td>I/O</td>
<td>USB2_DM</td>
<td>Data minus of shared USB2.0 port.</td>
</tr>
<tr>
<td>47</td>
<td>USB2_DP</td>
<td>I/O</td>
<td>USB2_DP</td>
<td>Data plus of shared USB2.0 port.</td>
</tr>
<tr>
<td>48</td>
<td>USB2_MONCDR</td>
<td>O</td>
<td>USB2_MONCDR</td>
<td>CDR monitor for debug.</td>
</tr>
<tr>
<td>49</td>
<td>USB2_AVDD33</td>
<td>PI</td>
<td>USB2_AVDD33</td>
<td>-</td>
</tr>
<tr>
<td>50</td>
<td>USB2_RREF</td>
<td>I/O</td>
<td>USB2_RREF</td>
<td>Bandgap reference resistor; 4.75K ohm +/-1% for USB. DNI for SDIO.</td>
</tr>
<tr>
<td>51</td>
<td>BT_DEV_WAKE</td>
<td>I</td>
<td>BT_DEV_WAKE</td>
<td>Bluetooth® device wake-up: Signal from the host to the CYW4373 indicating that the host requires attention. The polarity of this signal is software configurable and can be asserted high or low.</td>
</tr>
<tr>
<td>52</td>
<td>WL_HOST_WAKE</td>
<td>O</td>
<td>GPIO_0</td>
<td>Programmable GPIO Pin</td>
</tr>
<tr>
<td>53</td>
<td>JTAG_SEL</td>
<td>I</td>
<td>JTAG_SEL</td>
<td>-</td>
</tr>
<tr>
<td>No.</td>
<td>Terminal Name</td>
<td>Type</td>
<td>Connection to IC Terminal</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>---------------</td>
<td>------</td>
<td>---------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>54</td>
<td>STRAP_1</td>
<td>I</td>
<td>STRAP_1</td>
<td>USBHUB_BYPASS</td>
</tr>
</tbody>
</table>
| 55  | STRAP_2       | I    | STRAP_2                   | USB_DISABLE  
|     |               |      |                           | 1:USB disable  
|     |               |      |                           | 0: USB enable  |
| 56  | STRAP_0       | I    | STRAP_0                   | SDIO_PADVDDIO sel 
|     |               |      |                           | 1: SDIO is 1.8V  
|     |               |      |                           | 0: SDIO is 3.3V or USB mode |
| 57  | GND           | -    | -                         | -           |
| 58  | GND           | -    | -                         | -           |
| 59  | NC            | -    | -                         | -           |
| 60  | NC            | -    | -                         | -           |
| 61  | GND           | -    | -                         | -           |
| 62  | GND           | -    | -                         | -           |
| 63  | TRST_L        | I/O  | GPIO_6                    | GPIO_6 is TRST_L |
| 64  | JTAG_TDI      | I/O  | GPIO_4                    | GPIO_4 is TDI |
| 65  | JTAG_TDO      | I/O  | GPIO_5                    | GPIO_5 is TDO |
| 66  | JTAG_TCK/SWCLK | I/O | GPIO_2                    | GPIO_2 is TCK/SWCLK |
| 67  | JTAG_TMS/SWDIO | I/O | GPIO_3                    | GPIO_3 is TMS/SWDIO |
| 68  | BT_REG_EN     | I    | BT_REG_ON                 | Used by PMU to power-up or power down the internal CYW8x373 regulators used by the Bluetooth® section. Also, when deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 69  | GND           | -    | -                         | -           |
| 70  | GND           | -    | -                         | -           |
| 71  | GND           | -    | -                         | -           |
| 72  | GND           | -    | -                         | -           |
| 73  | GND           | -    | -                         | -           |
| 74  | GND           | -    | -                         | -           |
| 75  | GND           | -    | -                         | -           |
| 76  | GND           | -    | -                         | -           |
| 77  | GND           | -    | -                         | -           |
### SDIO Pin Description

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin Name</th>
<th>(i) SD 4-bit Mode</th>
<th>(ii) SD 1-bit Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>SDIO_CLK</td>
<td>CLK Clock</td>
<td>CLK Clock</td>
</tr>
<tr>
<td>17</td>
<td>SDIO_D0</td>
<td>DATA0 Data line 0</td>
<td>DATA Data line</td>
</tr>
<tr>
<td>15</td>
<td>SDIO_D1</td>
<td>DATA1 Data line 1</td>
<td>IRQ Interrupt</td>
</tr>
<tr>
<td>16</td>
<td>SDIO_D2</td>
<td>DATA2 Data line 2</td>
<td>NC Not used</td>
</tr>
<tr>
<td>14</td>
<td>SDIO_D3</td>
<td>DATA3 Data line 3</td>
<td>NC Not used</td>
</tr>
<tr>
<td>18</td>
<td>SDIO_CMD</td>
<td>CMD Command line</td>
<td>CMD Command line</td>
</tr>
</tbody>
</table>

### Strapping Options

<table>
<thead>
<tr>
<th>Mode Select</th>
<th>STRAP_2</th>
<th>STRAP_1</th>
<th>STRAP_0</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SDIO</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

0 = SDIO is 3.3V  
1 = SDIO is 1.8V
6. Rating

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature</td>
<td>-40</td>
<td>+125</td>
<td>deg.C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VBAT</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>-0.5</td>
<td>3.9</td>
<td>V</td>
</tr>
</tbody>
</table>

* Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

7. Operating Condition

7.1. Operating condition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>-20</td>
<td>+25</td>
<td>+70</td>
<td>deg.C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VBAT</td>
<td>3.2</td>
<td>3.6</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>1.62</td>
<td>1.8</td>
<td>1.98</td>
<td>V</td>
</tr>
</tbody>
</table>

*1 CYW4373 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.6V<VBAT<4.8V.

*2 The maximum continuous voltage is 4.8V.

7.2. External LPO signal Requirement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>External LPO Clock</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal input frequency</td>
<td>32.768</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency accuracy</td>
<td>+/-200</td>
<td>ppm</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>30-70</td>
<td>%</td>
</tr>
<tr>
<td>Input signal amplitude</td>
<td>200 - 3300</td>
<td>mV, p-p</td>
</tr>
<tr>
<td>Signal type</td>
<td>Square-wave or sine-wave</td>
<td>-</td>
</tr>
<tr>
<td>Input impedance*</td>
<td>&gt; 100k</td>
<td>ohm</td>
</tr>
<tr>
<td></td>
<td>&lt; 5</td>
<td>pF</td>
</tr>
<tr>
<td>Clock jitter (during initial start-up)</td>
<td>&lt;10,000</td>
<td>ppm</td>
</tr>
</tbody>
</table>

a) When power is applied or switch off.

---

1 Functionality is guaranteed but specifications require derating at extreme temperatures

Preliminary

< Specification may be changed by Murata without notice >

Murata(China) Investment Co., Ltd.
8. Power Up Sequence
8.1. Power Up Sequence for WLAN ON, and BT ON

32.768kHz Sleep Clock

VBAT1, 2

VDDIO

WL_REG_ON

BT_REG_ON

Notes:
1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

8.2. Power Up Sequence for WLAN ON, and BT OFF

32.768kHz Sleep Clock

VBAT

VDDIO

WL_REG_ON

BT_REG_ON

Notes:
1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
### 8.3. Power Up Sequence for WLAN OFF, and BT ON

32.768kHz Sleep Clock  

<table>
<thead>
<tr>
<th>VBAT</th>
<th>90% of VH</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO</td>
<td>(min.)2 Sleep cycle</td>
</tr>
</tbody>
</table>

**Notes:**
1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

### 8.4. Power Up Sequence for WLAN OFF, and BT OFF

32.768kHz Sleep Clock  

<table>
<thead>
<tr>
<th>VBAT</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO</td>
<td></td>
</tr>
<tr>
<td>WL_REG_ON</td>
<td></td>
</tr>
<tr>
<td>BT_REG_ON</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. VBAT should not rise 10-90% faster than 40 microseconds
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
### 9. Digital I/O Requirements

#### 9.1. Digital I/O Pins

<table>
<thead>
<tr>
<th>Digital I/O Pins</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>For VDDIO = 1.8V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input high voltage</td>
<td>VH</td>
<td>$0.65 \times VDDIO$</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Input low voltage</td>
<td>VL</td>
<td>-</td>
<td>-</td>
<td>$0.35 \times VDDIO$</td>
<td>V</td>
</tr>
<tr>
<td>Output high <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOH</td>
<td>VDDIO-0.45</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output low <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOL</td>
<td>-</td>
<td>-</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>For VDDIO = 3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input high voltage</td>
<td>VH</td>
<td>2.00</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Input low voltage</td>
<td>VL</td>
<td>-</td>
<td>-</td>
<td>0.80</td>
<td>V</td>
</tr>
<tr>
<td>Output high <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOH</td>
<td>VDDIO-0.40</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output low <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOL</td>
<td>-</td>
<td>-</td>
<td>0.40</td>
<td>V</td>
</tr>
</tbody>
</table>

#### 9.2. RF Switch Control Output Pins

<table>
<thead>
<tr>
<th>RF Switch Control Output Pins</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>For VDDIO_RF = 3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output high <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOH</td>
<td>VDDIO-0.40</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output low <a href="mailto:voltage@2.0mA">voltage@2.0mA</a></td>
<td>VOL</td>
<td>-</td>
<td>-</td>
<td>0.40</td>
<td>V</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>COUT</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>pF</td>
</tr>
</tbody>
</table>
## 10. Interface Timing

### 10.1. SDIO Timing (Default Mode)

![Timing diagram](image)

### Parameter Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min(1)</th>
<th>Typ(1)</th>
<th>Max(1)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock CLK (All values are referred to min. VIH and max. VIL[2])</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency-Data Transfer Mode</td>
<td>fPP</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency-Identification Mode</td>
<td>fIOD</td>
<td>0</td>
<td>-</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>Clock Low Time</td>
<td>tWL</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock High Time</td>
<td>tWH</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock Rise Time</td>
<td>tTLH</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Clock Falling Time</td>
<td>tTHL</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Inputs: CMD, DAT (referenced to CLK)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Setup Time</td>
<td>tISU</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Input Hold Time</td>
<td>tIH</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Outputs: CMD, DAT (referenced to CLK)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Delay time-Data Transfer Mode</td>
<td>tODLY</td>
<td>0</td>
<td>-</td>
<td>14</td>
<td>ns</td>
</tr>
<tr>
<td>Output Delay time-Identification Mode</td>
<td>tODLY</td>
<td>0</td>
<td>-</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1). Timing is based on CL ≤ 40pF load on CMD and Data.
(2). Min (Vih) = 0.7*VDDIO and max (Vil) = 0.2*VDDIO.
10.2. SDIO Timing (High Speed Mode)

Parameter | Symbol | Min$^{(1)}$ | Typ$^{(1)}$ | Max$^{(1)}$ | Unit
--- | --- | --- | --- | --- | ---
Clock CLK (All values are referred to min. VIH and max. VIL$^{(2)}$) |  |  |  |  | 
Frequency-Data Transfer Mode | fPP | 0 | - | 50 | MHz
Frequency-Identification Mode | fOD | 0 | - | 400 | kHz
Clock Low Time | tWL | 7 | - | - | ns
Clock High Time | tWH | 7 | - | - | ns
Clock Rise Time | tTLH | - | - | 3 | ns
Clock Falling Time | tTHL | - | - | 3 | ns
Inputs: CMD, DAT (referenced to CLK) |  |  |  |  | 
Input Setup Time | tISU | 6 | - | - | ns
Input Hold Time | tIH | 2 | - | - | ns
Outputs: CMD, DAT (referenced to CLK) |  |  |  |  | 
Output Delay time-Data Transfer Mode | tODLY | - | - | 14 | ns
Output Hold time | tOH | 2.5 | - | - | ns
Total System Capacitance (each line) | CL | - | - | 40 | pF

(1) Timing is based on CL < 40pF load on CMD and Data.
(2) Min (Vih) = 0.7*VDDIO and max (Vil) = 0.2*VDDIO.
10.3. SDIO BUS Timing Specifications in SDR Modes

Clock Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>tCLK</td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td>SDR12 mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td>-</td>
<td>ns</td>
<td>SDR25 mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>-</td>
<td>ns</td>
<td>SDR50 mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.8</td>
<td>-</td>
<td>ns</td>
<td>SDR104 mode</td>
</tr>
<tr>
<td></td>
<td>tCR,tCF</td>
<td>-</td>
<td>0.2 x tCLK</td>
<td>ns</td>
<td>tCR,tCF&lt;2.00ns(max)@100MHz,cCARD=10pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>tCR,tCF&lt;0.96ns(max)@208MHz,cCARD=10pF</td>
</tr>
</tbody>
</table>

Card Input Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDR104 Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tIS</td>
<td>1.4</td>
<td>-</td>
<td>ns</td>
<td>cCARD = 10pF,VCT = 0.975V</td>
</tr>
<tr>
<td>tIH</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
<td>cCARD = 5pF,VCT = 0.975V</td>
</tr>
<tr>
<td>SDR50 Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tIS</td>
<td>3.0</td>
<td>-</td>
<td>ns</td>
<td>cCARD = 10pF,VCT = 0.975V</td>
</tr>
<tr>
<td>tIH</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
<td>cCARD = 5pF,VCT = 0.975V</td>
</tr>
</tbody>
</table>
Card Output Timing

SDIO Bus Ouput Timing (SDR Modes up to 100MHz)

SDIO_CLK

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>tODLY</td>
<td>-</td>
<td>7.5</td>
<td>ns</td>
<td>tCLK ( \geq 10)ns CL = 30pF using driver type B for SDR50</td>
</tr>
<tr>
<td>tODLY</td>
<td>-</td>
<td>14.0</td>
<td>ns</td>
<td>tCLK ( \geq 20)ns CL = 40pF using for SDR12, SDR25</td>
</tr>
<tr>
<td>tOH</td>
<td>1.5</td>
<td>-</td>
<td>ns</td>
<td>Hold time at the tODLY(min) CL = 15pF</td>
</tr>
</tbody>
</table>
SDIO Bus Output Timing (SDR Modes 100MHz to 208MHz)

SDIO_CLK

CMD input
DAT[3:0]

t_{CLK}
t_{OP}
t_{ODW}

SDIO Bus Output Timing Parameters (SDR Modes 100MHz to 208MHz)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{OP}</td>
<td>0</td>
<td>2</td>
<td>UI</td>
<td>Card output phase</td>
</tr>
<tr>
<td>Δt_{OP}</td>
<td>-350</td>
<td>+1550</td>
<td>ps</td>
<td>Delay variation due to temp change after tuning</td>
</tr>
<tr>
<td>t_{ODW}</td>
<td>0.60</td>
<td></td>
<td>UI</td>
<td>t_{ODW} = 2.88ns @208MHz</td>
</tr>
</tbody>
</table>

- Δt_{OP}=+1550ps for junction temperature of Δtop=90°C during operation.
- Δt_{OP}=-350ps for junction temperature of Δtop=-20°C during operation.
- Δt_{OP}=+2600ps for junction temperature of Δtop=-20°C to +125°C during operation

Δtop Consideration for Variable Data Window (SDR 104 Mode)

Data valid window

Sampling point after tuning

Δt_{OP} = 1500 ps

Sampling point after card junction heating by +30°C from tuning temperature

Δt_{ODW} = -350 ps

Data valid window

Sampling point after card junction cooling by -20°C from tuning temperature
10.4. SDIO Timing Specifications in DDR50 Mode

SDIO Clock Timing (DDR50 Mode)

```
SDIO_CLK
```

SDIO Bus Clock Timing Parameters (DDR50 Mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>tCLK</td>
<td>20</td>
<td></td>
<td>ns</td>
<td>DDR50 mode</td>
</tr>
<tr>
<td></td>
<td>tCR, tCF</td>
<td>-</td>
<td>0.2 x tCLK</td>
<td>ns</td>
<td>tCR, tCF&lt;4.00ns(max)@50MHz, cCard=10pF</td>
</tr>
<tr>
<td>Clock duty cycle</td>
<td>-</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

SDIO Data Timing (DDR50 Mode)

```
SDIO_CLK
DAT[3:0] input
DAT[3:0] output
```

In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

SDIO Bus Timing parameters (DDR50 Mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input CMD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input setup time</td>
<td>tISU</td>
<td>6</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;10pF (1 card)</td>
</tr>
<tr>
<td>Input hold time</td>
<td>tIH</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;10pF (1 card)</td>
</tr>
<tr>
<td>Output CMD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output delay time</td>
<td>tODLY</td>
<td>-</td>
<td>13.7</td>
<td>ns</td>
<td>Ccard&lt;30pF (1 card)</td>
</tr>
<tr>
<td>Output hold time</td>
<td>tOH</td>
<td>1.5</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;15pF (1 card)</td>
</tr>
<tr>
<td>Input DAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input setup time</td>
<td>tISU2x</td>
<td>3</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;10pF (1 card)</td>
</tr>
<tr>
<td>Input hold time</td>
<td>tIH2x</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;10pF (1 card)</td>
</tr>
<tr>
<td>Output DAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output delay time</td>
<td>tODLY2x</td>
<td>-</td>
<td>7.5</td>
<td>ns</td>
<td>Ccard&lt;25pF (1 card)</td>
</tr>
<tr>
<td>Output hold time</td>
<td>tOH2x</td>
<td>1.5</td>
<td>-</td>
<td>ns</td>
<td>Ccard&lt;15pF (1 card)</td>
</tr>
</tbody>
</table>
10.5. UART Timing (Default Mode)

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The UART supports the Bluetooth® 4.2 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud. The UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

The timing diagrams and reference table are provided for detailed analysis of the UART timing and reference values.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Delay time, UART_CTS_N low to UART_TXD valid</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>Bit periods</td>
</tr>
<tr>
<td>2</td>
<td>Setup time, UART_CTS_N high before midpoint of stop bit</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>Bit periods</td>
</tr>
<tr>
<td>3</td>
<td>Delay time, midpoint of stop bit to UART_RTS_N high</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>Bit periods</td>
</tr>
</tbody>
</table>

Example of Common Baud Rates

<table>
<thead>
<tr>
<th>Desired Rate</th>
<th>Actual Rate set in the module</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4000000</td>
<td>4000000</td>
<td>0.00</td>
</tr>
<tr>
<td>3000000</td>
<td>3000000</td>
<td>0.00</td>
</tr>
<tr>
<td>921600</td>
<td>923077</td>
<td>0.16</td>
</tr>
<tr>
<td>115200</td>
<td>115385</td>
<td>0.16</td>
</tr>
<tr>
<td>57600</td>
<td>57692</td>
<td>0.16</td>
</tr>
<tr>
<td>9600</td>
<td>9600</td>
<td>0.00</td>
</tr>
</tbody>
</table>
10.6. Bluetooth® PCM Timing

The PCM Interface can connect to linear PCM Codec devices. In master or slave mode, the module generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the modules.

The PCM interface supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

10.6.1. Short Frame Sync, Master Mode

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCM bit clock frequency</td>
<td>-</td>
<td>-</td>
<td>12</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>PCM bit clock High</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>PCM bit clock Low</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>PCM_SYNC delay</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>PCM_OUT delay</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>PCM_IN setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>7</td>
<td>PCM_IN hold</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>8</td>
<td>Delay from rising edge of PCM_BCLK during last bit period to</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>PCM_OUT becoming high impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
10.7. Short Frame Sync, Slave Mode

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCM bit clock frequency</td>
<td>-</td>
<td>-</td>
<td>12</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>PCM bit clock Low</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>PCM bit clock High</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>PCM_SYNC setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>PCM_SYNC hold</td>
<td>8</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>PCM_OUT delay</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>7</td>
<td>PCM_IN setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>8</td>
<td>PCM_IN hold</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>9</td>
<td>Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
</tbody>
</table>

10.8. Long Frame Sync, Master Mode

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCM bit clock frequency</td>
<td>-</td>
<td>-</td>
<td>12</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>PCM bit clock High</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>PCM bit clock Low</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>PCM_SYNC delay</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>PCM_OUT delay</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>PCM_IN setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>7</td>
<td>PCM_IN hold</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>8</td>
<td>Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT</td>
<td>0</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
</tbody>
</table>
10.9. Long Frame Sync, Slave Mode

Reference | Description | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | ---
1 | PCM bit clock frequency | - | - | 12 | MHz
2 | PCM bit clock High | 41 | - | - | ns
3 | PCM bit clock Low | 41 | - | - | ns
4 | PCM_SYNC setup | 8 | - | - | ns
5 | PCM_SYNC hold | 8 | - | - | ns
6 | PCM_OUT delay | 0 | - | 25 | ns
7 | PCM_IN setup | 8 | - | - | ns
8 | PCM_IN hold | 8 | - | - | ns
9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | - | 25 | ns

10.9.1. Short Frame Sync, Burst Mode

Reference | Description | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | ---
1 | PCM bit clock frequency | - | - | 24 | MHz
2 | PCM bit clock Low | 20.8 | - | - | ns
3 | PCM bit clock High | 20.8 | - | - | ns
4 | PCM_SYNC setup | 8 | - | - | ns
5 | PCM_SYNC hold | 8 | - | - | ns
6 | PCM_IN setup | 8 | - | - | ns
7 | PCM_IN hold | 8 | - | - | ns
### 10.9.2. Long Frame Sync, Burst Mode

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCM bit clock frequency</td>
<td>-</td>
<td>-</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>2</td>
<td>PCM bit clock Low</td>
<td>20.8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>PCM bit clock High</td>
<td>20.8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>PCM_SYNC setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>PCM_SYNC hold</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>PCM_IN setup</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>7</td>
<td>PCM_IN hold</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>
11. DC / RF Characteristics

ALL DC/RF characteristics are defined by following file.

<table>
<thead>
<tr>
<th>WLAN:nvram file</th>
<th>Cyfmac4373-sdio.txt</th>
</tr>
</thead>
<tbody>
<tr>
<td>BT:hcd file</td>
<td>4373A0_Generic_UART_37_4MHz_wlbga_BU_sLNA_202107091730_0x800.hcd</td>
</tr>
</tbody>
</table>

11.1. DC/RF Characteristics for IEEE802.11b - 2.4GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11b</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>DSSS / CCK</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>2412 - 2472MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>1, 2, 5.5, 11Mbps</td>
</tr>
</tbody>
</table>

11.1.1. High Rate Condition for IEEE802.11b – 2.4GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=17dBm, 11Mbps mode

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>350</td>
</tr>
<tr>
<td>*1: Defined when output power setting is 17dBm at Murata module antenna pad</td>
<td></td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>40</td>
</tr>
<tr>
<td>- Tx Characteristics *1-</td>
<td>Min.</td>
</tr>
<tr>
<td>2. Output Power</td>
<td>14.5</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 1st side lobes(-30dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 2nd side lobes(-50dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Power-on and Power-down ramp</td>
<td>-</td>
</tr>
<tr>
<td>5. RF Carrier Suppression</td>
<td>15</td>
</tr>
<tr>
<td>6. Modulation Accuracy (EVM)</td>
<td>-</td>
</tr>
<tr>
<td>7. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td>8. Out band Spurious Emissions</td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>annotation</td>
<td></td>
</tr>
<tr>
<td>47MHz to 74MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>87.5MHz to 118MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>174MHz to 230MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>470MHz to 862MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td>-</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>9. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>10. Maximum Input Level (FER &lt; 8%)</td>
<td>-10</td>
</tr>
<tr>
<td>11. Adjacent Channel Rejection (FER &lt; 8%)</td>
<td>35</td>
</tr>
</tbody>
</table>
### 11.1.2. Low Rate Condition for IEEE802.11b – 2.4GHz

**Conditions:** 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=17dBm, 1Mbps mode

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>- DC Characteristics -</strong></td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *2</td>
<td>340</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>40</td>
</tr>
<tr>
<td>2. Output Power</td>
<td>14.5</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 1st side lobes(-30dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 2nd side lobes(-50dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Power-on and Power-down ramp</td>
<td>-</td>
</tr>
<tr>
<td>5. RF Carrier Suppression</td>
<td>15</td>
</tr>
<tr>
<td>6. Modulation Accuracy (EVM)</td>
<td>-</td>
</tr>
<tr>
<td>7. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td>8. Out band Spurious Emissions</td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>annotation</td>
<td></td>
</tr>
<tr>
<td>47MHz to 74MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>87.5MHz to 118MHz(BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>174MHz to 230MHz(BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>470MHz to 862MHz(BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td>-</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>9. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>10. Maximum Input Level (FER $\leq$ 8%)</td>
<td>-10</td>
</tr>
<tr>
<td>11. Adjacent Channel Rejection (FER $\leq$ 8%)</td>
<td>35</td>
</tr>
</tbody>
</table>

*2: Defined when output power setting is 17dBm at Murata module antenna pad
### 11.2. DC/RF Characteristics for IEEE802.11g - 2.4GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11g</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>2412 - 2472MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>6, 9, 12, 18, 24, 36, 48, 54Mbps</td>
</tr>
</tbody>
</table>

### 11.2.1. High Rate Condition for IEEE802.11g – 2.4GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=16dBm, 54Mbps mode

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>1) DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>290</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>40</td>
</tr>
<tr>
<td>- Tx Characteristics*3 -</td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>13.5</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (-20dBm)</td>
<td>0</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBm)</td>
<td>0</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBm)</td>
<td>0</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBm)</td>
<td>0</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td></td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td></td>
</tr>
<tr>
<td>6. Out band Spurious Emissions</td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>annotation</td>
<td></td>
</tr>
<tr>
<td>47MHz to 74MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>87.5MHz to 118MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>174MHz to 230MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>470MHz to 862MHz(BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td></td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>7. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>8. Maximum Input Level (PER ≤ 10%)</td>
<td>-20</td>
</tr>
<tr>
<td>9. Adjacent Channel Rejection</td>
<td>PER ≤ 10%</td>
</tr>
</tbody>
</table>

*3: Defined when output power setting is 16dBm at Murata module antenna pad
### 11.2.2. Low Rate Condition for IEEE802.11g – 2.4GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=18dBm, 6Mbps mode

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DC Characteristics</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>*4</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Tx Characteristics*4 -</td>
</tr>
<tr>
<td>2. Output Power</td>
<td></td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~ -20dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBr)</td>
<td>0</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td></td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td>6. Out band Spurious Emissions</td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>annotation</td>
<td>47MHz to 74MHz(BW=100kHz)</td>
</tr>
<tr>
<td></td>
<td>87.5MHz to 118MHz(BW=100kHz)</td>
</tr>
<tr>
<td></td>
<td>174MHz to 230MHz(BW=100kHz)</td>
</tr>
<tr>
<td></td>
<td>470MHz to 862MHz(BW=100kHz)</td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Rx Characteristics -</td>
</tr>
<tr>
<td>7. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>8. Maximum Input Level (PER &lt; 10%)</td>
<td>-20</td>
</tr>
<tr>
<td>9. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td>16</td>
</tr>
</tbody>
</table>

*4: Defined when output power setting is 18dBm at Murata module antenna pad
### 11.3. DC/RF Characteristics for IEEE802.11n – 2.4GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>2412 - 2472MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS7</td>
</tr>
</tbody>
</table>

### 11.3.1. High Rate Condition for IEEE802.11n – 2.4GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=14dBm, MCS7

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td></td>
</tr>
<tr>
<td>2) Rx mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>2. Output Power</td>
<td></td>
</tr>
<tr>
<td>3. Spectrum Mask</td>
<td></td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td></td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td></td>
</tr>
<tr>
<td>6. Out band Spurious Emissions</td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>annotation</td>
<td>-36</td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-64</td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td></td>
</tr>
</tbody>
</table>

*5: Defined when output power setting is 14dBm at Murata module antenna pad
### 11.3.2. Low Rate Condition for IEEE802.11n – 2.4GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=16dBm, MCS0

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. DC current</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)*6</td>
<td>300 mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>40 mA</td>
</tr>
<tr>
<td><strong>2. Output Power</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>13.5 16 18.5 dBm</td>
</tr>
<tr>
<td><strong>3. Spectrum Mask</strong></td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0 ~ -20dBm)</td>
<td>0 dB</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20 ~ -28dBm)</td>
<td>0 dB</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28 ~ -45dBm)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-45dBm)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-5 dB</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20 20 ppm</td>
</tr>
<tr>
<td><strong>6. Out band Spurious Emissions</strong></td>
<td></td>
</tr>
<tr>
<td>1) 30MHz to 1GHz (BW=100kHz)</td>
<td>-36 dBm</td>
</tr>
<tr>
<td>annotation</td>
<td></td>
</tr>
<tr>
<td>47MHz to 74MHz (BW=100kHz)</td>
<td>-54 dBm</td>
</tr>
<tr>
<td>87.5MHz to 118MHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>174MHz to 230MHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>470MHz to 862MHz (BW=100kHz)</td>
<td></td>
</tr>
<tr>
<td>2) 1GHz to 12.75GHz (BW=1MHz)</td>
<td>-30 dBm</td>
</tr>
<tr>
<td><strong>7. Minimum Input Level Sensitivity</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-82 dBm</td>
</tr>
<tr>
<td><strong>7. Adjacent Channel Rejection</strong></td>
<td></td>
</tr>
<tr>
<td>(PER ≤ 10%)</td>
<td>16 dB</td>
</tr>
</tbody>
</table>

*6: Defined when output power setting is 16dBm at Murata module antenna pad
### 11.4. DC/RF Characteristics for IEEE802.11a - 5GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11a</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>5180 to 5240MHz, 5260 to 5320MHz, 5500 to 5720MHz, 5745 to 5825MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>6, 9, 12, 18, 24, 36, 48, 54Mbps</td>
</tr>
</tbody>
</table>

#### 11.4.1. High Rate Condition for IEEE802.11a – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=14dBm, 54Mbps

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>- DC Characteristics -</strong></td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *7</td>
<td>290</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>60</td>
</tr>
<tr>
<td><strong>- Tx Characteristics*7 -</strong></td>
<td>Min.</td>
</tr>
<tr>
<td>2. Output Power</td>
<td>12</td>
</tr>
<tr>
<td>3. Spectrum Mask</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~ -20dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBr)</td>
<td>0</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td><strong>- Rx Characteristics -</strong></td>
<td>Min.</td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection</td>
<td>-1</td>
</tr>
</tbody>
</table>

*7: Defined when output power setting is 14dBm at Murata module antenna pad
### 11.4.2. Low Rate Condition for IEEE802.11a – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, 6Mbps

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *8</td>
<td>310</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>60</td>
</tr>
<tr>
<td>- Tx Characteristics*8 -</td>
<td>Min.</td>
</tr>
<tr>
<td>2. Output Power</td>
<td>14</td>
</tr>
<tr>
<td>3. Spectrum Mask</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~-20dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~-28dBr)</td>
<td>0</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td>16</td>
</tr>
</tbody>
</table>

*8: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.5. DC/RF Characteristics for IEEE802.11n(HT20) - 5GHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>IEEE802.11n</td>
</tr>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Frequency</td>
<td>5180 - 5825MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS7</td>
</tr>
</tbody>
</table>

### 11.5.1. High Rate Condition for IEEE802.11n(HT20) – 5GHz

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS7

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *9</td>
<td>280</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>70</td>
</tr>
<tr>
<td>- Tx Characteristics*9 -</td>
<td>Min.</td>
</tr>
<tr>
<td>2. Output Power</td>
<td>12</td>
</tr>
<tr>
<td>3. Spectrum Mask</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~-20dBr)</td>
<td>0</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~-28dBr)</td>
<td>0</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td>Min.</td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-</td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td>-2</td>
</tr>
</tbody>
</table>

*9: Defined when output power setting is 14dBm at Murata module antenna pad
### 11.5.2. Low Rate Condition for IEEE802.11n(HT20) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=16dBm, MCS0

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. DC Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>*10 300mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>60mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td><strong>2. Output Power</strong></td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~ -20dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td><strong>4. Constellation Error (EVM)</strong></td>
<td>-30dB</td>
</tr>
<tr>
<td><strong>5. Frequency tolerance</strong></td>
<td>-20ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td><strong>6. Minimum Input Level Sensitivity</strong></td>
<td>-82dB</td>
</tr>
<tr>
<td><strong>7. Adjacent Channel Rejection (PER &lt; 10%)</strong></td>
<td>-</td>
</tr>
</tbody>
</table>

*10: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.6. DC/RF Characteristics for IEEE802.11ac(HT20) - 5GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11ac</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Frequency</td>
<td>5180 - 5825MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS8</td>
</tr>
</tbody>
</table>

### 11.6.1. High Rate Condition for IEEE802.11ac(VHT20) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=13dBm, MCS8

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
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<tbody>
<tr>
<td><strong>1. DC current</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>*11 280mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>60mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td><strong>2. Output Power</strong></td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~ -20dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0dB</td>
</tr>
<tr>
<td><strong>4. Constellation Error (EVM)</strong></td>
<td>-30dB</td>
</tr>
<tr>
<td><strong>5. Frequency tolerance</strong></td>
<td>-20ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td><strong>6. Minimum Input Level Sensitivity</strong></td>
<td>-59dB</td>
</tr>
<tr>
<td><strong>7. Adjacent Channel Rejection (PER &lt; 10%)</strong></td>
<td>-</td>
</tr>
</tbody>
</table>

*11: Defined when output power setting is 13dBm at Murata module antenna pad
### 11.6.2. Low Rate Condition for IEEE802.11ac(VHT20) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=16dBm, MCS0

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>- DC Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>300 mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>60 mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>14 dBm</td>
</tr>
<tr>
<td>3. Spectrum Mask</td>
<td></td>
</tr>
<tr>
<td>1) 9MHz to 11MHz (0~ -20dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>2) 11MHz to 20MHz (-20~ -28dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>3) 20MHz to 30MHz (-28~ -40dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4) 30MHz to 33MHz (-40dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-27 dB</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20 ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-61 dBm</td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER ≤ 10%)</td>
<td>-2 dB</td>
</tr>
</tbody>
</table>

*12: Defined when output power setting is 16dBm at Murata module antenna pad

### 11.7. DC/RF Characteristics for IEEE802.11n(HT 40MHz) - 5GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>5190 to 5795MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS7</td>
</tr>
</tbody>
</table>

### 11.7.1. High Rate Condition for IEEE802.11n(HT40) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=13dBm, MCS7, HT 40MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
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</thead>
<tbody>
<tr>
<td><strong>- DC Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>320 mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>70 mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics</strong></td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>11 dBm</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 19MHz to 21MHz (0~ -20dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>2) 21MHz to 40MHz (-20~ -28dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>3) 40MHz to 60MHz (-28~ -45dBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4) 60MHz to 80MHz (-45dB)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-27 dB</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20 ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-61 dBm</td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER ≤ 10%)</td>
<td>-2 dB</td>
</tr>
</tbody>
</table>

*13: Defined when output power setting is 13dBm at Murata module antenna pad
### 11.7.2. Low Rate Condition for IEEE802.11n (HT40) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=14dBm, MCS0, HT 40MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td></td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *14</td>
<td>350 mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>70 mA</td>
</tr>
<tr>
<td>- Tx Characteristics*14 -</td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>12 14 16 dBm</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 19MHz to 21MHz (0~ -20dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>2) 21MHz to 40MHz (-20~ -28dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>3) 40MHz to 60MHz (-28~ -45dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4) 60MHz to 80MHz (-45dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>- 5 dB</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20 20 ppm</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td></td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection</td>
<td></td>
</tr>
</tbody>
</table>

*14: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.8. DC/RF Characteristics for IEEE802.11ac (VHT 40MHz) - 5GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11ac</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>5190 to 5795MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS9</td>
</tr>
</tbody>
</table>

### 11.8.1. High Rate Condition for IEEE802.11ac (VHT40) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO=3.3V, Output power setting=11dBm, MCS9, VHT 40MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>- DC Characteristics -</td>
<td></td>
</tr>
<tr>
<td>1. DC current</td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval) *15</td>
<td>320 mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>70 mA</td>
</tr>
<tr>
<td>- Tx Characteristics*15 -</td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>9 11 13 dBm</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
</tr>
<tr>
<td>1) 19MHz to 21MHz (0~ -20dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>2) 21MHz to 40MHz (-20~ -28dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>3) 40MHz to 60MHz (-28~ -45dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4) 60MHz to 80MHz (-45dBBr)</td>
<td>0 dB</td>
</tr>
<tr>
<td>4. Constellation Error (EVM)</td>
<td>-32 dB</td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>-20 20 ppm</td>
</tr>
<tr>
<td>- Rx Characteristics -</td>
<td></td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection</td>
<td></td>
</tr>
</tbody>
</table>

*15: Defined when output power setting is 11dBm at Murata module antenna pad
### 11.8.2. Low Rate Condition for IEEE802.11a (VHT40) – 5GHz

**Conditions**: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=14dBm, MCS0, VHT 40MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. DC current</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)  *16</td>
<td>Min. 350 Typ. mA Max. mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>Min. 70 Typ. mA Max. mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics*16 -</strong></td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>Min. 12 Typ. 14 Max. 16 dBm</td>
</tr>
<tr>
<td><strong>3. Spectrum Mask margin</strong></td>
<td></td>
</tr>
<tr>
<td>1) 19MHz to 21MHz (0~ -20dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>2) 21MHz to 40MHz (-20~ -28dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>3) 40MHz to 60MHz (-28~ -45dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>4) 60MHz to 80MHz (-45dB)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td><strong>4. Constellation Error (EVM)</strong></td>
<td>Min. -5 Typ. dB Max. dB</td>
</tr>
<tr>
<td><strong>5. Frequency tolerance</strong></td>
<td>Min. -20 Typ. 20 Max. ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td>Min. 16 Typ. dB Max. dB</td>
</tr>
</tbody>
</table>

*16: Defined when output power setting is 14dBm at Murata module antenna pad

### 11.9. DC/RF Characteristics for IEEE802.11ac(VHT 80MHz) - 5GHz

<table>
<thead>
<tr>
<th>Specification</th>
<th>IEEE802.11ac</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>OFDM</td>
</tr>
<tr>
<td>Channel Frequency</td>
<td>5210MHz to 5775MHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>MCS0-MCS9</td>
</tr>
</tbody>
</table>

### 11.9.1. High Rate Condition for IEEE802.11ac(VHT80) – 5GHz

**Conditions**: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=12dBm, MCS9, VHT 80MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. DC current</strong></td>
<td></td>
</tr>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)  *17</td>
<td>Min. 340 Typ. mA Max. mA</td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>Min. 90 Typ. mA Max. mA</td>
</tr>
<tr>
<td><strong>- Tx Characteristics*17 -</strong></td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>Min. 9 Typ. 11 Max. 13 dBm</td>
</tr>
<tr>
<td><strong>3. Spectrum Mask margin</strong></td>
<td></td>
</tr>
<tr>
<td>1) 39MHz to 41MHz (0~ -20dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>2) 41MHz to 80MHz (-20~ -28dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>3) 80MHz to 120MHz (-28~ -40dBr)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td>4) 120MHz to 140MHz (-40dB)</td>
<td>Min. 0 Typ. dB Max. dB</td>
</tr>
<tr>
<td><strong>4. Constellation Error</strong></td>
<td>Min. -32 Typ. dB Max. dB</td>
</tr>
<tr>
<td><strong>5. Frequency tolerance</strong></td>
<td>Min. -20 Typ. 20 Max. ppm</td>
</tr>
<tr>
<td><strong>- Rx Characteristics -</strong></td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER &lt; 10%)</td>
<td>Min. -9 Typ. dB Max. dB</td>
</tr>
</tbody>
</table>

*17: Defined when output power setting is 11dBm at Murata module antenna pad
### 11.9.2. Low Rate Condition for IEEE802.11ac(VHT80) – 5GHz

Conditions: 25deg.C, VBAT=3.3V, VDDIO= 3.3V, Output power setting=13dBm, MCS0, VHT 80MHz

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. DC current</strong></td>
<td></td>
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<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
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</tr>
<tr>
<td>2) Rx mode</td>
<td></td>
</tr>
<tr>
<td>- Tx Characteristics</td>
<td></td>
</tr>
<tr>
<td><strong>2. Output Power</strong></td>
<td></td>
</tr>
<tr>
<td><strong>3. Spectrum Mask margin</strong></td>
<td></td>
</tr>
<tr>
<td>1) 39MHz to 41MHz (0~ -20dBr)</td>
<td></td>
</tr>
<tr>
<td>2) 41MHz to 80MHz (-20~ -28dB)</td>
<td></td>
</tr>
<tr>
<td>3) 80MHz to 120MHz (-28~ -40dB)</td>
<td></td>
</tr>
<tr>
<td>4) 120MHz to 140MHz (-40dB)</td>
<td></td>
</tr>
<tr>
<td><strong>4. Constellation Error</strong></td>
<td></td>
</tr>
<tr>
<td><strong>5. Frequency tolerance</strong></td>
<td></td>
</tr>
<tr>
<td><strong>6. Minimum Input Level Sensitivity</strong></td>
<td></td>
</tr>
<tr>
<td><strong>7. Adjacent Channel Rejection (PER ≤ 10%)</strong></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Items</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Tx mode (1024byte, 20usec interval)</td>
<td>380</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2) Rx mode</td>
<td>90</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Tx Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2. Output Power</td>
<td>11</td>
<td>13</td>
<td>15</td>
<td>dBm</td>
</tr>
<tr>
<td>3. Spectrum Mask margin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1) 39MHz to 41MHz (0~ -20dBr)</td>
<td>0</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2) 41MHz to 80MHz (-20~ -28dB)</td>
<td>0</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3) 80MHz to 120MHz (-28~ -40dB)</td>
<td>0</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4) 120MHz to 140MHz (-40dB)</td>
<td>0</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. Constellation Error</td>
<td>-</td>
<td>-5</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>5. Frequency tolerance</td>
<td>20</td>
<td>20</td>
<td>ppm</td>
<td></td>
</tr>
<tr>
<td>6. Minimum Input Level Sensitivity</td>
<td>-</td>
<td>-76</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>7. Adjacent Channel Rejection (PER ≤ 10%)</td>
<td>16</td>
<td>-</td>
<td>-</td>
<td>dB</td>
</tr>
</tbody>
</table>

*18: Defined when output power setting is 13dBm at Murata module antenna pad
### 11.10. DC/RF Characteristics for Bluetooth®

Conditions: 25°C, \( V_{BAT}=3.3\) V, \( V_{DDIO}=3.3\) V

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bluetooth® specification (power class)</strong></td>
<td>Version 5.2</td>
</tr>
<tr>
<td><strong>Channel frequency (spacing)</strong></td>
<td>2402 to 2480 MHz (1MHz)</td>
</tr>
<tr>
<td><strong>Current Consumption</strong></td>
<td></td>
</tr>
<tr>
<td>( (a)) ( Tx=Rx=\text{DH5} ) (fully occupied)</td>
<td>Min.</td>
</tr>
<tr>
<td>( (b)) ( Tx=Rx=2\text{DH5} ) (fully occupied)</td>
<td>-</td>
</tr>
<tr>
<td>( (c)) ( Tx=Rx=3\text{DH5} ) (fully occupied)</td>
<td>-</td>
</tr>
<tr>
<td><strong>Transmitter</strong></td>
<td>Min.</td>
</tr>
<tr>
<td><strong>Output Power@DH5</strong></td>
<td>6</td>
</tr>
<tr>
<td><strong>Frequency range</strong></td>
<td>2400</td>
</tr>
<tr>
<td><strong>20dB bandwidth</strong></td>
<td>-</td>
</tr>
<tr>
<td><strong>Adjacent Channel Power</strong> *1</td>
<td></td>
</tr>
<tr>
<td>( (a)) ( [M-N]=2 )</td>
<td>-</td>
</tr>
<tr>
<td>( (b)) ( [M-N] \geq 3 )</td>
<td>-</td>
</tr>
<tr>
<td><strong>Modulation characteristics</strong></td>
<td></td>
</tr>
<tr>
<td>( (a)) Modulation ( \Delta f_{1\text{avg}} )</td>
<td>140</td>
</tr>
<tr>
<td>( (b)) Modulation ( \Delta f_{\text{max}} )</td>
<td>115</td>
</tr>
<tr>
<td>( (c)) Modulation ( \Delta f_{2\text{avg}} / \Delta f_{1\text{avg}} )</td>
<td>0.8</td>
</tr>
<tr>
<td><strong>Carrier Frequency Drift</strong></td>
<td></td>
</tr>
<tr>
<td>( (a)) 1slot</td>
<td>-25</td>
</tr>
<tr>
<td>( (b)) 3slot / 5slot</td>
<td>-40</td>
</tr>
<tr>
<td>( (c)) Maximum drift rate</td>
<td>-</td>
</tr>
<tr>
<td><strong>EDR Relative Power</strong></td>
<td>-4</td>
</tr>
<tr>
<td><strong>EDR Carrier Frequency Stability and Modulation Accuracy</strong></td>
<td></td>
</tr>
<tr>
<td>( (a)) ( \omega_i )</td>
<td>-75</td>
</tr>
<tr>
<td>( (b)) ( \omega_i+\omega_o )</td>
<td>-75</td>
</tr>
<tr>
<td>( (c)) ( \omega_o )</td>
<td>-10</td>
</tr>
<tr>
<td>( (d)) RMS DEVM (DQPSK)</td>
<td>-</td>
</tr>
<tr>
<td>( (e)) Peak DEVM (DQPSK)</td>
<td>-</td>
</tr>
<tr>
<td>( (f)) 99% DEVM (DQPSK)</td>
<td>-</td>
</tr>
<tr>
<td>( (g)) RMS DEVM (8DPSK)</td>
<td>-</td>
</tr>
<tr>
<td>( (h)) Peak DEVM (8DPSK)</td>
<td>-</td>
</tr>
<tr>
<td>( (i)) 99% DEVM (8DPSK)</td>
<td>-</td>
</tr>
<tr>
<td><strong>Spurious Emissions</strong></td>
<td></td>
</tr>
<tr>
<td>( (a)) 30MHz to 1GHz (BW=100kHz)</td>
<td>-</td>
</tr>
<tr>
<td>( (b)) 1GHz to 12.75GHz (BW=1MHz)</td>
<td>-</td>
</tr>
<tr>
<td><strong>Receiver</strong></td>
<td>Min.</td>
</tr>
<tr>
<td><strong>BDR Sensitivity (BER&lt;0.1%)</strong></td>
<td>-</td>
</tr>
<tr>
<td><strong>EDR Sensitivity (BER&lt;0.007%)@8DPSK</strong></td>
<td>-</td>
</tr>
<tr>
<td><strong>C/I Performance (BER&lt;0.1%)</strong> *2</td>
<td></td>
</tr>
<tr>
<td>( (a)) co-channel</td>
<td>-</td>
</tr>
<tr>
<td>( (b)) 1MHz</td>
<td>-</td>
</tr>
<tr>
<td>( (c)) 2MHz</td>
<td>-</td>
</tr>
<tr>
<td>( (d)) 3MHz</td>
<td>-</td>
</tr>
<tr>
<td>( (e)) image (+4MHz)</td>
<td>-</td>
</tr>
<tr>
<td>( (f)) image +/- 1MHz</td>
<td>-</td>
</tr>
<tr>
<td><strong>Maximum Input Level (BER&lt;0.1%)</strong></td>
<td>-20</td>
</tr>
</tbody>
</table>

*1: Up to three spurious responses within Bluetooth® limits are allowed.
*2: Up to five spurious responses within Bluetooth® limits are allowed.
## 11.11. DC/RF Characteristics for Bluetooth® (LE)

Conditions: 25°C, VBAT=3.3V, VDDIO= 3.3V

<table>
<thead>
<tr>
<th>Items</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth® specification (power class)</td>
<td>Version 5.2 (LE)</td>
</tr>
<tr>
<td>Channel frequency (spacing)</td>
<td>2402 to 2480 MHz (2MHz)</td>
</tr>
<tr>
<td>Number of RF Channel</td>
<td>40</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Item / Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center Frequency</td>
<td>2402</td>
<td>-</td>
<td>2480</td>
<td>MHz</td>
</tr>
<tr>
<td>Channel Spacing</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Number of RF channel</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output power</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>dBm</td>
</tr>
</tbody>
</table>

### Modulation Characteristics

1) $\Delta f_{1\text{avg}}$ | 225 | - | 275 | kHz |
2) $\Delta f_{2\text{max}}$ (at 99.9%) | 185 | - | - | kHz |
3) $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8 | - | - | - |

### Carrier frequency offset and drift

1) Frequency offset | - | - | 150 | kHz |
2) Frequency drift | - | - | 50 | kHz |
3) Drift rate | - | - | 20 | kHz |

| Receiver sensitivity (PER < 30.8%) | - | - | -70 | dBm |
| Maximum input signal level (PER < 30.8%) | -10 | - | - | dBm |
| PER Report Integrity (-30dBm input) | 50 | - | 65.4 | % |
12. Land Patterns

Note:
The land pattern is for reference purpose only.
Consult your manufacturing group to ensure your company’s manufacturing guidelines are met.
13. Reference Circuit

Module
Power supply and configuration

1. VBAT typical value is 3.3 +/-5% V
2. VDDIO can be provided 1.6V or 3.3V
3. LDO IN must be provided
4. For L4 selection, recommended P/N is DYN20161Z-2M2M (Murata)
5. JTAG_SEL must be kept connect to ground if the JTAG interface is not used.
   It must be high to select SWD or JTAG

*1) SDIO Pull-UP Requirements
10 to 100k ohm pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO Host pull-ups. The CYW4373 module (LBE5PK2BC-771) does not have internal pull-ups on these lines.

---

<table>
<thead>
<tr>
<th>Mode Selected</th>
<th>Strap_2</th>
<th>Strap_1</th>
<th>Strap_0</th>
<th>J7</th>
<th>J6</th>
<th>J5</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDIO 3.3V</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Jump on Pin2,3</td>
<td>Jump on Pin1,2</td>
<td>Jump on Pin1,2</td>
</tr>
<tr>
<td>SDIO 1.8V</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Jump on Pin2,3</td>
<td>Jump on Pin1,2</td>
<td>Jump on Pin2,3</td>
</tr>
<tr>
<td>USB</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Jump on Pin1,2</td>
<td>Jump on Pin1,2</td>
<td>Jump on Pin1,2</td>
</tr>
</tbody>
</table>
14. **Tape and Reel Packing**

(1) Dimensions of Tape (Plastic tape)

*1. Cumulative tolerance of max. 40.0 ± 0.15 every 10 pitches

(2) Dimensions of Reel

[unit: mm]
(3) Taping Diagrams

[1] Feeding Hole : As specified in (1)
[2] Hole for chip : As specified in (1)
[4] Base tape : As specified in (1)

(4) Leader and Tail tape

Tail tape (No components) 40 to 200mm
Components
No components 150mm min.
Leader tape (Cover tape alone) 250mm min.
(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

(8) Packaging unit : 1000pcs./ reel

(9) material: Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : 1.1N max. in the direction of peeling as shown below.

165 to 180 °

1.1 N max.

Cover tape

Base tape

(11) Packaging (Humidity proof Packing)

Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.
15. Notice

15.1. Storage Conditions
Please use this product within 6-month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.
(Packing materials, in particular, may be deformed at the temperature over 40 °C)
- The product left more than 6-months after reception, it needs to be confirmed the solder ability before used.
- The product shall be stored in non-corrosive gas (CL2, NH3, SO2, NOx, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
- After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.
Please record and manage the time after opening.
- Product should be repacked with desiccating agent immediately after using.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
Baking condition: 125 +5/-0 °C, 24 hours, 1 time
The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

*For the MSL standard, see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org). If the storage environment is not conducted above standard conditions, it will cause some issue (e.g., Operation issue, Overcurrent, Malfunction) we shall not be responsible for that. Before using please refer to "PRECONDITIONS TO USE MURATA PRODUCTS"

15.2. Handling Conditions
Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability.

15.3. Standard PCB Design (Land Pattern and Dimensions)
All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4. Notice for Chip Placer :
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5. Soldering Conditions :
The recommendation conditions of soldering are as in the following figure.
When products are immersed in solvent after mounting, pay special attention to maintain the temperature difference within 100 °C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C.
Contact Murata before use if concerning other soldering conditions.

15.6. Cleaning:
Since this Product is Moisture Sensitive, any cleaning is not permitted.

15.7. Operational Environment Conditions:
Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.
- In an atmosphere containing corrosive gas (CL2, NH3, SOx, NOx, etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

15.8. Input Power Capacity:
Products shall be used in the input power capacity as specified in this specification. Inform Murata beforehand, in case that the components are used beyond such input power capacity range.
16. Regulatory Statements

16.1. FCC Statements
T.B.D.

16.2. IC Statements
T.B.D.
17. PRECONDITION TO USE OUR PRODUCTS
PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

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The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

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- Aerospace equipment
- Undersea equipment.
- Power plant control equipment
- Medical equipment.
- Traffic signal equipment.
- Burning / explosion control equipment
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/or reliability requirements to the applications listed in the above.

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Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the “U.S. export administration regulations”, etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

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