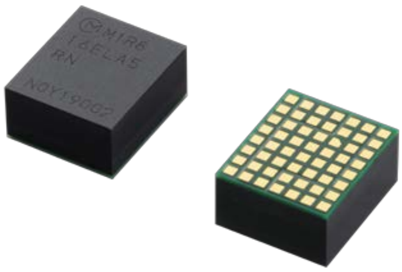


Product Description

The **MYMGM1R816ELA5RN** is miniature MonoBK™ called "Mono Block", non-isolated Point-of-Load (PoL) DC-DC power converters for embedded applications. The small form factor measures only 10.5 x 9.0 x 5.0 mm.

The converter has input voltage ranges of 7.5 to 15V and a maximum output current of 16A. Based on a fixed frequency synchronous buck converter switching topology, this high power conversion efficient PoL module features programmable output voltage 0.7 to 1.8V, ON/OFF control, Power Good (PGOOD) signal output and PMBus™ ALERT output.

This product also includes under voltage lock out (UVLO), output short circuit protection (SCP), over-current protection (OCP), over-voltage protection (OVP). under-voltage protection (UVP) and over-temperature protection (OTP).

Moreover, this converter has PMBus™ interface so various parameters can be handled and monitored by digital signals.

Features

- Settable output voltage from 0.7 to 1.8V
- Up to 16A of output current
- Quick response to load change
- Ultra small surface mount package 10.5 x 9.0 x 5.0mm
- High efficiency of 94.0% max
- Outstanding thermal derating performance
- Over Current (OC) /Voltage (OV), Under Voltage (UV) protection and Over Temperature protection (OT).
- Enable control (Positive logic)
- Power Good (PGOOD) signal
- High Reliability / Heat Shock Testing 700cycle (-40 to +125degC)
- PMBus™ interface available
- PMBus™ 1.3 ready
- Minimum V_{OUT} setting resolution 2mV/bit

Typical Applications

- PCIe / server applications
- FPGA and DSP
- Datacom / telecom systems
- Distributed bus architectures (DBA)
- Programmable logic and mixed voltage

Efficiency

V_{IN} =12V, V_{OUT} =1.8V, T_A =25degC

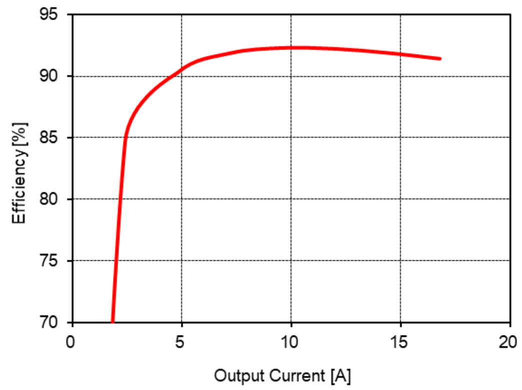


Figure 1. Efficiency Curve

Simplified Application Circuit

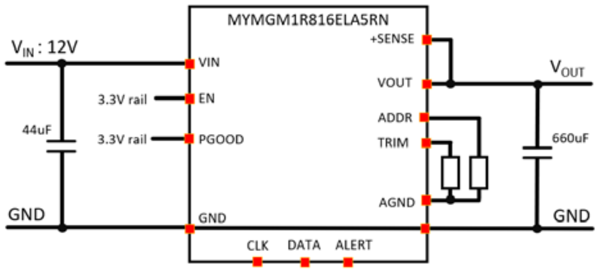


Figure 2. Simplified Circuit Diagram

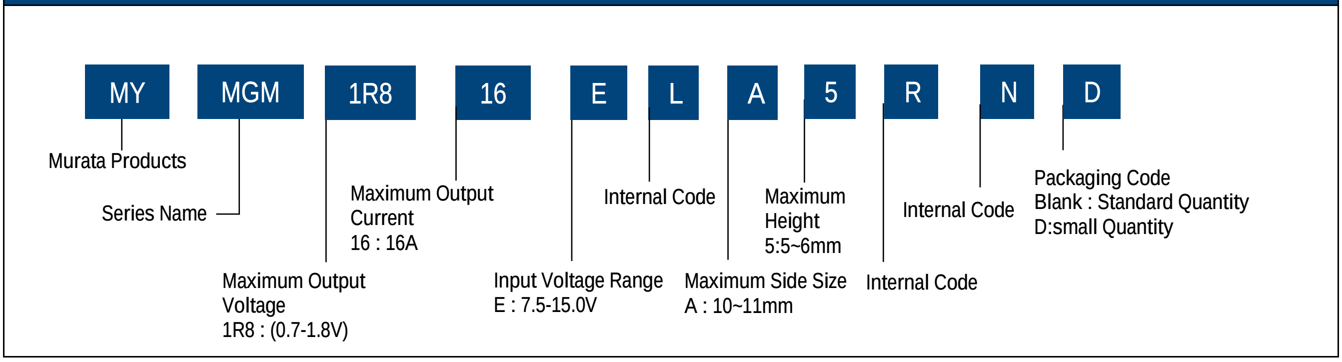
Performance Specifications Summary and Ordering Information

Table 1. Performance Specifications Summary and Ordering Information

PART NUMBER	OUTPUT		INPUT			Efficiency [%]	EN	Package [mm]	MSL	Quantity/ Packing
	V_{OUT} [V]	I_{OUT} (max.) [A]	V_{IN} (typ.) [V]	RANGE [V]	I_{IN} full load [A]					
MYMGM 1R816ELA5RN	0.7-1.8	16	12	7.5-15.0	4.3	91.8	Yes (Positive)	10.5 x 9.0 x 5.0 LGA	3	400 units/T&R
MYMGM 1R816ELA5RND	0.7-1.8	16	12	7.5-15.0	4.3	91.8	Yes (Positive)	10.5 x 9.0 x 5.0 LGA	3	100 units/T&R

1. All specifications are at typical line voltage, V_{OUT} = 1.8V and full load, +25degC unless otherwise noted. Output capacitors are 220uF x 3 ceramic. Input capacitors is 22uF x 2 ceramic and plenty electrolytic capacitors. See detailed specifications. Input and Output capacitors are necessary for our test equipment.
2. Use adequate ground plane and copper thickness adjacent to the converter.

Table 2. Part Numbering



Top Marking Specifications

Because of the small size of these products, the product marking contains a character-reduced code to indicate the model number and manufacturing date code. Not all items on the marking are always used. Please note that the marking differs from the product photograph. Here is the layout of the Marking.

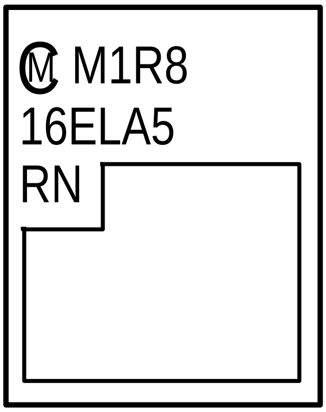


Figure 3. Top Marking Specification

Table 3. Code Description

CODE	DESCRIPTION
(M)	Pin 1 Marking
M1R816ELA5RN	Product code (Please see product code table beside)
	Internal manufacturing code

Table 4. Product code table

PART NUMBER	PRODUCT CODE
MYMGM1R816ELA5RN	M1R816ELA5RN
MYMGM1R816ELA5RND	M1R816ELA5RN

Pin Configuration

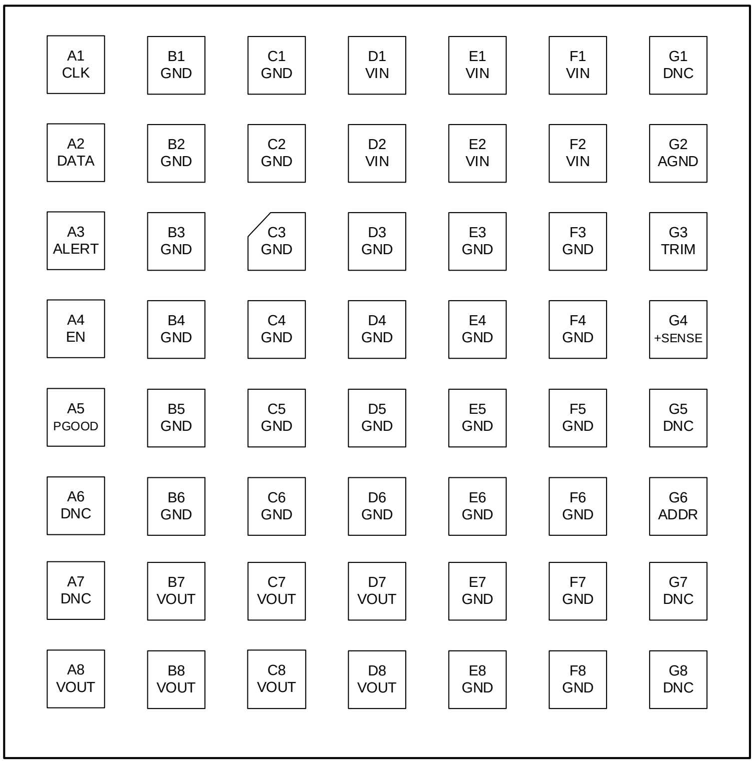


Figure 4. Module Terminals (Top View)

Pin Function & Descriptions

Table 5. Pin Function & Descriptions

PIN No.	NAME	FUNCTION and DESCRIPTION
A1	CLK	PMBus™ Clock.
A2	DATA	PMBus™ data.
A3	ALERT	PMBus™ alert pin. ALT is active low. A pull-up resistor connected to 3.3V is required if the ALT function is needed.
A4	EN	PMBus™ control pin. EN is a digital input that turns the converter on or off with proper ON_OFF_CONFIG (02h) configuration. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. Do not float EN.
A5	PGOOD	Power good output. The output of PGOOD is an open-drain signal. PGOOD requires a pull-up resistor connected to a DC voltage to indicate high if the output voltage is higher than 90% of the nominal voltage. There is a PGOOD delay from low to high. PGOOD must be pulled high to ensure proper operation.
A6	DNC	Do not connect pins. Those pins must be left floating individually.
A7	DNC	Do not connect pins. Those pins must be left floating individually.
A8, B7, B8, C7, C8, D7, D8	VOUT	Power output voltage.
B1-B6, C1-C6, D3-D6, E3-E8, F3-F8	GND	Ground pins. Connect to the GND plane.
D1, D2, E1, E2, F1, F2	VIN	Power input voltage.
G1	DNC	Do not connect pins. Those pins must be left floating individually.
G2	AGND	Analog GND
G3	TRIM	Output voltage setting pin. The divider resistor must be located between GND to set output voltage correctly. Tie the TRIM pins of each phase together.
G4	+SENSE	Output voltage sense positive return. Connect VOUT +SENSE to the output voltage sense of the load directly.
G5	DNC	Do not connect pins. Those pins must be left floating individually.
G6	ADDR	PMBus™ slave address-setting pin. Connect a resistor from ADDR to GND to set the address of this device.
G7	DNC	Do not connect pins. Those pins must be left floating individually.
G8	DNC	Do not connect pins. Those pins must be left floating individually.

Absolute Maximum Ratings (1)(2)

Table 6. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VIN	−0.3	16	V
EN, PGOOD, CLK, DATA, ADDR, ALERT	−0.3	3.9	V
VOUT	0.7	2.0	V
Output Current (I_{OUT})	0	16	A
Storage Temperature (T_{stg})	−40	125	degC
Soldering / Reflow temperature (3)	-	250	degC
Maximum Number of Reflows Allowed	-	1	
ESD Tolerance, HBM (4)	-	±1000	V

Notes:
(1) The application of any stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, and exposure at any of these ratings for extended periods may reduce the reliability of the device. The above "Absolute Maximum Ratings" are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside of the range identified by the operational sections of this specification.
(2) All Voltage are with respect to GND plane.
(3) Recommended Reflow profile is written in "Soldering Guidelines".
(4) Human body model, per the JEDEC standard JS-001-2012.

Recommended Operating Conditions(1)

Table 7. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS
Input Voltage (V_{IN})	7.5	15	V
Ambient Temperature (T_A) (2)	-40	105	degC
Junction Temperature (T_J) (2)	-40	125	degC
Output Current (I_{OUT})	0	16	A

Notes:
(1) Device should not be operated outside the operating conditions. The reliability is tested at the maximum voltage of the recommended operating condition. Above of recommended operation may reduce reliability of the device.
(2) See the temperature derating curves in the thermal deratings. However, do not condensate.

Package Thermal Characteristics

Table 8. Package Thermal Characteristics

PARAMETER	CONDITIONS	TYP	UNITS
Junction-to-top characterization parameter (Ψ_{JT})	V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 16A	1.7	degC/W
	V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 8A	2.2	degC/W

Notes:
(1) The thermal resistances are only reference data, and they are measured with our evaluation board as below.
50.8mm x 60.0mm x 1.6mm (8 Layer, 2oz copper each) FR-4.

Electrical Characteristics[1]

Electrical Characteristics Table

V_{IN} = 12V, I_{OUT} = 16A, T_A = 25degC, unless otherwise noted

Table 9. Electric Characteristics Table

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage	V_{IN}		7	12	15	V
V_{IN} Under Voltage Lockout Threshold, V_{IN} rising	V_{IN_UVH}	I_{OUT} = 0A	-	7.25	-	V
V_{IN} Under Voltage Lockout Threshold, V_{IN} falling [11]	V_{IN_UVL}	I_{OUT} = 0A	-	6.75	-	V
V_{IN} Current Supply, Full load	I_{IN_FULL}	V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 16A	-	2.7	-	A
V_{IN} Current Supply, Switching	I_{IN_SW}	V_{IN} = 12V, I_{OUT} = 0A	-	100	-	mA
V_{IN} Current Supply, Shutdown	I_{IN_SD}	V_{IN} = 12V, EN = 0V	-	1	-	mA
ENABLE INPUT (EN PIN)						
Threshold High	V_{TH_ENH}		2.15	-	3.6	V
Threshold Low	V_{TH_ENL}		-0.3	-	1.2	V
EN Pin Input current	I_{EN}	V_{IN} = 12V, EN =3.3V, I_{OUT} = 0A	-	10	-	µA
CONVERTER						
Efficiency	EFF	V_{IN} = 12.0V, V_{OUT} = 1.8V, I_{OUT} = 16A	-	91.8	-	%
		V_{IN} = 12.0V, V_{OUT} = 1.0V, I_{OUT} = 16A	-	87. 0	-	
Fixed Switching Frequency	F_{SW}		-	400	-	kHz
Start-up Time(Vin ON)	T_{START_UP}	V_{OUT} = 1.8V (V_{OUT} = 5% to 90% of V_{OUT})	-	2	-	ms
Start-up Time(Enable ON)		V_{OUT} = 1.8V (V_{OUT} = 5% to 90% of V_{OUT})	-	2	-	ms
POWER GOOD (PGOOD PIN) [4]						
PGOOD Sink Current	I_{S_PG}		-	-	5	mA
PGOOD Low Level Output Voltage	V_{L_PG}		-	-	1.0	V
PGOOD TRUE (HI)	V_{TH_PGH}		(V_{OSET} x 90%) < V_{OUT} < (Voset x 115%)			V
PGOOD FALSE (LO)	V_{TH_PGL}		Out of above range			V
OUTPUT						
Output Current [2]	I_{OUT}		0	-	16	A
Output Voltage [9]	V_{OUT}		0.7	-	1.8	V
Total Output Voltage Accuracy [7][14]	V_{OUT_ACC}		-3.0	-	+3.0	%
Line Regulation [15]	V_{OUT_LINE}	V_{IN} = min. to max.	-	±0.5	-	%
Load Regulation [15]	V_{OUT_LOAD}	I_{OUT} = min. to max.	-	±0.5	-	%
Temperature variation [15]	V_{OUT_TEMP}	$-40 \le T_A \le 105$degC	-	±1.5	-	%
Dynamic Load Peak Deviation [14]	V_{OUT_DYN}	V_{IN} = 12V, V_{OUT} = 1.0V, I_{OUT} = 50-100%	-	±3.0	-	%
Ripple and Noise (20MHz bandwidth) [6]	V_{RIP}		-	5	30	mV pk-pk
External Output Capacitance Range [10]	C_{OUT}		660	-	5000	µF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION						
Over Current Protection Threshold	I_{OCPTH}	HICUP operating (5)	-	24	-	A
Over Voltage Protection (12)	V_{OCPTH}			>120		% of V_{OUT}
Under Voltage Protection	V_{UVPTH}			<70		% of V_{OUT}
Thermal Protection (8)(13)	T_{OTPTH}	Shutdown operating	-	155	-	degC
Thermal Protection Hysteresis (8)(13)	T_{OTPHYS}		-	20	-	degC
ENVIRONMETAL						
Moisture Sensitivity Level				3		
Calculated MTBF (3)		T_A =40degC, V_{IN} = 12.0V, V_{OUT} = 1.8V, I_{OUT} = 50%	-	8.45x 10^6	-	hours

Notes

(1) Specifications are typical at +25degC, V_{IN}= 12.0V. (MYMGM1R816ELA5RN), V_{OUT} = 1.8V , full load, external caps and natural convection unless otherwise indicated. All models are tested and specified with external 220uF x 3 ceramic output capacitors, 22uF x 2 (for MYMGM1R816ELA5RN) ceramic and plenty electrolytic external input capacitors. All capacitors are low ESR types. These capacitors are necessary to accommodate our test equipment and may not be required to achieve specified performance in your applications. However, Murata recommends installation of these capacitors. Please refer the test circuit. Several parameters can be changed by PMBus™. (See PMBus™ register map)
(2) Note that Maximum Power Derating curves indicate an average current at typical input voltage. At higher temperatures and/or no airflow, the converter will tolerate brief full current outputs if the total RMS current over time does not exceed the Derating curve.
(3) Mean Time Between Failure is calculated using the Telcordia SR-332 method, +40degC, half output load, natural air convection.
(4) The EN Input should use either a switch or an open collector/open drain transistor referenced to GND. A logic gate may also be used by applying appropriate external voltages which do not exceed absolute maximum ratings.
(5) “Hiccup” overcurrent operation repeatedly attempts to restart the converter with a brief, full-current output. If the overcurrent condition still exists, the restart current will be removed and then tried again. This short current pulse prevents overheating and damaging the converter. Once the fault is removed, the converter immediately recovers normal operation.
(6) Output noise may be further reduced by adding an external filter. At zero output current, the output may contain low frequency components which exceed the ripple specification. The output may be operated indefinitely with no load.
(7) Regulation specifications describe the deviation as the line input voltage or output load current is varied from a midpoint value to either extreme.
(8) Thermal Protection/Shutdown temperature is measured with the sensor in the converter.
(9) Do not exceed maximum power specifications when adjusting the output trim.
(10) The maximum output capacitive loads depend on the Equivalent Series Resistance (ESR) of the external output capacitor and, to a lesser extent, the distance and series impedance to the load. Larger caps will reduce output noise but may change the transient response. Newer ceramic caps with very low ESR may require lower capacitor values to avoid instability. Thoroughly test your capacitors in the application.
(11) Do not allow the input voltage to degrade lower than the input under voltage shutdown voltage at all times. Otherwise, you risk having the converter turn off. The Under-voltage shutdown is not latching and will attempt to recover when the input is brought back into normal operating range.
(12) The outputs are intended to sink appreciable reverse current.
(13) When the temperature decreases below the turn-in threshold, the converter will automatically restart.
(14) About di/dt condition, please refer to the table described later.
(15) Ensured by design. Not production tested.

Typical Performance Characteristics

In this document, all characteristics are measured with the test board. The schematic and part list of the board are shown inFigure 25 andTable 11. The board is under T_A=25degC with no airflow unless otherwise noted.

V_{OUT} = 1.8V

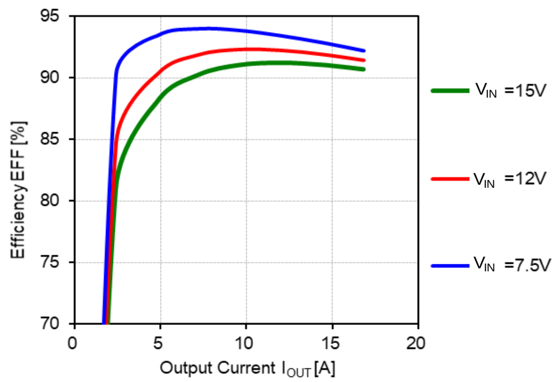


Figure 5. Efficiency vs. Load Current and Line Voltage

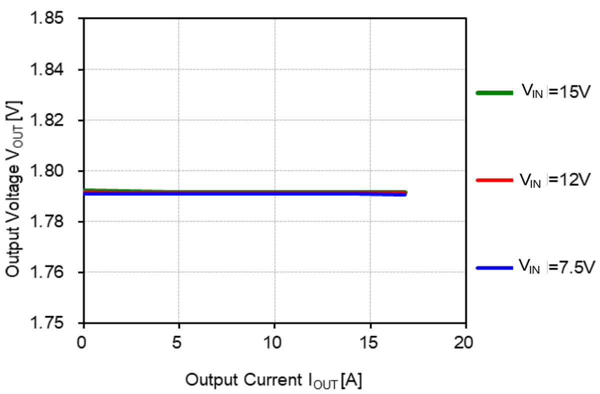
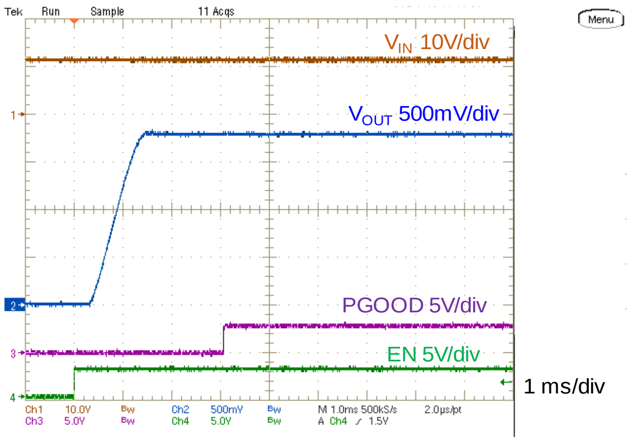
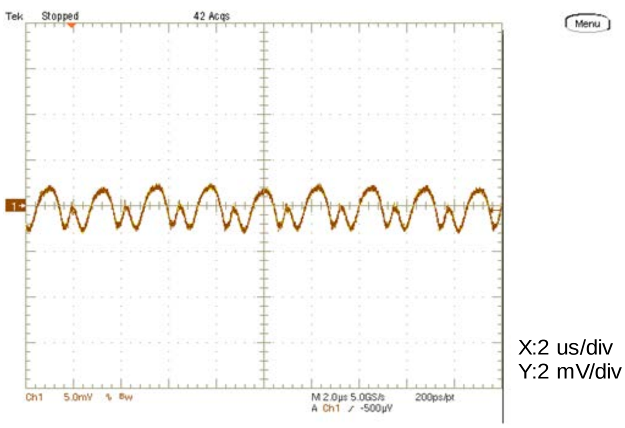


Figure 6. V_{OUT} vs. Load Current and Line Voltage



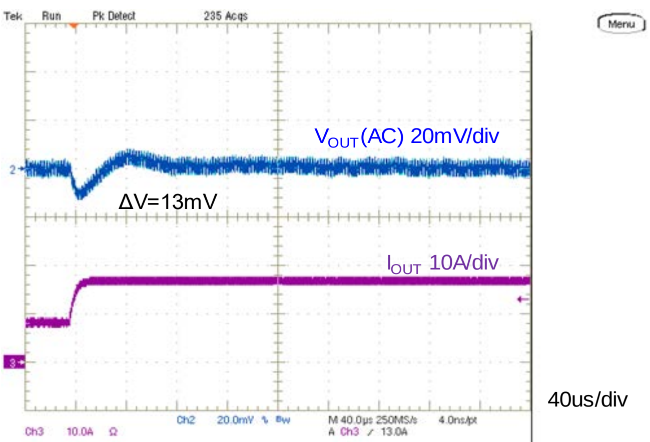
(V_{IN} = 12V, I_{OUT} = 16A)

Figure 7. On/Off Enable wave form



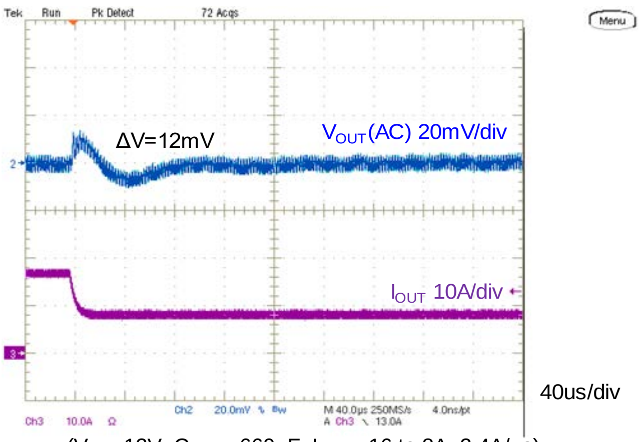
(V_{IN} = 12V, I_{OUT} = 16A, C_{OUT} = 660µF, ScopeBW = 20MHz)

Figure 8. Output Ripple and Noise



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 8 to 16A, 2.4A/µs)

Figure 9. Step Load Transient Response



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 16 to 8A, 2.4A/µs)

Figure 10. Step Load Transient Response

V_{OUT} = 1.0V

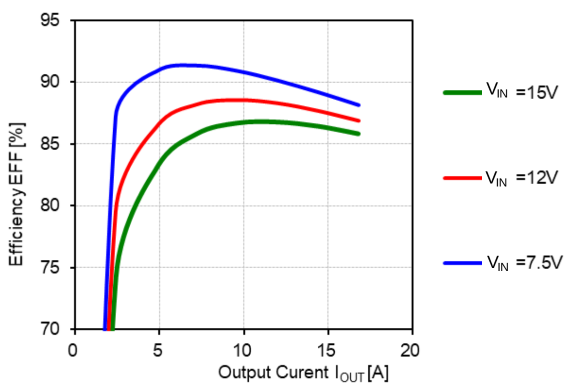


Figure11. Efficiency vs. Load Current and Line Voltage

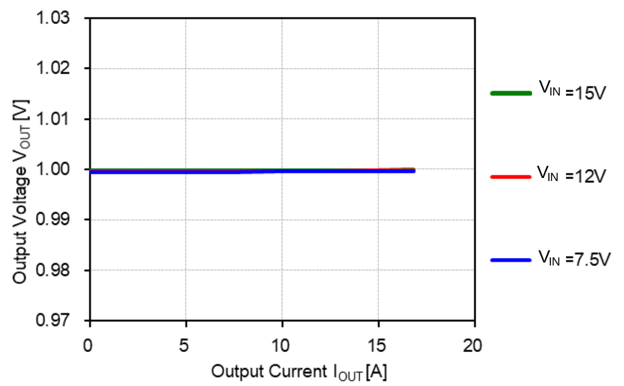
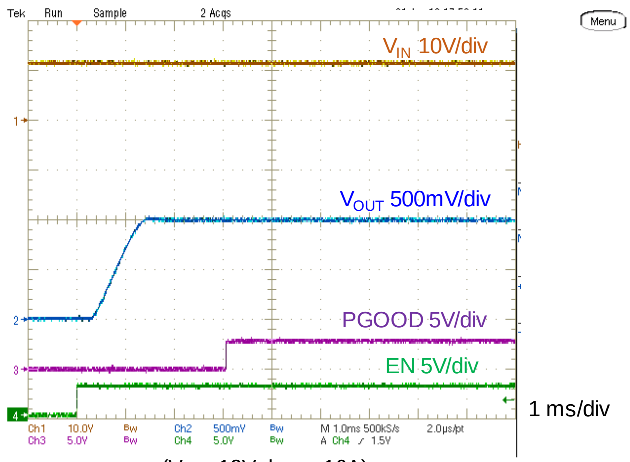
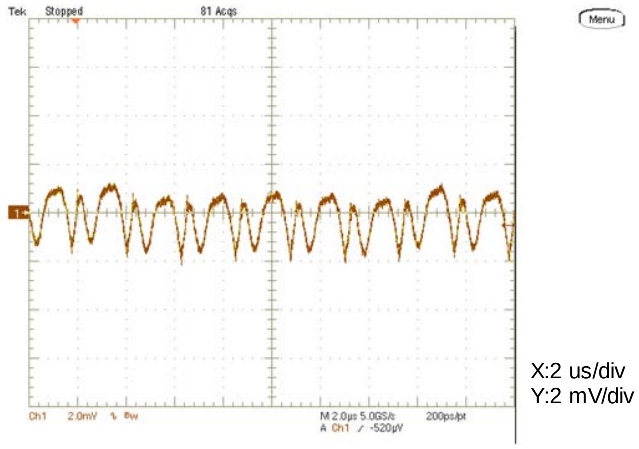


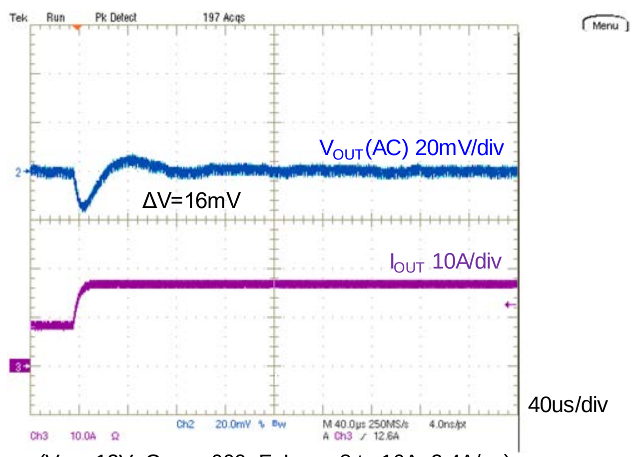
Figure12. V_{OUT} vs. Load Current and Line Voltage



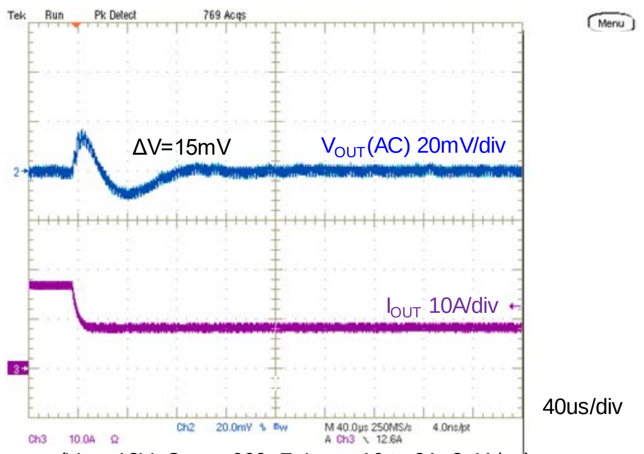
(V_{IN} = 12V, I_{OUT} = 16A)
Figure13. On/Off Enable wave form



(V_{IN} = 12V, I_{OUT} = 16A, C_{OUT} = 660µF, ScopeBW = 20MHz)
Figure14. Output Ripple and Noise



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 8 to 16A, 2.4A/µs)
Figure 15. Step Load Transient Response



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 16 to 8A, 2.4A/µs)
Figure 16. Step Load Transient Response

V_{OUT} = 0.7V

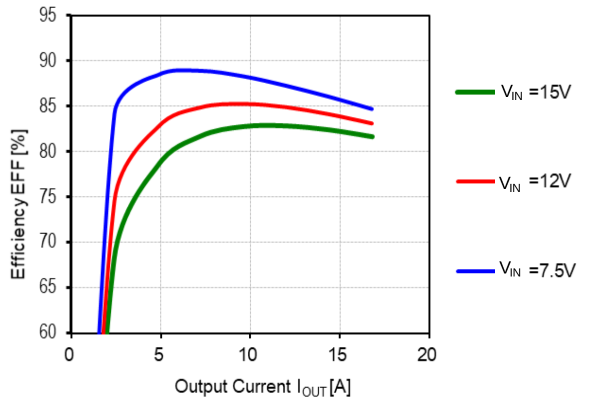


Figure17. Efficiency vs. Load Current and Line Voltage

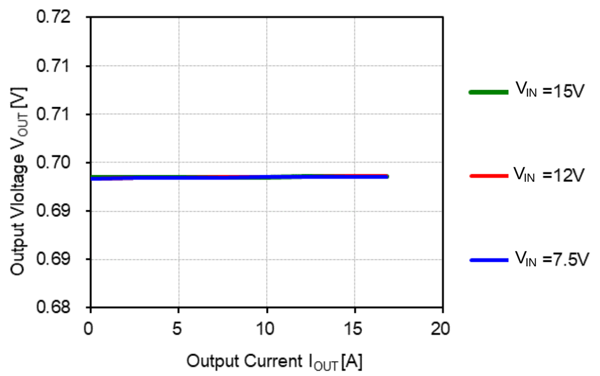
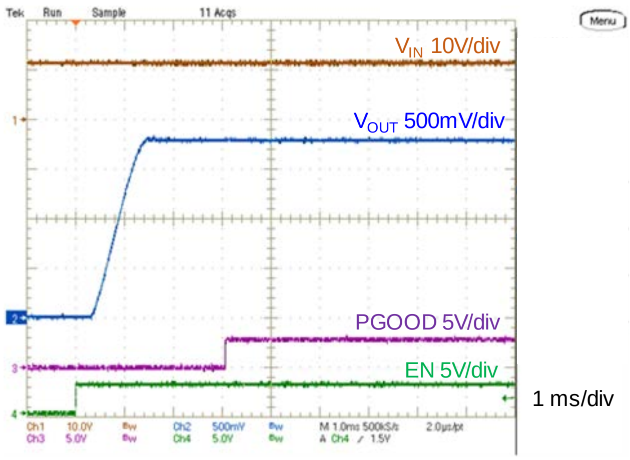
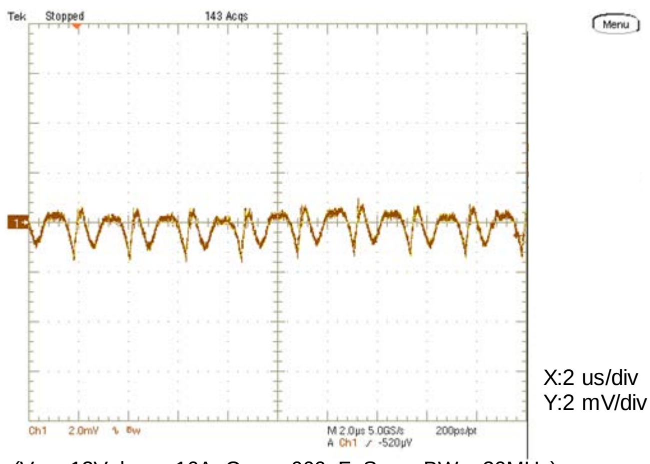


Figure 18. V_{OUT} vs. Load Current and Line Voltage



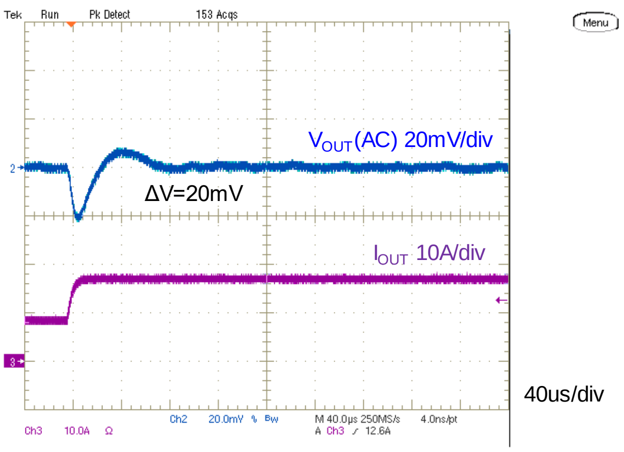
(V_{IN} = 12V, I_{OUT} = 16A)

Figure 19. On/Off Enable wave form



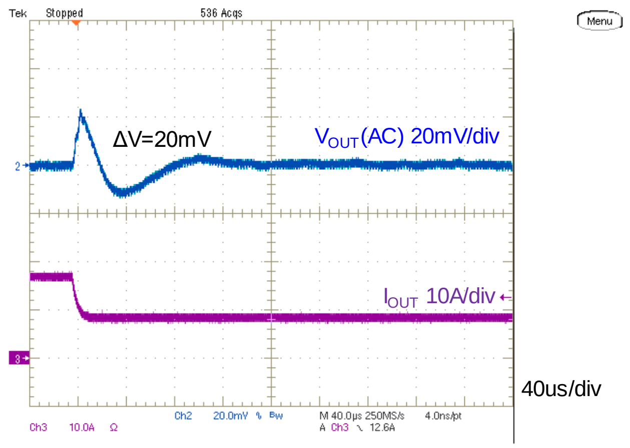
(V_{IN} = 12V, I_{OUT} = 16A, C_{OUT} = 660µF, ScopeBW = 20MHz)

Figure 20. Output Ripple and Noise



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 8 to 16A, 2.4A/µs)

Figure 21. Step Load Transient Response



(V_{IN} = 12V, C_{OUT} = 660µF, I_{OUT} = 16 to 8A, 2.4A/µs)

Figure 22. Step Load Transient Response

Thermal Deratings (Reference Data)

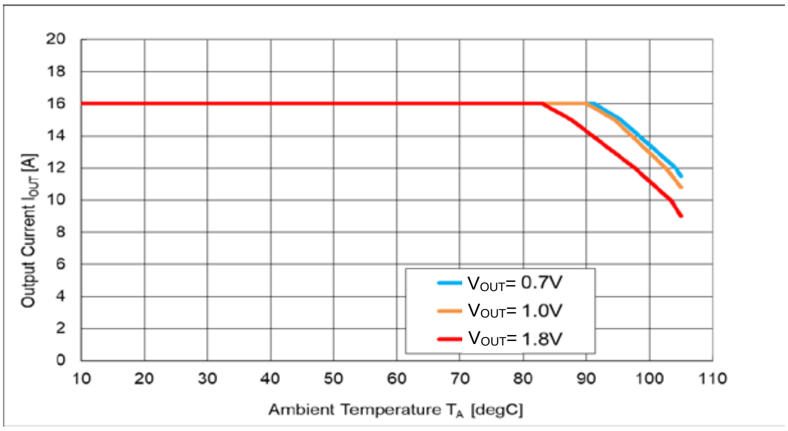


Figure 23. Safe Operating Area (V_{IN} = 12V)

Position : Center of the Module
Radius : 1mm

Figure 24. Temperature Measuring Area

Thermal deratings are evaluated in following condition.

・The product is mounted on 50.8mm x 60.0mm x 1.6mm (8 Layer, 2oz copper each) FR-4 board respectively.
・No forced air flows.

Surface (Top of the coil) temperature of the product : 110degC max

Transient Response Data

Transient response data at various conditions are showed in following table.
Minimum output capacitance can serve less than 3% x V_{OUT} of deviation for 8A load change(1A/us).

Table 10. Transient Response Data

V_{OUT}(V)	V_{IN}(V)	C_{OUT}(UF)	VOLTAGE DEVIATION(mV) 8-16A LOAD STEP (1A/us)
0.7	12	660	21
1			16
1.2			15
1.8			12

Test Circuit

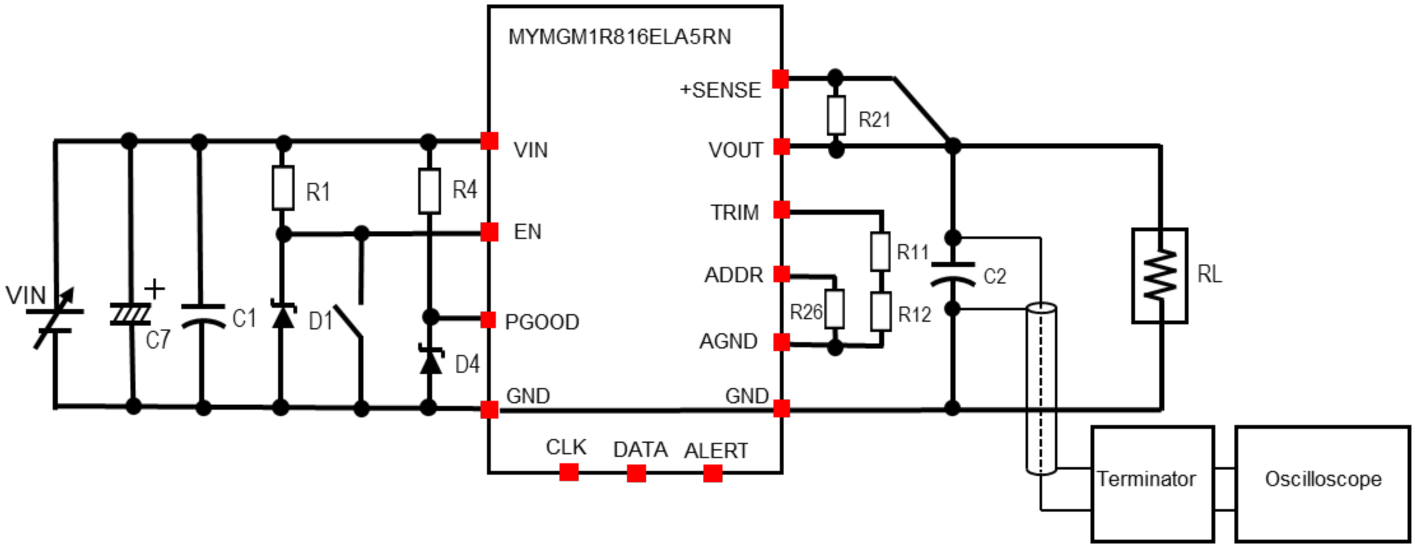


Figure 25. Test Circuit

*1: If there is a non-negligible parasitic impedance between the power supply and the converter, such as during evaluation, the optional input capacitor “C7” may be required to reduce the impedance. The recommended optional capacitor is an example. Please consider the optimum value for the case. This capacitor is usually an aluminum electrolytic type. It isn't necessary to place the capacitor near the input terminal of the converter.

*2: Do not connect any additional components between the TRIM pin and VOUT or between the TRIM and +SENSE pins. Use only the specified connections.

Table 11. Test Circuit Part List

REFERENCE	VALUE	DESCRIPTION	PART AND EQUIPMENT
C1	22uF/25V×2	Output Capacitor Ceramic capacitor, 22uF, 25V, +/-/10%, X7R	GRM32ER71E226KE15 (Murata)
C2	220uF/4V×3	Output Capacitor Ceramic capacitor, 220uF, 4V, +/-/20%, X7U	GRM32EC80G227ME05 (Murata)
R21	0 ohm	Chip resister	RK73Z1JTTD(KOA)
R11, R12	-	Chip resistor, 1/10W, +/-0.5% The value is determined by the target output voltage.	
R1, R4	10 kohm	Chip resistor, 1/10W, +/-5.0%	RK73B1JTTD103J (KOA)
R26	-	Chip resistor, 1/10W, +/-0.5% The value is determined by the target PMBus™ address.	
D1, D4	3.3V	Zenner Diode	EDZV3.3B (Rohm)
C7	1500uF/25V	Electrolysis Capacitor (Optinal)	
RL	-	Electronic Load Device	ELL-355(KeisokuGiken)
Oscilloscope	-	Digital Oscilloscope	DPO5034 or TDS5034(Tektronix)
Terminator	-	Terminator	TRC-50F2(KeisokuGiken)

Detailed Description

Input Under-Voltage Shutdown and Start-Up Threshold

Under normal start-up conditions, converters will not begin to regulate properly until the ramping-up input voltage exceeds and remains at the Start-Up Threshold Voltage (see Specifications). Once operating, converters will not turn off until the input voltage drops below the Under-Voltage Shutdown Limit. Subsequent restart will not occur until the input voltage rises again above the Start-Up Threshold. This built-in hysteresis prevents any unstable EN operation at a single input voltage.
Users should be aware however of input sources near the Under-Voltage Shutdown whose voltage decays as input current is consumed (such as capacitor inputs), the converter shuts off and then restarts as the external capacitor recharges. Such situations could oscillate. To prevent this, make sure the operating input voltage is well above the UV Shutdown voltage at all times.

Start-Up Time

Assuming that the output current is set at the rated maximum, the V_{IN} to V_{OUT} Start-Up Time (see Specifications) is the time interval between the point when the ramping input voltage crosses the Start-Up Threshold and the fully loaded regulated output voltage enters and remains within its specified accuracy band. Actual measured times will vary with input source impedance, external input capacitance, input voltage slew rate and final value of the input voltage as it appears at the converter.
This converter includes a soft start circuit to moderate the duty cycle of its PWM controller at power up, thereby limiting the input inrush current.
The EN Remote Control interval from ON command to VOUT regulated assumes that the converter already has its input voltage stabilized above the Start-Up Threshold before the ON command. The interval is measured from the ON command until the output enters and remains within its specified accuracy band. The specification assumes that the output is fully loaded at maximum rated current. Similar conditions apply to the On to V_{OUT} regulated specification such as external load capacitance and soft start circuitry.

Output Noise

This converter is tested and specified for output noise using designated external output components, circuits and layout as shown in the figures below. In the figure below, the two copper strips simulate real-world printed circuit impedances between the power supply and its load. In order to minimize circuit errors and standardize tests between units, scope measurements should be made using BNC connectors or the probe ground should not exceed one half inch and soldered directly to the test circuit.

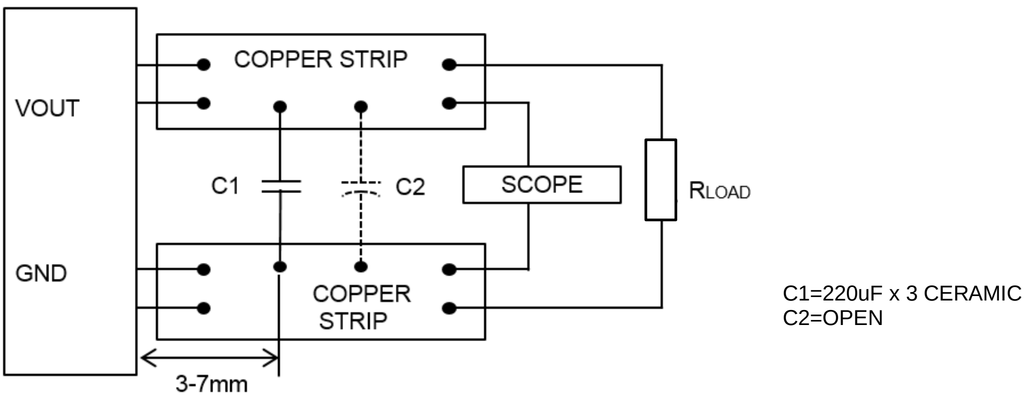


Figure 26. Circuits and Layout

Minimum Output Loading Requirements

This converter regulates within specification and are stable under no load to full load conditions. Operation under no load might however slightly increase output ripple and noise.

Thermal Shutdown

To prevent many over temperature problems and damage, these converters include thermal shutdown circuitry. If environmental conditions cause the temperature of the Converter's to rise above the Operating Temperature Range up to the shutdown temperature, an on-board electronic temperature sensor will shut down the unit. When the temperature decreases below the turn-on threshold, the converter will automatically restart.
CAUTION: If you operate too close to the thermal limits, the converter may shut down suddenly without warning. Be sure to thoroughly you're your application to avoid unplanned thermal shutdown.

Temperature Derating Curves

The graph in this data sheet illustrates typical operation under a variety of conditions. The derating curves show the maximum continuous ambient air temperature. Note that these are AVERAGE measurements.
Note that the temperatures are of the ambient airflow, not the converter itself which is obviously running at higher temperature than the outside air. Also note that very low flow rates (below about 25 LFM) are similar to "natural convection," that is, not using fan-forced airflow. Murata makes Characterization measurements in a closed cycle wind tunnel with calibrated airflow. We use both thermocouples and an infrared camera system to observe thermal performance.
CAUTION: This graph is collected at slightly above Sea Level altitude. Be sure to reduce the derating for higher density altitude.

Output Current Limiting

Current limiting inception is defined as the point at which full power falls below the rated tolerance. See the Performance/Functional Specifications. Note particularly that the output current may briefly rise above its rated value in normal operation as long as the average output power is not exceeded. This enhances reliability and continued operation of your application. If the output current is too high, the converter will enter the short circuit condition.

Output Short Circuit Condition

When a converter is in current-limit mode, the output voltage will drop as the output current demand increases. Following a time-out period, the converter will restart, causing the output voltage to begin ramping up to its appropriate value. If the short-circuit condition persists, another shutdown cycle will initiate. This rapid on/off cycling is called "hiccup mode". The hiccup cycling reduces the average output current, thereby preventing excessive internal temperatures and/or component damage. A short circuit can be tolerated indefinitely.
The "hiccup" system differs from older latching short circuit systems because you do not have to power down the converter to make it restart. The system will automatically restore operation as soon as the short circuit condition is removed.

Power Good (PGOOD)

Please refer to the Connection Diagram on page 1 for PGOOD connection.
The Product has a power good (PGOOD) output. PGOOD is the open drain of a MOSFET. Connect PGOOD to Vin or another external voltage source less than 3.6V through a pull-up resistor. After applying the input voltage, the module turns on so that PGOOD is pulled to GND before the soft start is ready. After the Trimming voltage reaches the threshold set internally, PGOOD is pulled high after a delay.
When the converter encounters any fault (e.g.: UV, OV, OT, UVLO, etc.), PGOOD is latched low and cannot be pulled high again until a new soft start is initialized.

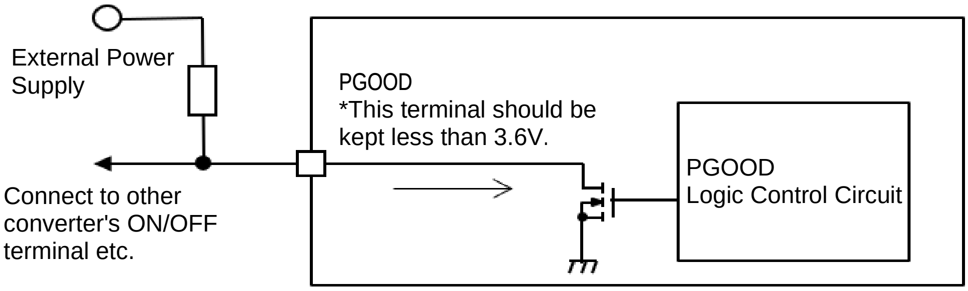


Figure 27. PGOOD Internal Circuit Diagram

PMBus™ Alert (ALT#)

ALT# is active low. A pull-up resistor connected to 3.3V is required if the ALT# function is needed.
If any PMBus™ warnings appears, this terminal turn to High.
The CLEAR_FAULTS command is used to reset all stored warning and fault flags.
See, Clear Faults command and any Warning commands, if need.

UVP/OVP Function

This product monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, after 1ms, the product turns OFF. The converter restarts after a hiccup delay (about 16ms). This function is enabled 1.5ms after the soft-start is completed.
When the feedback voltage becomes higher than 120% of the target voltage, the circuit operates sink-mode to decrease output voltage. If the output voltage reaches UV threshold, the device restarts after a hiccup delay. If the OV condition remains, the converter will not start until the OV condition is removed.

Enable (EN)

Please refer to the Connection Diagram on page 1 for EN connection.
This converter is enabled when the EN pin is pulled high with respect to GND. This device is disabled when the EN pin is grounded or brought to within a low voltage (see Specifications) with respect to GND.
The ON/OFF function and operation are also controlled by using PMBus™ command OPERATION (01h) and ON_OFF_CONFIG (02h)
as below.
Dynamic control of the ON/OFF function should be able to sink appropriate signal current when brought low and withstand appropriate voltage when brought high. Be aware too that there is a finite time in milliseconds (see Specifications) between the time of ON/OFF Control activation and stable, regulated output. This time will vary slightly with output load type and current and input conditions.

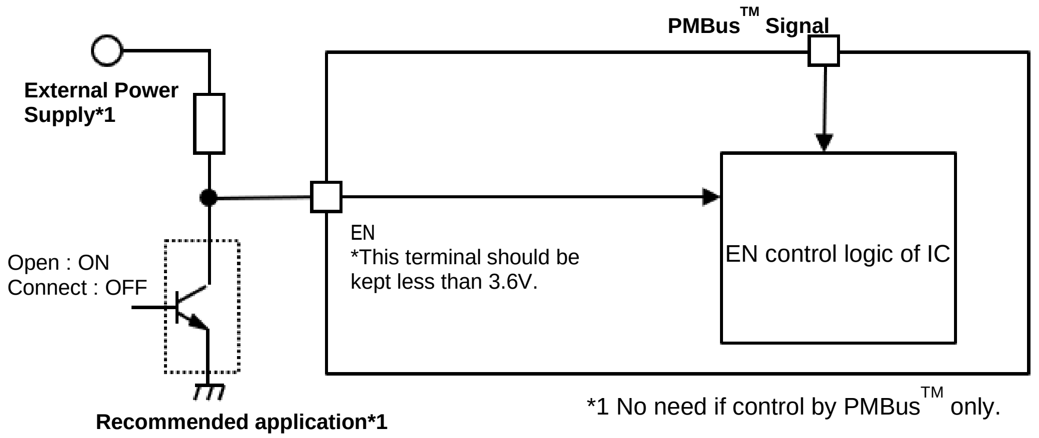


Figure 28. EN Internal Circuit Diagram

Table 12. ON/OFF Control

OUTPUT	OPERATION(01h) ON/OFF bit	ON_OFF_CONFIG (02h)	EN PIN
ON	ignore	16h(Default)	H
OFF			L
ON	ON	1Ah	ignore
OFF	OFF		
ON	ON	1Eh	H
OFF	OFF		L
OFF	OFF		H
OFF	ON		L
OFF	Ignore	12h	Ignore
ON	ignore	0xh	ignore

Output Capacitive Load

Users should only consider adding capacitance to reduce switching noise and/or to handle spike current load steps. Install only enough capacitance to achieve noise objectives. Excess external capacitance may cause regulation problems, degraded transient response and possible oscillation or instability.

Output Voltage Adjustment

Caution
This converter can be changed output voltage by external resister only.

This product provides output voltage monitoring through the register of READ_VOUT (8Bh). In order to have correct output voltage setting and monitoring, the external voltage divider (Rtrim) and the registers of VOUT_COMMAND (21h), VOUT_MARGIN_HIGH (25h), VOUT_MARGIN_LOW (26h), VOUT_SCALE_LOOP (29h) should be set correspondingly. The following shows how to set the output voltage.

1. Determin the Rtrim value using following formula.
    Rtrim (kohm) = 6 /(V_{OUT} - 0.6)
Then, connect an external trim resistor (Rtrim) between the TRIM pin and GND pin. The Rtrim resistor must be a 1/10W precision metal film type, ±0.5% accuracy or better with low temperature coefficient, ±100 ppm/degC.

2.Set the VOUT_COMMAND (21h) and the VOUT_SCALE_LOOP(29h) as follows.
VOUT_COMMAND: Target Voltage in hexadecimal (Least Significant Bit is 0.002V)
VOUT_SCALE_LOOP: Set following value in hexadecimal
VOUT_SCALE_VALUE= 0.6/Target V_{OUT} (Least Significant Bit is 0.001)

3.Set VOUT_MARGIN_HIGH (25h), VOUT_MARGIN_LOW (26h) as follows.
VOUT_MARGIN_HIGH (25h): VOUT margin (high) voltage in hexadecimal.(Should be set in the range of 100~110% of target VOUT)
VOUT_MARGIN_LOW (26h): VOUT margin (low) voltage in hexadecimal. (Should be set in the range of 90~100% of target VOUT) (Least Significant Bit is 0.002V respectively)
The following table shows the Rtrim and PMBus™ parameters at particular V_{OUT} for example.

Table 13. Rtim Calculation and PMBus™ Parameter Example

V_{OUT} [V]	ESTIMATED RTRIM [kohm]	PMBus™ COMMAND PARAMETERS			
		21h	29h	25h	26h
0.7	30+30	0x015E (0.7V)	0x0359 (0.857)	0x0181 (0.77V)	0x013B (0.63V)
1.0	15	0x01F4 (1.0V)	0x0258 (0.600)	0x0226 (1.1V)	0x01C2 (0.9V)
1.2	10	0x0258 (1.2V)	0x01F4 (0.500)	0x0294 (1.32V)	0x021C (1.08V)
1.5	4.7+2.0.	0x02EE (1.5V)	0x0190 (0.400)	0x0339 (1.65V)	0x02A3 (1.35V)
1.8	4.7+0.3	0x0384 (1.8V)	0x014D (0.333)	0x03DE (1.98V)	0x032A (1.62V)

CAUTION
It's not recommended to change PMBus™ parameters when the power stage is enabled. Proper operation of the converter is not guaranteed to do so.
Do not exceed the specified limits of the output voltage or the converter's maximum power rating when applying these resistors.

Output Voltage Remote Sense

This function is capable to compensate up the voltage drop between the output and input of load. The sense range depend on the maximum voltage allowing on the VOUT pin. The sense trace should be short as possible and shielded by GND line or else to reduce noise susceptibility. The sense line length is recommended within 10cm for output voltage stability. If the remote sense is not needed, +SENSE pin should be connected to VOUT pin.

PMBus™ Serial Interface Description

The Power Management Bus (PMBus™) is an open-standard, power-management protocol that defines a means of communication with power conversion and other devices.
The PMBus™ is a two-wire, bidirectional, serial interface, consisting of a data line (DATA) and a clock line (CLK). The lines are externally pulled to a bus voltage when they are idle. When connecting to the lines, a master device generates the SCL signal and device address and arranges the communication sequence. This is based on the I²C operation principles. This product is a PMBus™ slave which supports both the standard mode (100kHz) and fast modes (400kHz). The PMBus™ interface adds flexibility to the power supply solution.

Multi Address

To support multiple devices used on the same PMBus™, use the ADDR pin to program the different address for each device.
To determine by external resistor, connect a resistor between ADDR pin and AGND to set the ADDR voltage. The internal ADC converts the pin voltage to set the PMBus™ address. Maximum 16 addresses can be set by ADDR pin. Following table shows the PMBus™ address for different resistor values from ADDR pin to AGND.

Table 14 . PMBus™ Address Setting Resistor

R ADDR-GND [kohm]	ADDRESS
4.99	30h
15	31h
24.9	32h
34.8	33h
45.3	34h
54.9	35h
64.9	36h
75	37h
84.5	38h
95.3	39h
105	3Ah
115	3Bh
124	3Ch
133	3Dh
147	3Eh
154	3Fh

Start and Stop Conditions

The start and stop are signaled by the master device which signifies the beginning and the end of the PMBus™ transfer.
The start condition is defined as the SDA signal transitioning from high to low while the SCL is high.
The STOP condition is defined as the SDA signal transitioning from low to high while the SCL is high as shown in Figure 29.
The master then generates the SCL clocks, and transmits the device address and the read/write direction bit r/w on the SDA line. Data is transferred in 8-bit bytes by SDA line. Each byte of data is to be followed by an acknowledge bit.

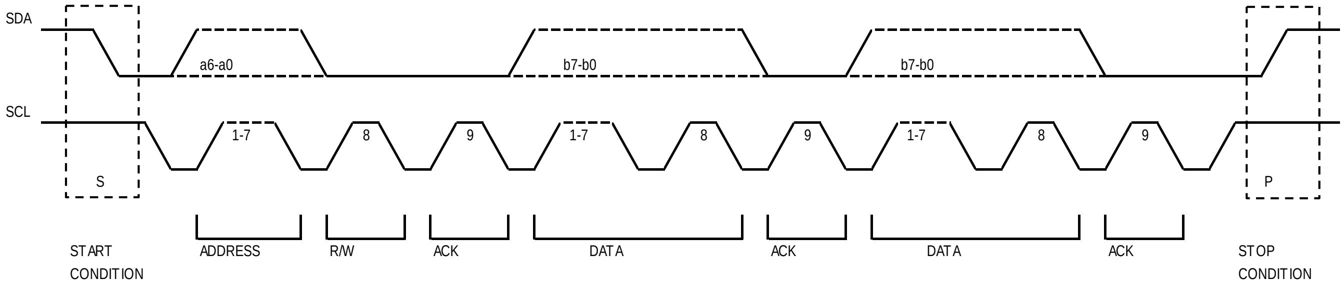


Figure 29. Start and Stop Conditions

PMBus™ Update Sequence

This product requires a start condition, a valid PMBus™ address, a register address byte, and a data byte for a single data update.
The product acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus™ address selects the product.
The product performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus™ transactions on device are done using defined bus protocols.
The following protocols are implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus™ Bus message format

In the tables in Figure B, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the device is driving the bus.
S = start condition
Sr = repeated start condition
P = stop condition
R = read bit
W= write bit
A = acknowledge bit (0)
A#= acknowledge bit (1)
"A" represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a logic 1, indicated by A#.

Packet Error Checking (PEC)

The device PMBus™ interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the device during a read transaction or sent by the bus host to the device during a write transaction.
The PEC byte is used by the bus host or the device to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the device determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the device.

PMBus™ Alert Response Address (ARA)

The PMBus™ alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to it. A host typically uses a hardware interrupt pin to monitor the PMBus™ ALERT pins of a number of devices. When a host interruption occurs, the host issues a message on the bus using the PMBus™ receive byte or receive byte with PEC protocol. The special address used by the host is 0x0C.
Any devices that have a PMBus™ alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0.
The host reads the device address from the received data byte and proceeds to handle the alert condition. More than one device may have an active PMBus™ alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus™ alert signal. If the host sees that the PMBus™ alert signal is still low, it continues to read addresses until all devices that need to talk to it have successfully transmitted their addresses.

Data and Numerical Formats

The device uses a direct format internally to represent real-world values such as voltage, current, power and temperature. All numbers with no suffix in this document are decimals unless explicitly designated otherwise. Numbers in binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 5’b01010 indicates a 5-bit binary data, and the data is 01010. The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document. The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus™ Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several types of the data transmission faults as listed below:
- Sending too few data
- Reading too few data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus™ Reporting and Status Monitoring

The device supports real-time monitoring for some operation parameters and status with PMBus™ interface. They are listed on following table.

Communication Pattern

a) Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	PEC	A	P

b) Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

c) Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P

d) Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

e) Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

f) Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	A	P

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	8	1	1
Data Byte High	A	PEC	A	P

g) Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count =N	A	···

8	1	8	1		8	1	1
Data Byte 1	A	Data Byte 2	A	···	Data Byte N	A	P

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count =N	A	···

8	1	8	1		8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	···	Data Byte N	A	PEC	A	P

PMBus™ Register Map

Table 15. PMbus™ command list

CODE	COMMAND NAME	TYPE	DEFAULT VALUE (HEX)	DEFAULT VALUE (Actual)
01h	OPERATION	R/W w/PEC	0x80	-
02h	ON_OFF_CONFIG	R/W w/PEC	0x16	-
03h	CLEAR_FAULTS	Send byte w/PEC	-	-
10h	WRITE_PROTECT	R/W w/PEC	0x00	-
19h	CAPABILITY	R w/PEC	0xB0	-
20h	VOUT_MODE	R w/PEC	0x40	-
21h	VOUT_COMMAND	R/W w/PEC	0x015E	0.7V
25h	VOUT_MARGIN_HIGH	R/W w/PEC	0x0181	0.77V
26h	VOUT_MARGIN_LOW	R/W w/PEC	0x013B	0.63V
29h	VOUT_SCALE_LOOP	R/W w/PEC	0x0359	0.857
35h	VIN_ON	R/W w/PEC	0x001D	7.25V
36h	VIN_OFF	R/W w/PEC	0x001B	6.75V
4Ah	IOUT_OC_WARN_LIMIT	R/W w/PEC	0x0050	19.36A
51h	OT_WARN_LIMIT	R/W w/PEC	0x0091	145degC
57h	VIN_OV_WARN_LIMIT	R/W w/PEC	0x0020	16V
58h	VIN_UV_WARN_LIMIT	R/W w/PEC	0x001C	7V
60h	TON_DELAY	R/W w/PEC	0x0000	0ms
61h	TON_RISE	R/W w/PEC	0x0001	2ms
78h	STATUS_BYTE	R/W w/PEC	-	-
79h	STATUS_WORD	R/W w/PEC	-	-
7Ah	STATUS_VOUT	R/W w/PEC	-	-
7Bh	STATUS_IOUT	R/W w/PEC	-	-
7Ch	STATUS_INPUT	R/W w/PEC	-	-
7Dh	STATUS_TEMPERATURE	R/W w/PEC	-	-
7Eh	STATUS_CML	R/W w/PEC	-	-
88h	READ_VIN	R w/PEC	-	-
8Bh	READ_VOUT	R w/PEC	-	-
8Ch	READ_IOUT	R w/PEC	-	-
8Dh	READ_TEMPERATURE_1	R w/PEC	-	-
98h	PMBus™_REVISION	R/W w/PEC	-	-
D1h	MFR_CTRL_VOUT	R/W w/PEC	0x00	-
D3h	MFR_ADDR_PMBus™	R/W w/PEC	0x00	-

OPERATION (01h)
The OPERATION command turns the converter output on or off in conjunction with the input from the CTRL pin. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit remains in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CTRL pin instructs the converter to change to another mode. This OPERATION command is also used to re-enable the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown will not clear the fault registers.

Table 16. OPERATION command

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0-
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	-	-	-	-	-	-	x	x
Default Value	1	0	0	0	0	0	x	x

Table 17. The details of each bit of the command 01h.

Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]	ON/OFF	MARGIN STATE	01h
00	xx	xx	xx	Immediate Off	N/A	0x00
01	xx	xx	xx	Immediate Off	N/A	0x60
10	00	xx	xx	On	Off	0x80
10	01	01	xx	On	Margin low (ignore fault)	0x94
10	01	10	xx	On	Margin low (act on fault)	0x98
10	10	01	xx	On	Margin high (ignore fault)	0xA4
10	10	10	xx	On	Margin high (act on fault)	0xA8

ON_OFF_CONFIG (02h)
The ON_OFF_CONFIG command configures the combination of the CTRL input and the PMBus™ commands to turn the converter on and off. This includes how the converter responds when an input voltage is applied.

Table 18. ON_OFF_CONFIG

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0-
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	x	x	x	on	op	ctrl	x	delay
Default Value	0	0	0	1	0	1	1	0

on
This on bit sets the default to either operate whenever the input voltage is present or for the on/off to be controlled by CTRL and PMBus™ commands.

Table 19. on Bit

Bit[4] VALUE	MEANING
0	Converter powers up whenever the input voltage is present regardless of state of the CTRL pin
1	Converter does not power up until commanded by the CTRL pin and OPERATION command (as programmed in Bits[3:0]

op
This op bit controls how the converter responds to the OPERATION commends.

Table 20. op Bit

Bit[3] VALUE	MEANING
0	Converter ignores the "on" bit in the OPERATION command from PMBus™
1	Converter responds the "on" bit in the OPERATION command from PMBus™

crtl
This ctrl bit controls how the converter responds to the CTRL pin.

Table 21. ctrl Bit

Bit[2] VALUE	MEANING
0	Converter ignores the CTRL pin (on/off controlled only by the OPERATION command)
1	Converter requires the CTRL pin to be asserted to power up. Depending on Bit[3] op bit, the OPERATION command may also be required to instruct the converter to power up.

delay
This delay bit sets the turn-off action when the converter is commanded off through the PMBus™. This bit is read only and cannot be modified by the end user.

Table 22. delay Bit

Bit[0] VALUE	MEANING
0	TOFF_DELAY, TOFF_FALL

CLEAR_FAULTS (03h)
The CLEAR_FAULTS command is used to reset all stored warning and fault flags. If a fault or warning condition still remains when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared or is reasserted almost immediately. Issuing a CLEAR_FAULTS command will not cause the converter to restart in the event of a fault turn-off. The converter restart must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus™ to send the byte protocol.

WRITE PROTECT (10h)
The WRITE_PROTECT command is used to control writes to the converter. This command provides protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the converter's configuration or operation.
All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Table 23. WRITE_PROTECT command

Bit[7:0] VALUE								MEANING
0	0	0	0	0	0	0	0	Enable writes to all commands.
0	0	1	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands.
0	1	0	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands.
1	0	0	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT command.

CAPABILITY (19h)
The CAPABILITY command returns information about the PMBus™ functions supported by this product. This command is read with the PMBus™ read byte protocol.

Table 24. CAPABILITY command

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0-
Access	r	r	r	r	r	r	r	r
Function	PEC	MAX bus speed		Alert	x	x	x	x
Default Value	1	0	1	1	0	0	0	0

Table 25. The details of each bit of the command 10h.

Bit[6:5] VALUE		MEANING
0	0	Maximum supported bus speed is 100KHz.
0	1	Maximum supported bus speed is 400KHz.
1	1	Reserved
1	0	Not supported

VOUT_MODE (20h)
The VOUT_MODE command is used to command and read the output voltage. The three most significant bits are used to determine the data format (only direct format is supported in this product), and the rest of five bits represent the exponent used in the output voltage Read/Write commands. The default value of 20h is 0x40.

VOUT_COMMAND (21h)

The VOUT_COMMAND sets the output voltage to read output voltage correctly. The VOUT_COMMAND and VOUT_SCALE_LOOP together determine the feedback reference voltage: VOUT_COMMAND x VOUT_SCALE_LOOP. In the section of “Output Voltage Setting” on Table13, it shows the details about how to set this command.
The value is unsigned and 1LSB = 2mV. The default value of 21h is 0x015E, which is 0.7V.

Table 26. VOUT_COMMAND

Command	VOUT_COMMAND															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0

VOUT_MARGIN_HIGH (25h)

Table 27. VOUT_MARGIN_HIGH

Command	VOUT_MARGIN_HIGH															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1

The value is unsigned and 1LSB = 2mV. The default value is 0.77V. So the default value of 25h is 0x0181.

VOUT_MARGIN_LOW (26h)

Table 28. VOUT_MARGIN_LOW

Command	VOUT_MARGIN_LOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	1

The value is unsigned and 1LSB = 2mV. The default value is 0.63V. So the default value of 26h is 0x013B.

VOUT_SCALE_LOOP (29h)

VOUT_SCALE_LOOP sets the feedback resistor divider ratio and is equal to VFB/VOUT. Regardless of whether an external or internal feedback resistor divider is used, VOUT_SCALE_LOOP should match the actual feedback resistor divider used.

Table 29. VOUT_SCALE_LOOP

Command	VOUT_SCALE_LOOP															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				0.001mV/LSB											
Default Value	0	0	0	0	0	0	1	1	0	1	0	1	1	0	0	1

The value is unsigned and 1LSB =0.001. The default value is 0.857. So the default value of 29h is 0x0359.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage, (in V), at which the converter should start to run if all other required power-up conditions are met. The VIN_ON value can be set between 7.25V and 15V with 0.25V increment. The VIN_ON value should be always set higher than VIN_OFF value with enough margin, so that there will be no bouncing between VIN_ON and VIN_OFF during power conversion.

Table 30. VIN ON

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

The value is unsigned and 1LSB=250mV. The default value is 7.25V. So the default value of 35h is 0x001D.

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage, (in V), at which the converter, once operation has started, should stop power conversion. The VIN_OFF value can be set between 6.75V and 15V with 0.25V increment. The VIN_OFF value should be always set lower than VIN_ON value with enough margin, so that there is no bouncing between VIN_OFF and VIN_ON during power conversion.

Table 31. VIN OFF

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

The value is unsigned and 1 LSB=250mV. The default value is 6.75V. So the default value of 36h is 0x001B.

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command is used to configure or read the threshold for the over-current warning detection. If the sensed current exceeds this value, the OC warning flags are set in the STATUS BYTE (78h), STATUS_WORD (79h) respectively, and the ALT# signal is asserted.

Table 32. IOUT_OC_WARN_LIMIT

Command	IOUT_OC_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															
Default Value	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

The value is unsigned and 1LSB=242mA. The default value is 0050h. The corresponding value of the total output current is about 19.4A.

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT is used to configure or read the threshold for the over-temperature warning detection. If the sensed temperature exceeds this value, an over temperature warning is triggered, the OT warning flags are set in the STATUS BYTE(78h) and STATUS_WORD(79h) respectively, and the ALT# signal is asserted. The minimum temperature warning detection time should be smaller than 20ms.

Table 33. OT_WARN_LIMIT

Command	IOUT_OC_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x								1degC/LSB							
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

The value is unsigned and 1LSB=1 degC. The default value is 0x0091h. The corresponding value is 145degC. The OT_WARN_LIMIT setting value should be lower than 155degC.

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command is used to configure or read the threshold for the input-over-voltage warning detection. If the measured value of VIN rises above the value in this register, VIN OV warning flags are set in the respective registers, and the ALT# signal is asserted.

Table 34. VIN_OV_WARN_LIMIT

Command	VIN_OV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				500mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

The value is unsigned and 1LSB=500mV. The default value is 0x20. The corresponding value is 16V. The VIN_OV_WARN_LIMIT setting value should not be higher than 16V.

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command is used to configure or read the threshold for the input-under-voltage warning detection. If the measured value of VIN falls below the value in this register, VIN UV warning flags are set in the respective registers, and the ALT# signal is asserted.

Table 35. VIN_UV_WARN_LIMIT

Command	VIN_UV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

The value is unsigned and 1LSB=250mV. The default value is 0x1C. The corresponding value is 7.0V. The VIN_UV_WARN_LIMIT setting value should be higher than 7.0V.

TON_DELAY (60h)

The TON_DELAY command sets the time, (in ms), from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Table 36. TON_DELAY

Command	TON_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x					4ms/LSB										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB=4ms. The maximum value is 60h=0x0100 (1024ms). The default value is 0x0000 (0ms).

TON_RISE (61h)

The TON_RISE command sets the soft-start time, (in ms), from when the output starts to rise until the voltage has reached the regulation point.

Table 37. TON_RISE

Command	TON_RISE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The only supported values are as follows:
3'b000: 1ms
3'b001: 2ms
3'b010: 4ms
3'b011: 8ms
3'b100 and up: 16ms.
The default value is 0x0001, i.e. 2ms for soft-start time.

STATUS BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of this product. Accesses to this command should use the read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 38. STATUS_BYTE

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[7]	Reserved	-	0	Always read as 0.
[6]	OFF	Live	0	0: product enabled. 1: product disabled, this can be from: the OC fault, the OT fault, the bad MOSFET fault, the UV/OV fault, or the OPERATION command turning off.
[5]	VOUT_OV	-	0	An output over voltage fault has occurred.
[4]	IOUT_OC_FAULT	Latched	0	0: no over current fault detected. 1: over current fault detected.
[3]	VIN_UV	-	0	Not supported, always read as 0.
[2]	OT_FAULT_WARN	Live	0	0: no over temperature warning or fault detected. 1: over temperature warning or fault detected.
[1]	CUMM_ERROR	Latched	0	0: no communication error detected. 1: communication error detected.
[0]	NONE_OF_THE_ABOVE	Live	0	0: no other fault or warning. 1: fault or warning not listed in bits [7:1] has occurred.

STATUS WORD (79h)

The STATUS_WORD returns the value of a number of flags indicating the state of this product. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 39. STATUS_WORD

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[15]	VOUT_STATUS	Live	0	0: no output fault or warning. 1: output fault or warning.
[14]	IOUT_STATUS	Live	0	0: no IOUT fault. 1: IOUT fault.
[13]	VIN_STATUS	Live	0	0: no VIN fault. 1: VIN fault, at the period when VIN starts up, the initial flag is 1 before VIN pass UVLO threshold. The flag cleared once VIN passes UVLO.
[12]	MFR_STATUS	-	0	Always read as 0.
[11]	POWER_GOOD#	Live	0	0: power good signal is asserted. 1: power good signal is not asserted.
[10]	Reserved		0	Always read as 0.
[9]	Reserved		0	Always read as 0.
[8]	UNKNOWN	Latched	0	0: no any other fault has occurred. 1: a fault type not specified in bits [15:1] of the STATUS_WORD has been detected.
Low byte	STATUS_BYTE	-	-	STATUS BYTE is the low byte of the STATUS_WORD.

STATUS_ VOUT (7Ah)

The STATUS_VOUT command returns one data byte with contents as follows:

Table 40. STATUS_VOUT

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[7]	VOUT_OV_FAULT	Live	0	0: no output OV fault.
[6]	Reserved	Latched	0	Always read as 0.
[5]	Reserved	Latched	0	Always read as 0.
[4]	IOUT_UV_FAULT	Live	0	0: no output UV fault. 1: output UV fault.
[3]	VOUT_MAX_MIN	Live	0	0: no VOUT_MAX, VOUT_MIN warning. 1: an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command or lower than the limit allowed by the VOUT_MIN command.
[2]	Reserved	-	0	Always read as 0.
[1]	Reserved	-	0	Always read as 0.
[0]	UNKNOWN	Latched	0	0: no any other fault has occurred. 1: a fault type not specified in bits \15:1] of the STATUS_WORD has been detected.

STATUS_ IOUT (7Bh)

Table 41. STATUS_IOUT

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OC	IOUT_OC & VOUT_UV	IOUT_OC_WARNING	x	x	x	x	x
DefaultValue	0	0	0		0	0	0	0

STATUS_ INPUT (7Ch)

The STATUS_INPUT returns the value of flags indicating input voltage status of this product. To clear bits in this register, the underlying fault or warning should be removed and a CLEAR_FAULTS command issued.

Table 42. STATUS_INPUT

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[7]	VIN_OV_FAULT	r, Latched	0	0: no over voltage detected on the OV pin. 1: over voltage detected on the OV pin.
[6]	VIN_OV_WARN	r, Latched	0	0: over voltage condition on V_{IN} has not occurred 1: over voltage condition on V_{IN} has occurred
[5]	VIN_UV_WARN	r, Latched	0	0:under voltage condition on V_{IN} has not occurred 1: under voltage condition on V_{IN} has occurred
[4]	VIN_UV_FAULT	r, Latched	0	0: Input voltage is higher than the voltage setting in VIN_ON. 1: Input voltage is lower than the voltage setting in VIN_ON.
[3:0]	Reserved	-	0	Always read as 0000

STATUS_ TEMPERATURE (7Dh)

The STATUS_TEMPERATURE returns the value of flags indicating the VIN overvoltage or under-voltage of this product. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 43. STATUS_ TEMPERATURE

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[7]	OT_FAULT	r, Latched	0	1: over-temperature Warning has occurred.
[6]	OT_WARNING	r, Latched	0	1: over-temperature Warning has occurred.
[5:0]	Reserved	r	0	Always read as 0

STATUS_ CML (7Eh)

Table 44. STATUS_ CML

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid unsupported command	Invalid /unsupported data	x	Memory fault detected	x	x	Other fault	Memory busy
Default Value	0	0	0	0	0	0	0	0

READ_VIN (88h)

The READ_VIN command returns the 10-bit measured value of the input voltage.

Table 45. READ_ VIN

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						25mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

READ_VOUT (8Bh)
The READ_VOUT command returns the 13-bit measured value of the output voltage.

Table 46. READ_ VOUT

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						1.25mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

READ_IOUT (8Ch)
The READ_IOUT command returns the 14-bit measured value of the output current. This value is also used to compare with the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT, and then affects the STATUS_IOUT.

Table 47. READ_ IOUT

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						62.5mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

READ_TEMPERATURE_1 (8Dh)
The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for the Over Temperature Fault and Warning detection. This data has a range of -255degC to +255degC.

Table 48. READ_ TEMPERATURE

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						Sign	1degC/LSB								
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

READ_TEMPERATURE_1 is a 2-byte, twos complement integer. The bit [9] is the sign bit. Below table shows the relationship between direct value and real word value.

Table 49. READ_ TEMPERATURE

SING	DIRECT VALUE	REAL VALUE degC
0	0 0000 0000	0
0	0 0000 0001	1
0	1 1111 111	+511
1	0 0000 0000	-511
1	1 1111 1111	-1

PMBus™_REVISION (98h)
The PMBus™_REVISION command returns the protocol revision we used. Accesses to this command should use the read byte protocol. Bits [7:4] indicate the PMBus™ revision of specification Part I to which the device is compliant. Bits [3:0] indicate the revision of specification Part II to which the device is compliant.

Table 50. PMBus™_REVISION

Command	PMBus™ REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0-
Access	r	r	r	r	r	r	r	r
Default Value	0	0	1	1	0	0	1	1

Bits [7:4] always reads as 4’b0011, specification PMBus™ Part I Revision 1.3.
Bits [3:0] always reads as 4’b0011, specification PMBus™ Part II Revision 1.3.

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command is used to adjust the output voltage behaviors of this product.

Table 51. MFR_CTRL_VOUT

BITS	NAME	BEHAVIOR	DEFAULT	DESCRIPTION
[7]	Reserved	Live	0	N/A
[6]	Vo Discharge	Live	0	1: output voltage discharge at CTRL low. 0: no active output voltage discharge.
[5:0]	Reserved	Live	0	N/A

Bit[6] (Vo discharge): Enable or disable active output voltage discharge when this product is commanded off through CTRL or the OPERATION command.

MFR_ADDR_PMBus™ (D3h)

Table 52. MFR_ADDR_PMBus™

Command	MFR_ADDR_PMBus™							
Format	Direct							
Bit	7	6	5	4	3	2	1	0-
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Enable	ADDR						
Default Value	0	0	0	0	0	0	0	0

Bit[7] (enable bit):
1: the address is decided by MFR_ADDR_PMBus™ [6:0].
0: the address is decided by ADDR pin.
The default value of D3h is 0x00.

Application Information

Application Circuit

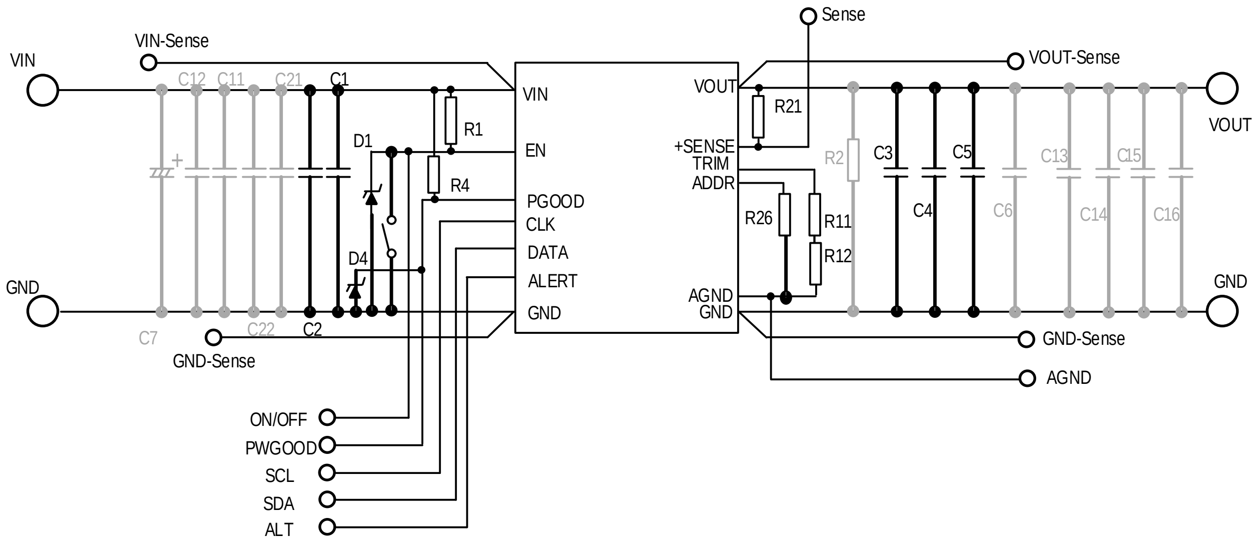


Figure 30. Application Circuit

Application Circuit Part List

An Example of the standard components are shown in Table 53. Components must be chosen referring the system requirement like Voltage, Temperature, etc.

Table 53. Application Circuit Part List

REFERENCE	VALUE	DESCRIPTION	PART AND EQUIPMENT
C1, C2	22uF/25V	Output Capacitor Ceramic capacitor, 22uF, 25V, +/-/10%, X7R	GRM32ER71E226KE15 (Murata)
C3, C4, C5	220uF/4V	Output Capacitor Ceramic capacitor, 100uF, 4V, +/-/20%, X7U	GRM32EC80G227ME05 (Murata)
R21	0 ohm	Chip resister	RK73Z1JTTD(KOA)
R11, R12	-	Chip resistor, 1/10W, +/-0.5% The value is determined by the target output voltage.	
R1, R4	10 kohm	Chip resistor, 1/10W, +/-5.0%	RK73B1JTTD103J (KOA)
R26	-	Chip resistor, 1/10W, +/-0.5% The value is determined by the target PMBus™ address.	
D1, D4	3.3V	Zenner Diode	EDZV3.3B (Rohm)
C7	1500uF/25V	Electrolysis Capacitor (Optinal)	

Example of Pattern Layout (Top View)

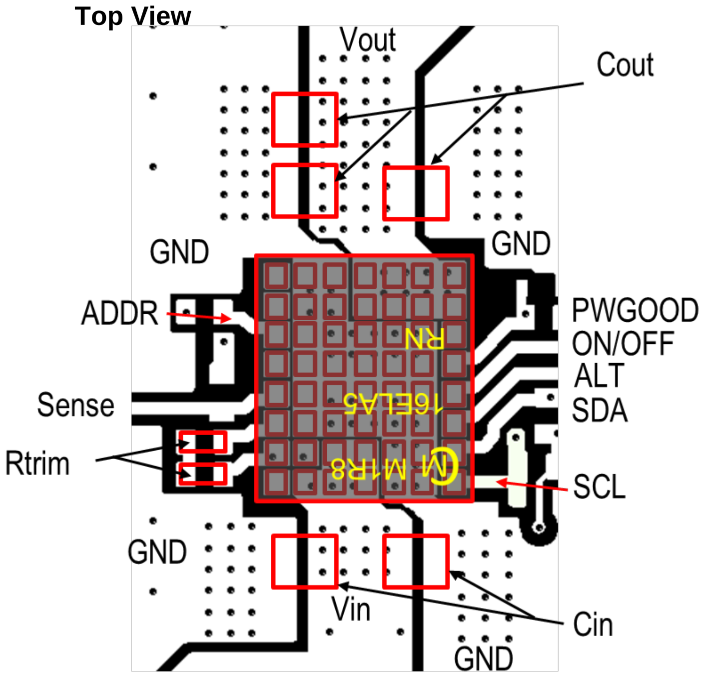


Figure 31. Example of Pattern Layout (Top View)

Application Board Example

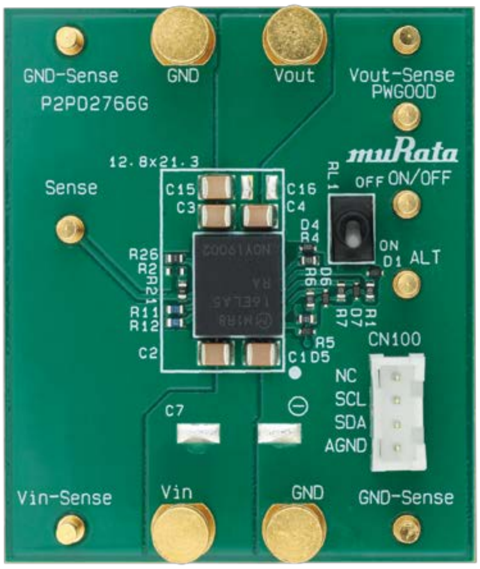


Figure 32. Application Board Example

Component Selection

Input Fuse

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

Recommended Input Filtering

The user must assure that the input source has low AC impedance to provide dynamic stability and that the input supply has little or no inductive content, including long distributed wiring to a remote power supply. For best performance, we recommend installing a low-ESR capacitor immediately adjacent to the converter's input terminals.

The capacitor should be a ceramic type such as the Murata GRM32 series and a electrolytic type such as Panasonic OS-CON series. Initial suggested capacitor values are 22uF x 2 ceramic type and 1000uF x 1 electrolytic type, rated at twice the expected maximum input voltage. Make sure that the input terminals do not go below the under voltage shutdown voltage at all times. More input bulk capacitance may be added in parallel (either electrolytic or tantalum) if needed.

Recommended Output Filtering

The converter will achieve its rated output ripple and noise with additional external capacitor. The user may install more external output capacitance reduce the ripple even further or for improved dynamic response. Again, use low-ESR ceramic (Murata GRM32 series). Initial values of 220uF x 3 ceramic type may be tried, either single or multiple capacitors in parallel. Mount these close to the converter. Measure the output ripple under your load conditions. Use only as much capacitance as required to achieve your ripple and noise objectives. Excessive capacitance can make step load recovery sluggish or possibly introduce instability. Do not exceed the maximum rated output capacitance listed in the specifications.

Packaging Information

This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Package Drawing

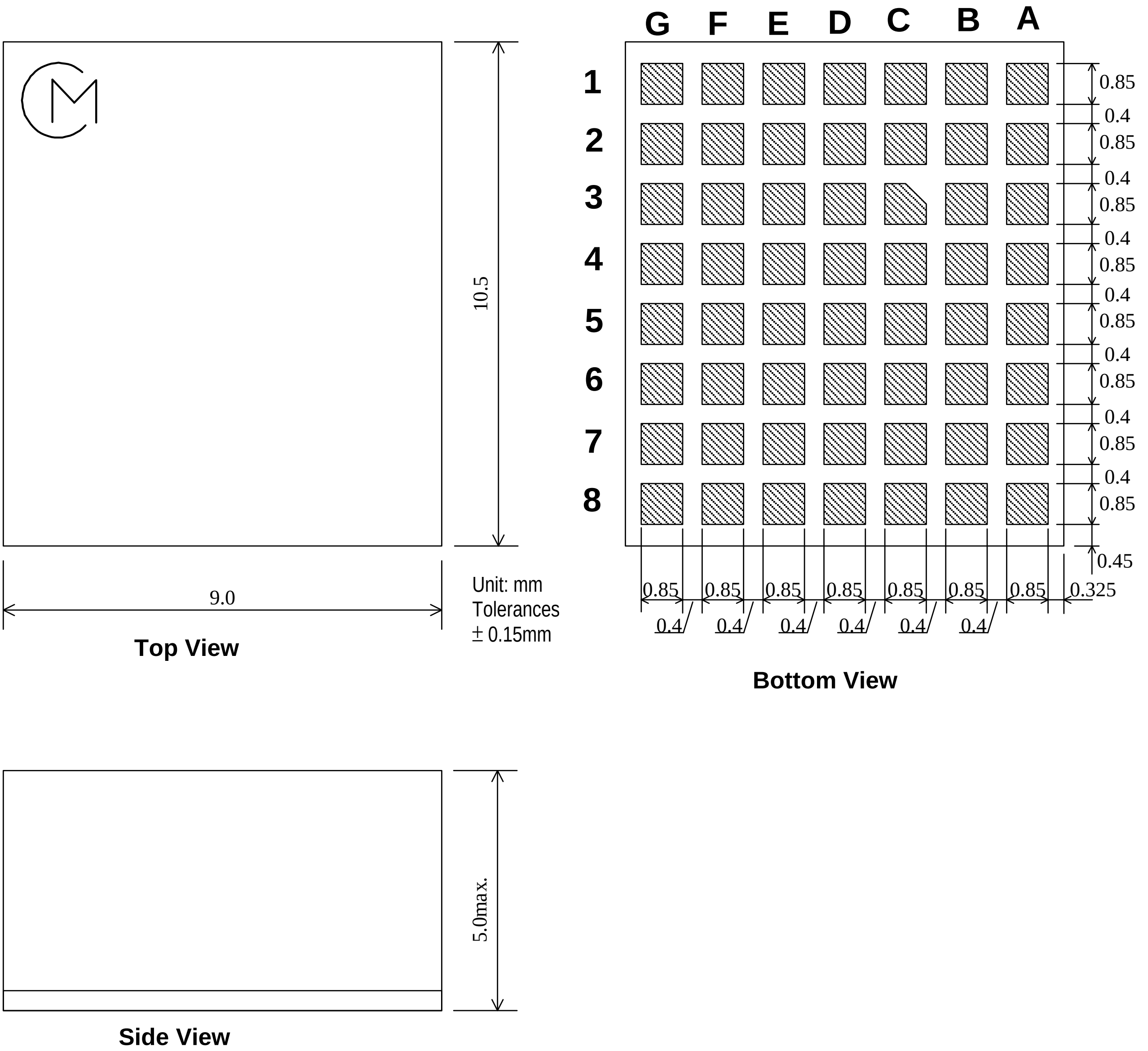


Figure 33. Package Outline Drawing

Recommended Board Land Pattern (Top View)

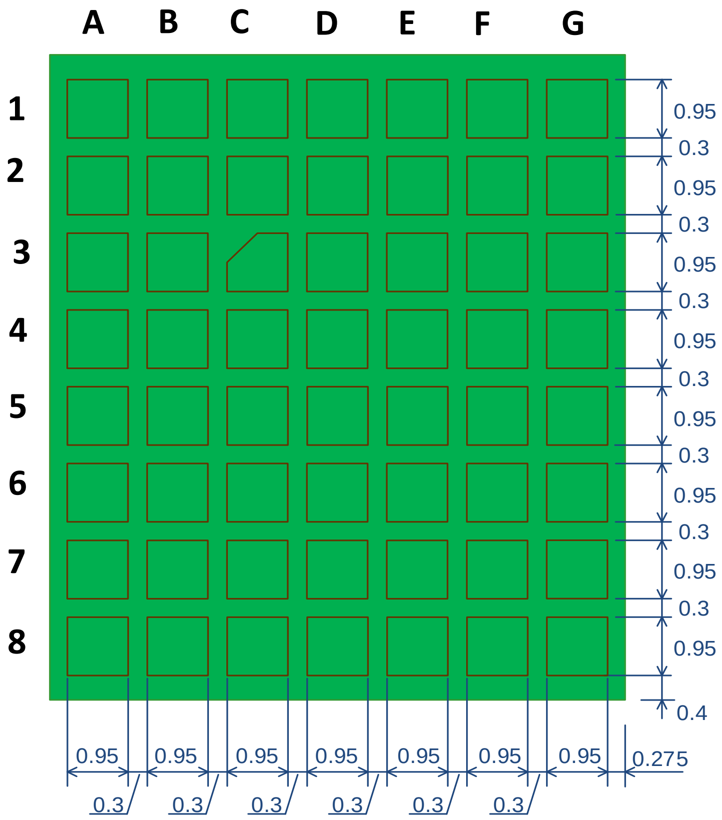


Figure 34. Recommended Board Land Pattern (Top View)

Tape and Reel Information

Tape Dimension

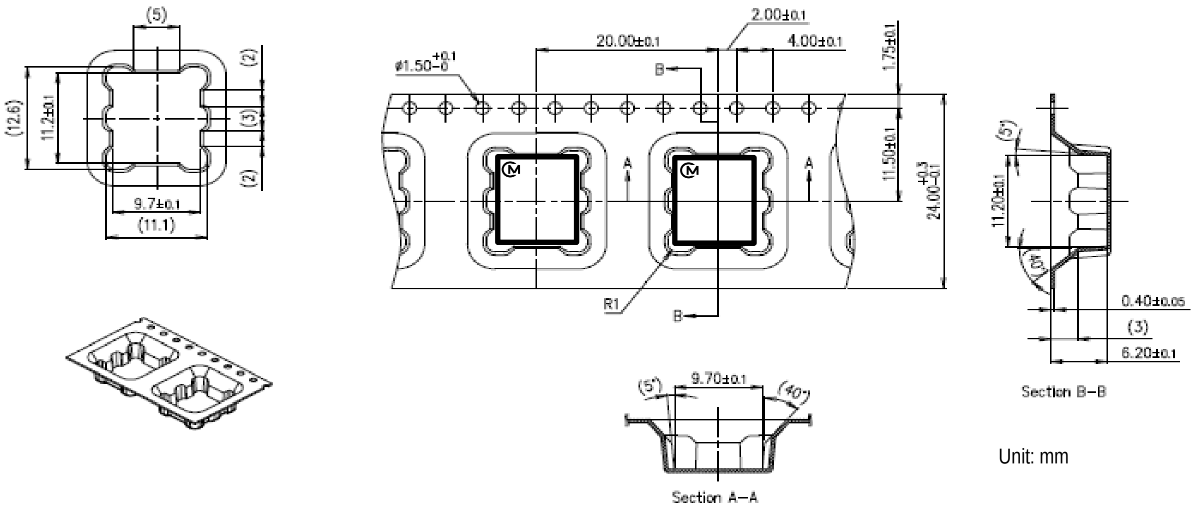


Figure 35. Tape Dimension

Reel Dimension

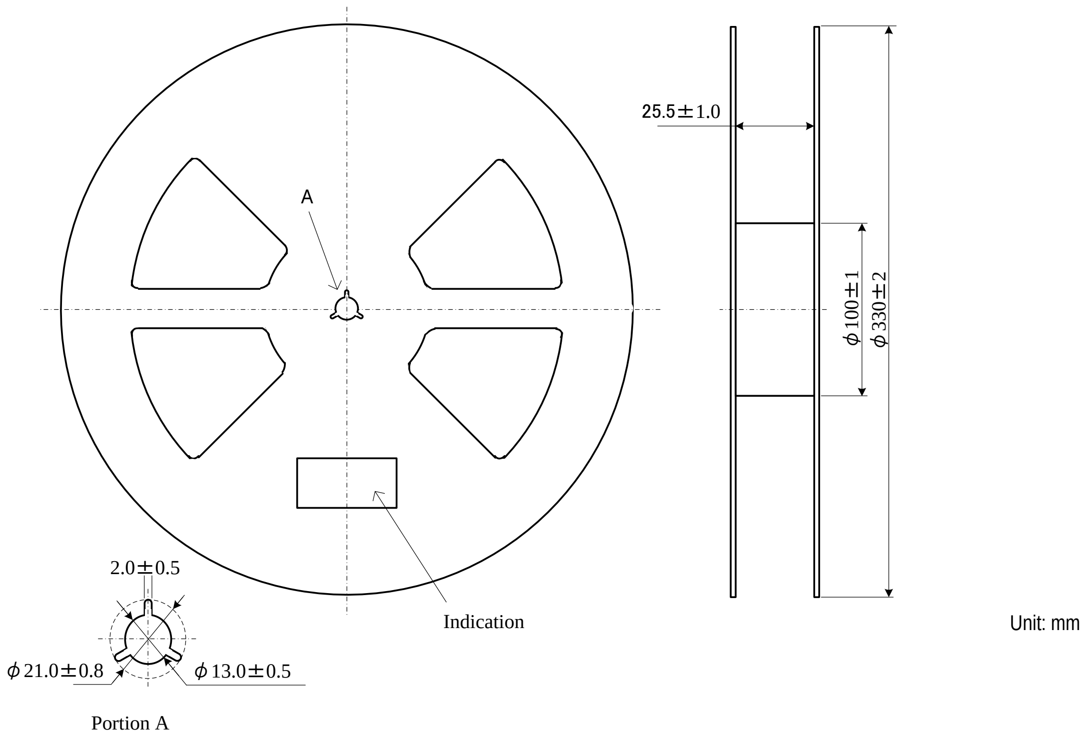
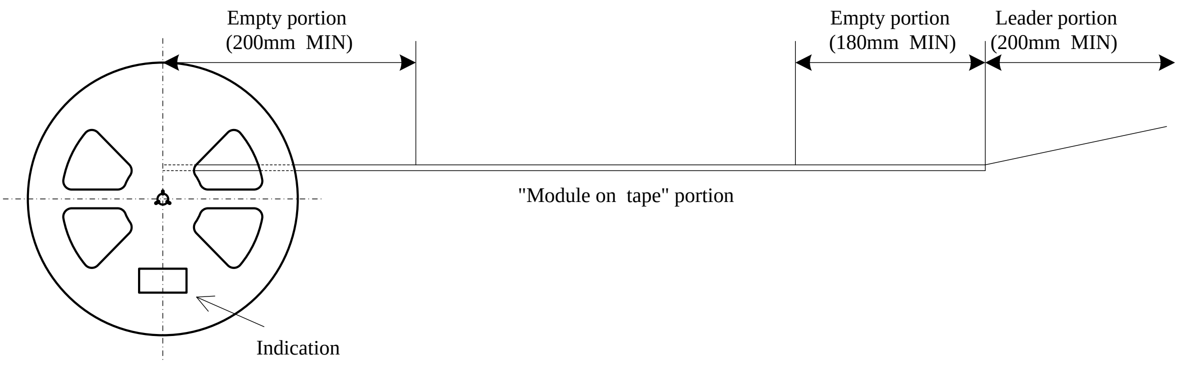


Figure 36. Reel Dimension

Tape Specifications



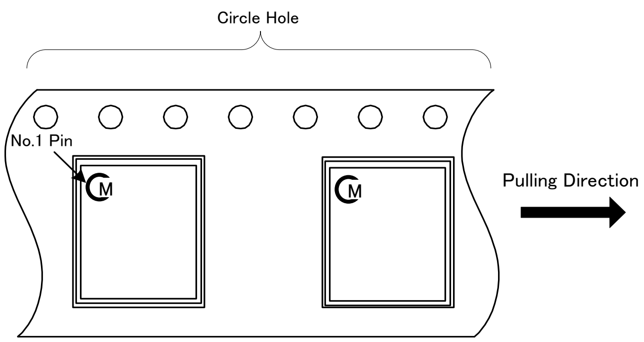


Figure 37. Tape Specifications

Notes

1. The adhesive strength of the protective tape must be within 0.3-1.0N.
2. Each reel contains the quantities such as the table below.
3. Each reel set in moisture-proof packaging because of MSL 3.
4. No vacant pocket in “Module on tape” section.
5. The reel is labeled with Murata part number and quantity.
6. The color of reel is not specified.

Soldering Guidelines

Murata recommends the specifications below when installing these converters. These specifications vary depending on the solder type.
Exceeding these specifications may cause damage to the product. Your production environment may differ therefore please thoroughly review these guidelines with your process engineers.
This product can be reflowed once.

Table 54. Reflow Solder Operations for Surface-Mount Products

For Sn/Ag/Cu BASED SOLDERS:	
Preheat Temperature	Less than 1degC per second
Time Over Liquidus.	45 to 75 seconds
Maximum Peak Temperature	250degC
Cooling Rate	Less than 3degC per second
For Sn/Pb BASED SOLDERS	
Preheat Temperature	Less than 1degC per second
Time Over Liquidus.	60 to 75 seconds
Maximum Peak Temperature	235degC
Cooling Rate	Less than 3degC per second

Recommended Lead-free Solder Reflow Profile

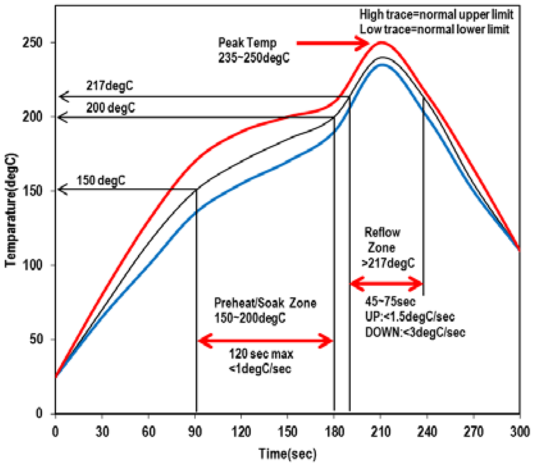
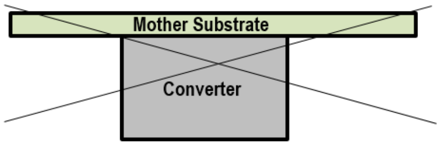


Figure 38. Recommended Lead-free Solder Reflow Profile

<u>CAUTION:</u> Do not reflow the converter as follows, because the converter may fall from the substrate during reflowing.



Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020D. During reflow PRODUCT must not exceed 250degC at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033.
(Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices.)
Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Revision History

REV	DATE	DESCRIPTION	PAGE NUMBER
A02	JUL-2023	Revise 2 terninal names (TRIM, ADDR) on Figure 25. Test Circuit and Figure 30. Application Circuit. Revise R26 connection on Figure 30. Application Circuit.	P12 P30 P30

Notices

Scope

This datasheet is applied to MYMGM1R816ELA5RN and MYMGM1R816ELA5RND.
- Specific applications: Consumer Electronics, Industrial Equipment

⚠ CAUTION

Limitation of Applications

The products listed in the datasheet (hereinafter the product(s) is called the “Product(s)”) are designed and manufactured for applications specified in the specification or the datasheet. (hereinafter called the “Specific Application”). We shall not warrant anything in connection with the Products including fitness, performance, adequateness, safety, or quality, in the case of applications listed in from (1) to (11) written at the end of this precautions, which may generally require high performance, function, quality, management of production or safety. Therefore, the Product shall be applied in compliance with the specific application.

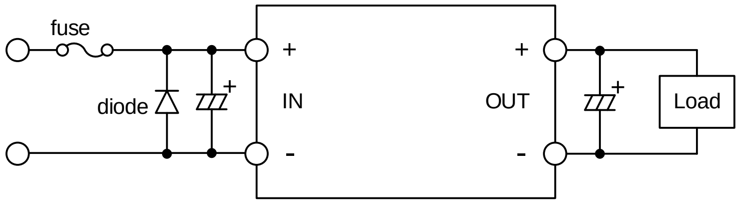
We disclaim any loss and damages arising from or in connection with the products including but not limited to the case such loss and damages caused by the unexpected accident, in event that (i) the product is applied for the purpose which is not specified as the specific application for the product, and/or (ii) the product is applied for any following application purposes from (1) to (11) (except that such application purpose is unambiguously specified as specific application for the product in our catalog specification forms, datasheets, or other documents officially issued by us*).

(1) Aircraft equipment
(2) Aerospace equipment
(3) Undersea equipment
(4) Power plant control equipment
(5) Medical equipment
(6) Transportation equipment (such as vehicles, trains, ships)
(7) Traffic control equipment
(8) Disaster prevention / crime prevention equipment
(9) Industrial data-processing equipment
(10) Combustion/explosion control equipment
(11) Application of similar complexity and/or reliability requirements to the applications listed in the above

For exploring information of the Products which will be compatible with the particular purpose other than those specified in the datasheet, please contact our sales offices, distribution agents, or trading companies with which you make a deal, or via our web contact form.
Contact form: https://www.murata.com/contactform
*We may design and manufacture particular Products for applications listed in (1) to (11). Provided that, in such case we shall unambiguously specify such Specific Application in specification or datasheet without any exception. Therefore, any other documents and/or performances, whether exist or non-exist, shall not be deemed as the evidence to imply that we accept the applications listed in (1) to (11).

Fail-Safe Function
Be sure to add an appropriate fail-safe function to your finished product to prevent secondary damage in the unlikely event of an abnormality function or malfunction in our product.

Please connect the input terminal by right polarity. If you mistake the connection, it may break the DC-DC converter. In the case of destruction of the DC-DC converter inside, over input current may flow. Please add a diode and fuse as following to protect them.



Please select diode and fuse after confirming the operation.

Figure 39. Circuit example with a diode and fuse

⚠ Note

1. Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.
2. You are requested not to use our product deviating from the reference specifications.
3. If you have any concerns about materials other than those listed in the RoHS directive, please contact us.
4. Please don't wash this product under any conditions.

Product Specification
Product Specification in this datasheet are as of May 2023. Specifications and features may change in any manner without notice. Please check with our sales representatives.

Contact form
https://www.murata.com/contactform?Product=Power%20Device

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Furthermore, the buyer and developer are responsible for predicting hazards and taking adequate safeguards against potential events at your own risk in order to prevent personal accidents, fire accidents, or other social damage. When using this product, perform thorough evaluation and verification of the safety design designed at your own risk for this product and the application.

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