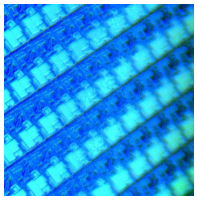


Integrated Passive Devices Technology Breakthrough by IPDiA

Rev 1.1 White Paper

Abstract

As the market for miniaturized devices continues to grow and expand, it has become evident that IPDIA has made the right choice to consider the 3D passive integration as a top priority. This IPD (Integrated Passive Device) provider is focusing its activities on 3D passive integration in silicon with an advanced technology called “PICS” (Passive Integrated Connective Substrate). High-density trench capacitors, MIM capacitors, resistors, high-Q inductors, PIN diodes or zener diodes are implemented in silicon allowing their integration in various packaging technologies with active devices suitable for very high reliability applications such as medical-grade components. In this paper, the PICS capacitors performances will be discussed and compared with the standard SMD components and an example of an efficient way of integrating 9 capacitors in a single Silicon die will be illustrated.

Key words: Integrated Passive Devices, Capacitors.

Introduction

IPDIA is involved in Silicon based 3D-IPD advanced technology. The 3D high-density capacitor is already at the forefront of IPDIA’s roadmap with three generations already in production 25nF/mm^2, 80nF/mm^2 and 250nF/mm^2 and millions of products sold in the world in the consumer market. Thanks to the outstanding characteristics of IPDIA silicon components, in terms of integration, electrical performances and reliability, the medical domain is now also demanding such a technology realizing that it is the path for miniaturization for implantable devices such as defibrillators, pace makers, neurological stimulators, drug delivery implants, earing aids, electronic pills or sensors. IPDIA is indeed providing a high-capacitance platform which, combined with the low thickness of the components, 400µm down to 100µm, delivers a high volumetric efficiency.

To enable even higher integration, development activities are now focused on the next generations of high-density capacitors targeting ambitious 1µF/mm^2. Increase of the capacitor density while keeping an acceptable breakdown voltage is challenging and requires the integration of high-k materials and studies for maximizing the 3D silicon surface.

Overview of technology & passive components

1- Description of the technology

The “PICS” high-density capacitors are using the third dimension to substantially increase the capacitor surface and thus its capacitance without increasing the capacitor footprint. Figure 1 shows a cross section of the first generation capacitor: the bottom electrode is formed by doped silicon, the dielectric is a thin layer and the top electrode is formed by deposition of a doped layer. Pores in the silicon are realized by dry etching with the so called “Bosch process” [6].

According to the well known formula $C = \frac{\varepsilon_0 \times \varepsilon_r \times S}{e}$, there are several ways to get higher capacitor density: increase the permittivity (ε_r) of the capacitor dielectric, minimize dielectric thickness (e) or increase the surface of the capacitor (S).

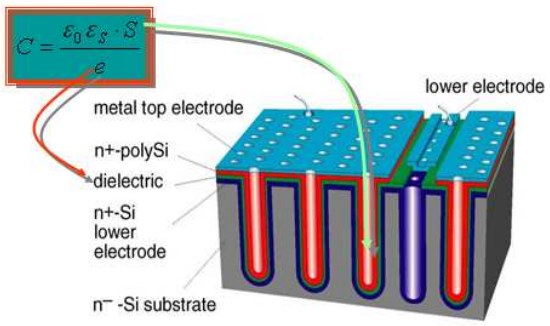


Figure 1: Cross-sectional view of a "PICS" high density trench capacitor

It is important to notice that the fabrication of these capacitors is requiring only standard process techniques and that the materials used are well known and appreciated for their high reliability.

2- Performances and advantages of "PICS" high density capacitors

This Passive Integrated Connecting Substrate ("PICS") technology exhibits inherent good performances with very high stability (temperature, voltage, ageing), superior reliability and very low parasitic elements (ESR, ESL). It is an excellent alternative to discrete component (MLCC and tantalum capacitors) as it exhibits better performances in a much smaller volume.

The temperature performance exceeds MLCC and tantalum capacitors as "PICS" capacitors are very stable over the -50℃ / +200℃ temperature range (<0.002%) (Figure 2). The capacitance value is also very stable whatever the DC voltage variation applied on the electrodes as depicted in figure 3 (<0.1%/V). There is no trade off needed between the density and the stability: "PICS" technology is offering both unlike MLCC and tantalum components.

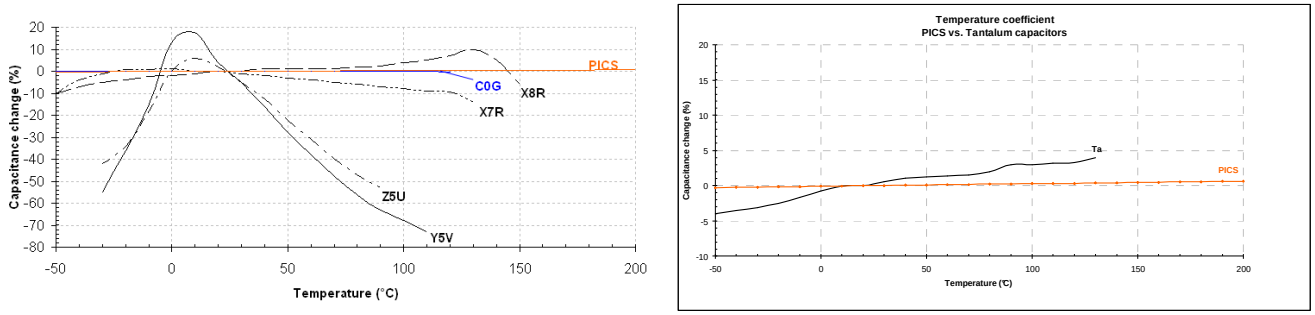


Figure 2: Temperature performances comparison with various types of MLCC

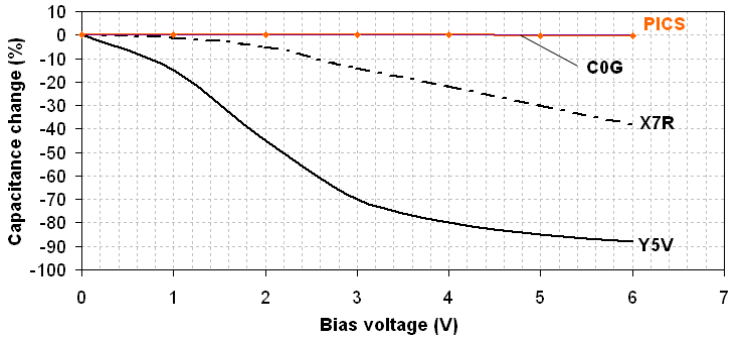


Figure 3: Voltage stability performances comparisons with various types of MLCC

Leakage current is also a key differentiator as typical value is <30nA/µF whatever the temperature and the operating voltage conditions. A leakage current variation inferior to 12pA/℃ is measured (Figure 4).

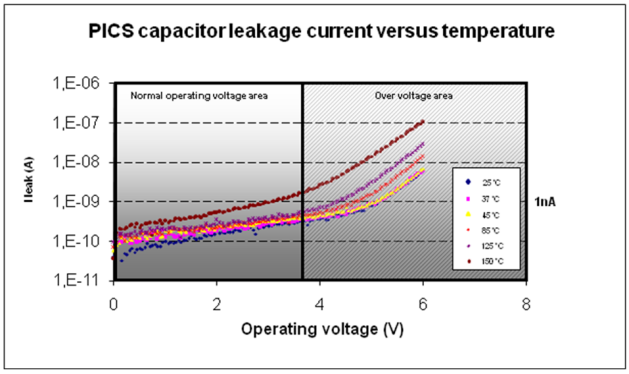


Figure 4: Leakage current vs. temperature

Because of their 3D structures, the silicon capacitors offer drastic improvement in terms of parasitics compared to commonly used capacitors. Both ESR and ESL are lower than its discrete competitors for the same capacitance value: ESR<40mΩ and ESL<250pH (Figure 5). These characteristics have a direct impact on the application performances such as higher Q-factor (>400) and self resonance frequency.

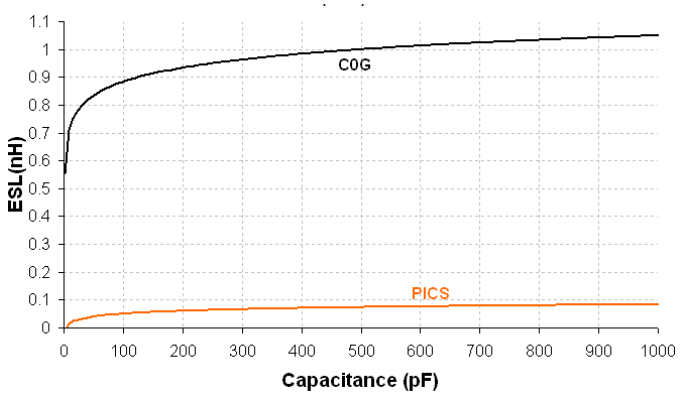


Figure 5: COG and PICS ESL versus capacitance

One of the applications for these 3D silicon capacitors is power supplies decoupling. To illustrate this, the curves in figure 6 represent the comparison in terms of insertion loss between a 100nF X7R MLCC capacitor and a 100nF “PICS” capacitor. Thanks to ultra low ESL performances, frequency rejections can be improved by 15dB.

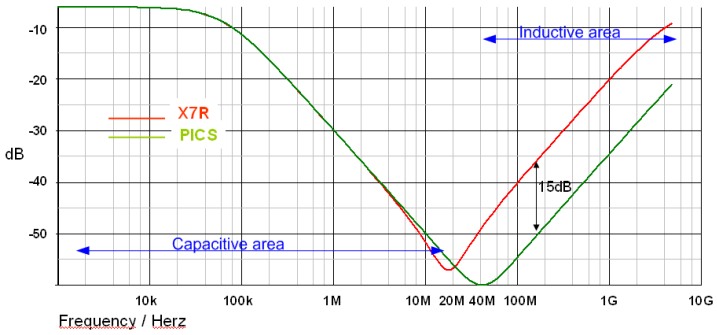


Figure 6: X7R and PICS capacitor insertion loss (100nF)

The tables figure 7 depict a summary of the reliability performances of PICS Capacitors compared to the X7R capacitor at 3 different application scenarios: operating voltage and 50% of the operating voltage, at 37℃ and 85℃.

Capacitor	FIT	FIT	FIT
	V operating 37℃	50% V operating 37℃	50% V operati ng 85℃
X7R 0402 100nF	1,31E-01	9,44E-03	2,14E+00
PICS 0402 33nF	1,25E-02	2,44E-04	4,74E-04

Figure 7: X7R, PICS FIT

Reliability engineers commonly use FIT rates to estimate reliability .FIT rates are expressed in failures per billion piece hours. Using estimated FIT rates, we can make reliability predictions at the parts-per-billion and parts-per-million levels into future years of device service given application use conditions. PICS is providing a Failure In Time (FIT) ten times better than standard SMD @ 37 ℃ and 10000 times better @ 85℃. This performance demonstrates the robust reliability of the Silicon component.

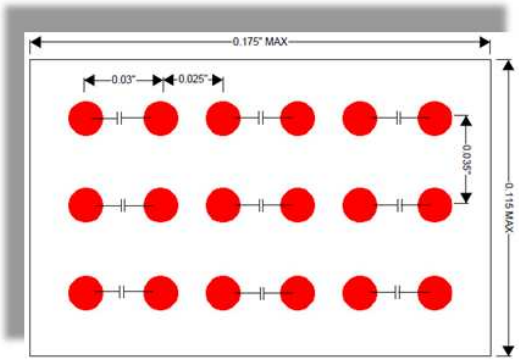
Capacitor	MTTF years	MTTF Years	MTTF years
	V operating 37℃	50% V operating 37℃	50% V operati ng 85℃
X7R 0402 100nF	4,40E+04	6,20E+05	2,50E+03
PICS 0402 33nF	4,16E+06	6,99E+07	2,10E+07

Figure 8: X7R , PICS Median time to failure

The projected median time-to-failure is well in excess of 4 000 000 years for medical devices using the Pics capacitors at the operating voltage and 37℃.

3- Application

There are many applications where the PICS technology added value is recognized as a breakthrough. Among them, the Silicon Capacitor array which is used as a replacement solution of the ceramic-based cap array combining high volume reduction and higher performances. An example is described below:

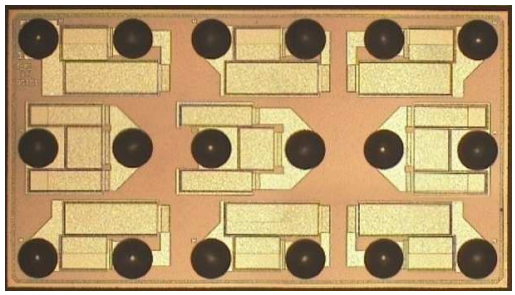


size: 13mm² and 1mm thickness

Figure 9: Current Ceramic Capacitor array

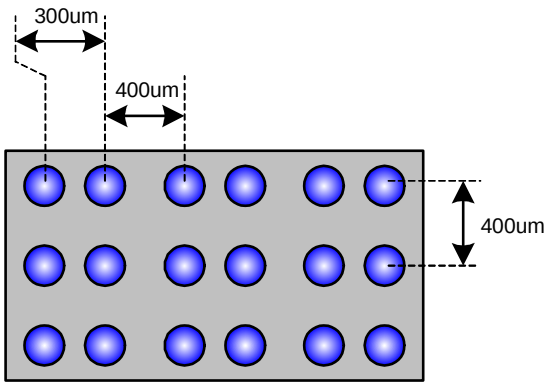
With its 3 generations of PICS, IPDIA's technology is offering the path to miniaturization:

The Silicon capacitor array is using the same PCB layout, it is pin to pin compatible with increase reliability, expanded life time and higher stability.



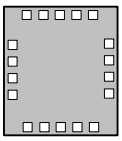
size: 8.8mm² and 250µm thickness

Figure 10: The Silicon Capacitor array with PICS1



size: 2.52mm² and 250µm thickness

Figure 11: The Silicon Capacitor array with PICS2



size**:** 0.72mm² and 130 µm thickness

Figure 12: The Silicon Capacitor array with PICS3

Conclusion

Targeting the growing passive component market, several generations of highly integrated capacitors have been successfully developed and industrialized at IPDIA.
Advantages and high performances of this 3D capacitor technology versus its competitors (MLCC and tantalum) have been demonstrated.
Technology roadmap is focusing on higher capacitor densities and development has already started to achieve the ambitious 1µF/mm^2.
This very high capacitance platform presents lots of interest in different domains, in this paper we have illustrated one of them in the medical domain where miniaturization and reliability are the key drivers.

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