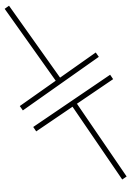

Silicon PICS capacitors as replacement of MLCC and Tantalum capacitors

Rev 1.1

Application Note

Outline

IPDiA high stability capacitors are dedicated to all demanding applications where stability is the main parameter.

IPDiA Silicon capacitors offer improved temperature, voltage, and aging performance as well as high reliability far exceeding the alternative capacitor technology.

Silicon capacitors offer intrinsic performances which can improve the applications performances when they replace ceramic/tantalum capacitors. They are also a smart way to reduce the application volume and increase the IP protection level.

Problematic with MLCC and Tantalum capacitors

Problematic with SMD capacitors	Solutions and benefits with PICS
High leakage current for battery powered applications.	Very low leakage current (<500pA for a capacitor 200nF capacitor @3.6V) guaranteed by process. No screening required.
Reliability (cracks on MLCC...).	High integration capability reducing the number of passive components in the application and reducing component interconnects. TDDB **>10 years @100°C** **>12 years @37°C**.
Decoupling efficiency requiring (RF, digital).	Very low ESL capacitors. Capacitance to be used can be optimized.
Efficient decoupling with minimum embedded capacitors.	Very low ESL capacitors.
Over sizing of capacitor value (often a factor of 2) for sensitive capacitive circuitry to secure the amount of energy stored in the capacitors, whatever the operating voltage.	Very stable capacitor value over the full operating voltage & temperature ranges.
Size.	Integration with a volume of **2200nF/mm^3**
Voltage and temperature stability.	Ultra stable capacitors in the **range -50 to +200°C and 0 to +5.5V**.

ipdia
The 3D Silicon Leader

PICS capacitors general performances compared to MLCC & Tantalum technologies

The PICS technology offers clear advantages compared to MLCC and Tantalum capacitors.
The temperature performances exceed MLCC and Tantalum capacitors, as depicted in the next figure.

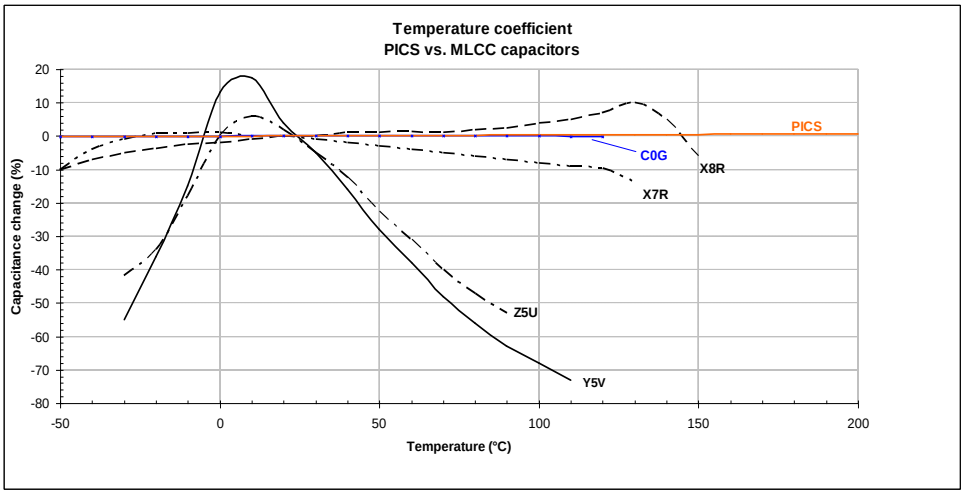

Fig.1 Temperature performances comparison with various types of MLCC capacitors

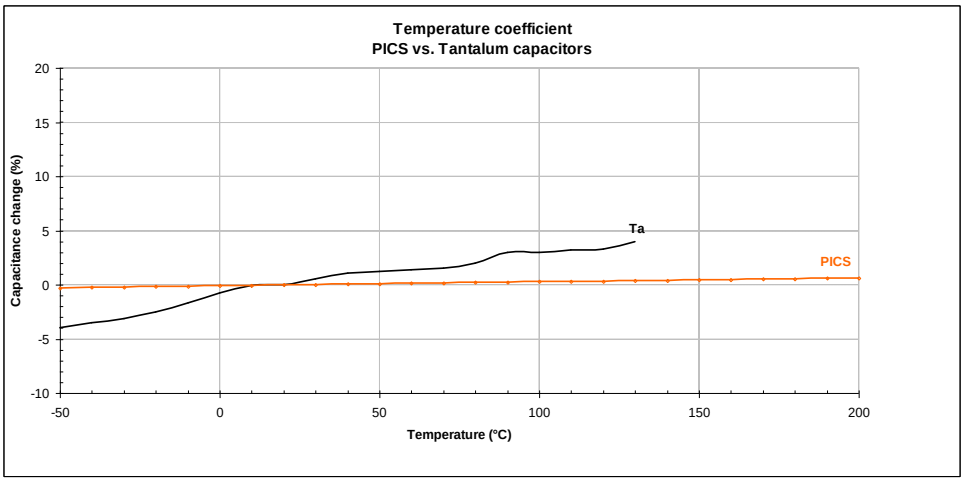

Fig.2 Temperature performances comparison with Tantalum capacitors

The capacitance value is also very stable whatever the DC bias voltage applied on the electrodes, as depicted in the next figure.

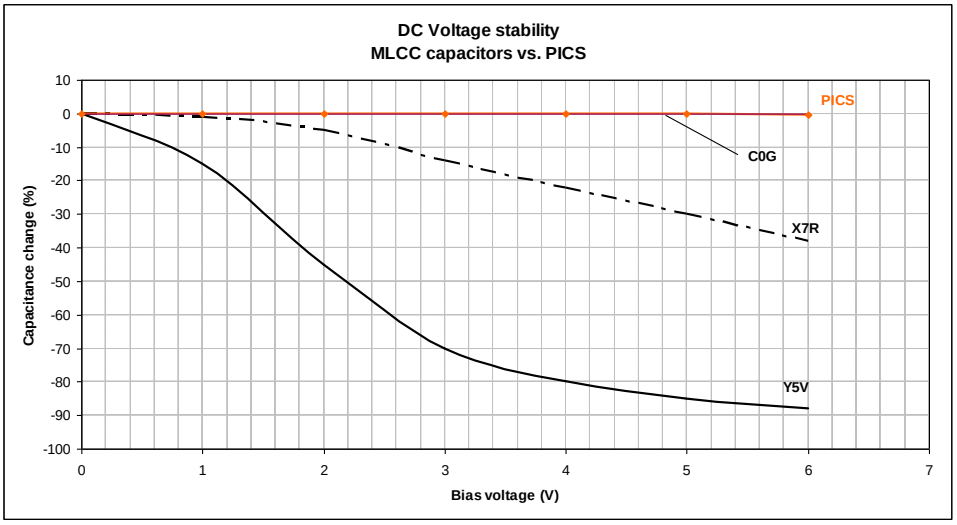

Fig.3 Voltage stability performances comparisons with various type of MLCC capacitors

Electrical aspects

Because of their 3D structure, the silicon capacitors offer major improvements in terms of parasitics compared to commonly used capacitors. Fig.4 shows the general electrical model of a capacitor.

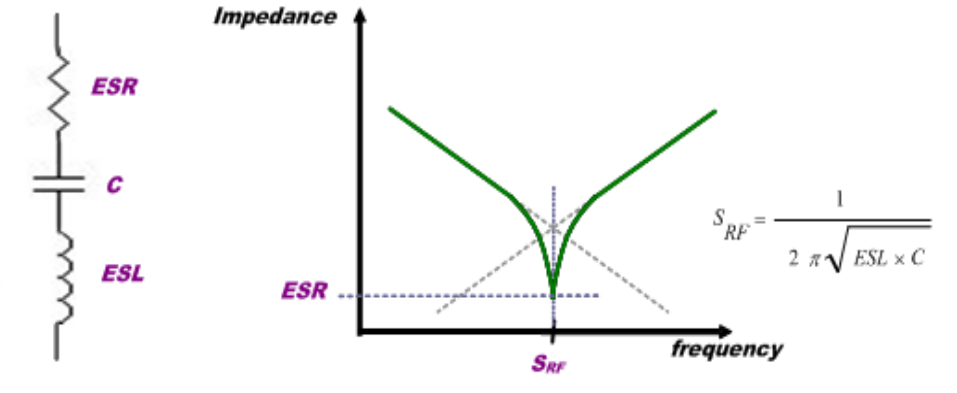

Fig.4 Capacitor model and Series Resonance Frequency definition

Both ESR and ESL are lowered compared to MLCC and Tantalum capacitors for the same capacitance value, having a direct impact on the applications performances.

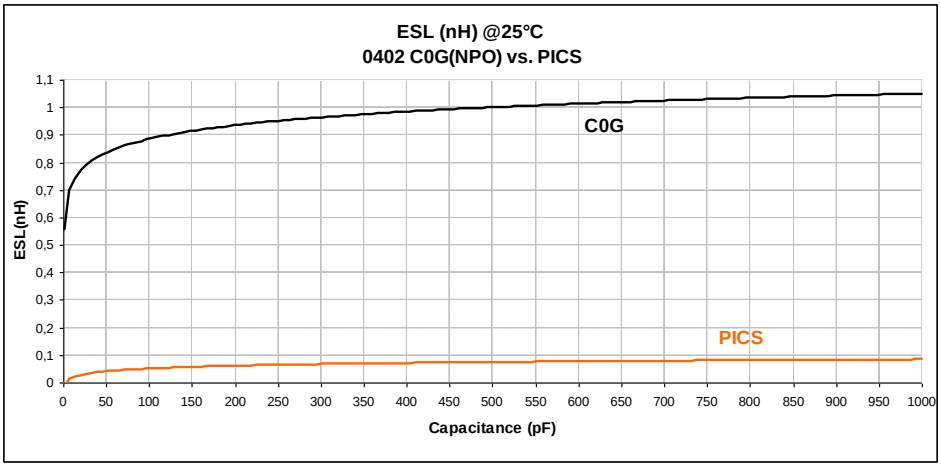

Fig.5 Comparison between 0402 C0G (NPO) and PICS capacitors

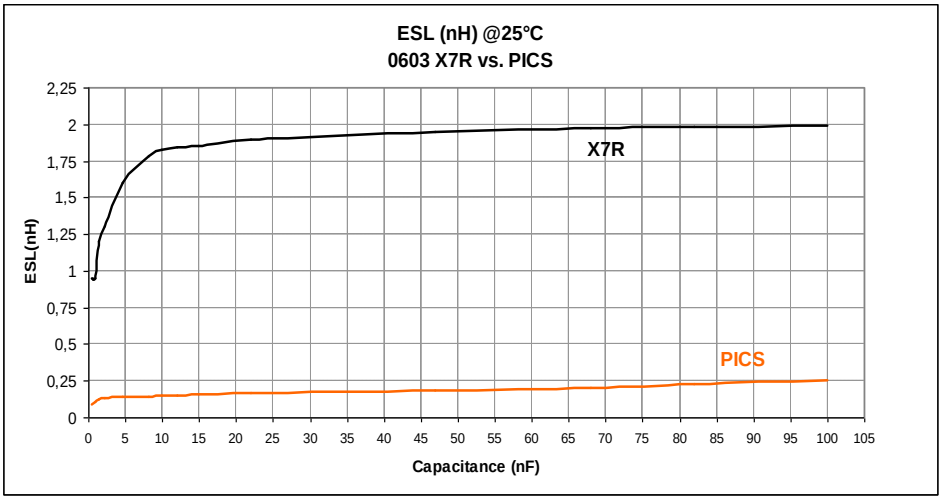

Fig.6 Comparison between 0603 X7R and PICS capacitors

Decoupling aspects

Power supplies decoupling

The power supply decoupling can often be optimized with even better performances compared to standard decoupling with SMD capacitors but a few rules need to be verified.

A decoupling capacitor offers two domains where the decoupling is effective:

- the capacitive area directly related to the capacitor value
- the inductive area driven by the parasitic ESL.

The next figure represents the comparison in terms of insertion loss between a 100nF SMD X7R capacitor and a 100nF PICS capacitor.

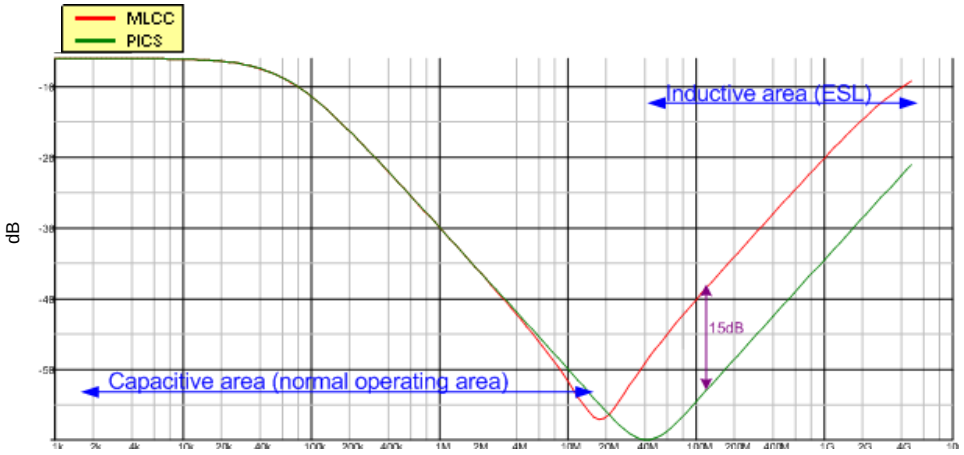

Fig.7 MLCC and PICS capacitor insertion loss (100nF)

The insertion loss at the resonance frequency is directly driven by the capacitor ESR (lower with PICS technology). The decoupling efficiency can be improved by 15dB in the inductive area.

Two decoupling situations are described hereafter as examples.

Situation 1 : Multiple resonances for high band efficiency (RF decoupling)

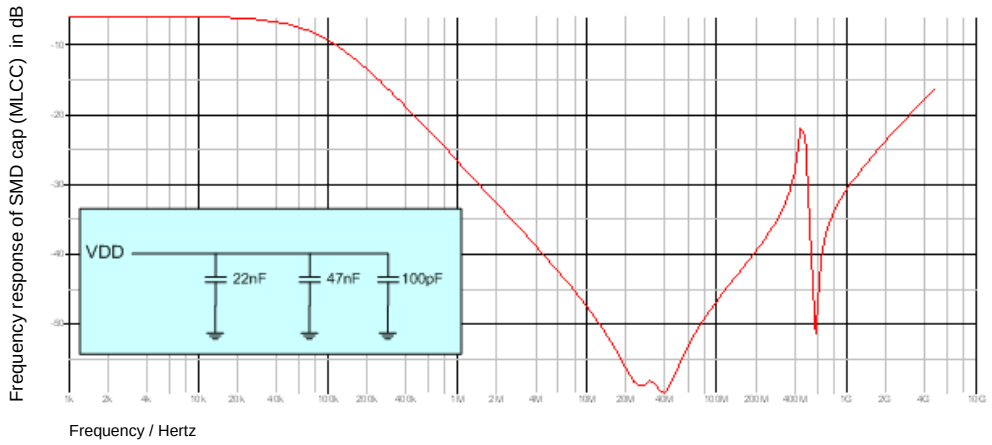

Fig.8 Analog decoupling situation with SMD capacitors (MLCC)

For such a situation, the decoupling capacitors value needs as a first order to stay at the same value (no optimization). The advantage with PICS is a better efficiency at the resonance frequencies (lower ESR).

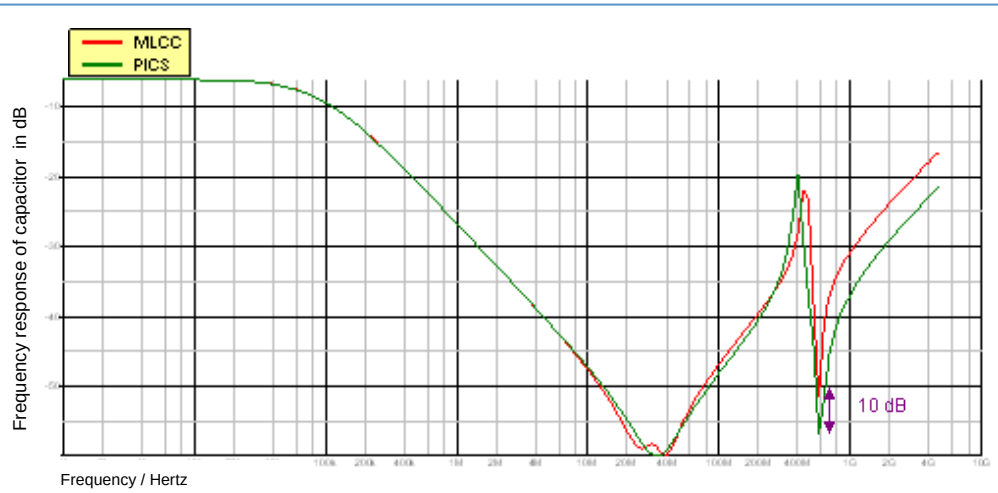

Fig.9 Analog decoupling situation with PICS capacitors

Note that the PICS technology allows fine tuning of the ESL to place the notches at the required frequencies.

<u>Situation 2</u>: digital devices (digital power supplies decoupling)

This situation is met with decoupling of digital devices. As example, we assume a 100nF capacitor is used for the decoupling and most of the time, the capacitor is used in the inductive area as we need to suppress frequencies higher than a certain value. The PICS capacitor is placed very close to the power supply pins/pads to be decoupled, reducing in a drastic way the parasitic inductance between the capacitor and the pads. It is very common to divide the SMD capacitor value by a factor 4 to 5.

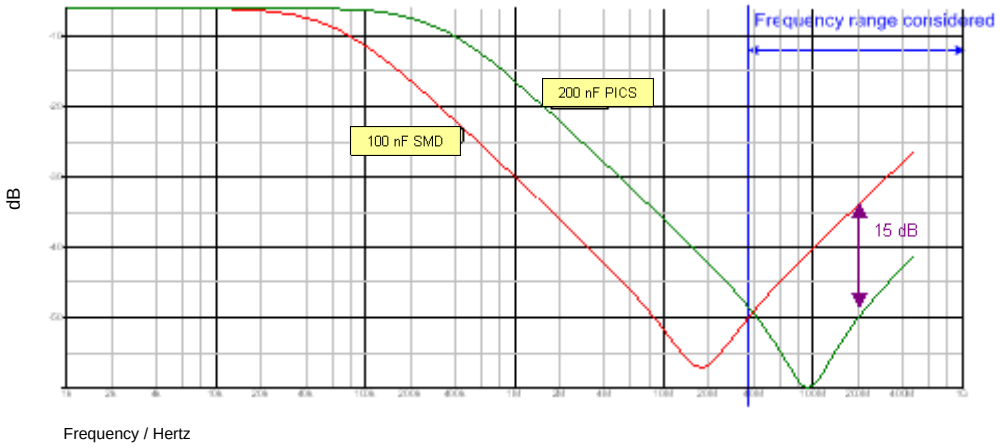

Fig.10 Digital power supply decoupling situation with PICS capacitors

Charge pump aspects

In charge pump applications, two parameters are critical:

- the capacitor value stability over the voltage applied
- the leakage current which needs to be as small as possible to ensure the capacitors remain charged. This is important for battery powered applications.

The next figure shows the stability of the capacitor value (C) compared to the value when no voltage is applied (C_0) for various supply voltages and temperatures.

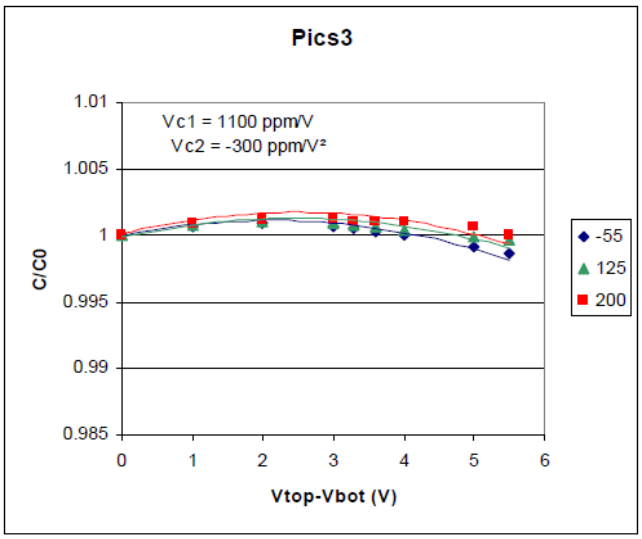

Fig.11 Capacitance stability vs. applied voltage at different temperatures

The capacitance value 'C' can be expressed as:

$$C = C_0.(1 + VC_1.V + VC_2.V^2).(1 + Tcl.(T - T_0))$$

For PICS3:

VC1= 1100ppm/V

VC2=-300ppm/V²

Tcl= 62ppm/K

The next figure provides some indications in terms of leakage current performances for three capacitor values processed in PICS3.

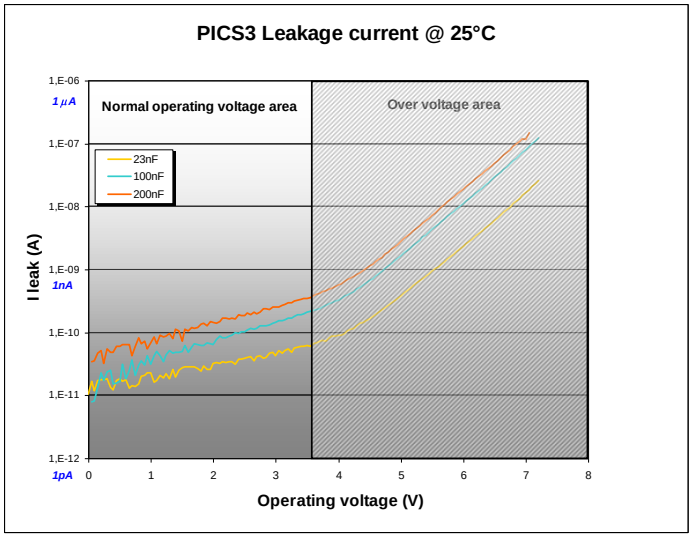

Fig.12 Leakage current in PICS capacitors (PICS3)

The next figure provides the leakage current variation for a 100nF capacitor vs. the operating voltage for different temperatures.

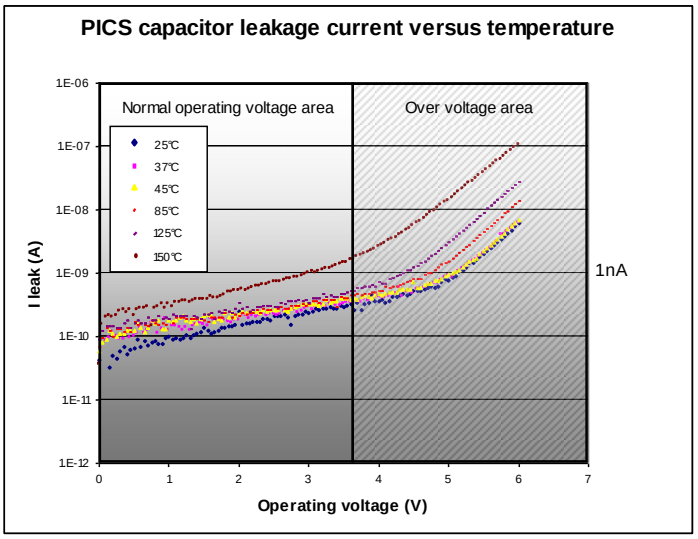

Fig.13 Leakage current in a 100nF PICS capacitors vs. temperature (PICS3)

Key values:

- leakage current <30nA/µF whatever the process, temperature and voltage conditions.
- leakage current variation < 12pA[per 100nF]/°C (1nA@85°C@3.6V for 100nF).

Optimizing the integrated capacitance value with the PICS technology

In many applications, the capacitors value is oversized to take into account that the capacitance changes with the operating voltage, with the temperature and ageing.

As an example, we assume a 100nF 0402 X7R 6.3V capacitor in an application working at 100°C, under a 5.5V DC operating voltage and achieving filtering of a signal @1MHz. The 100nF capacitors represent a standard value in many applications.

The PICS capacitor optimized value would be in the range of 65nF, because of the capacitor stability over voltage, temperature and ageing, which is about **35% lower than the SMD value** (see next figure).

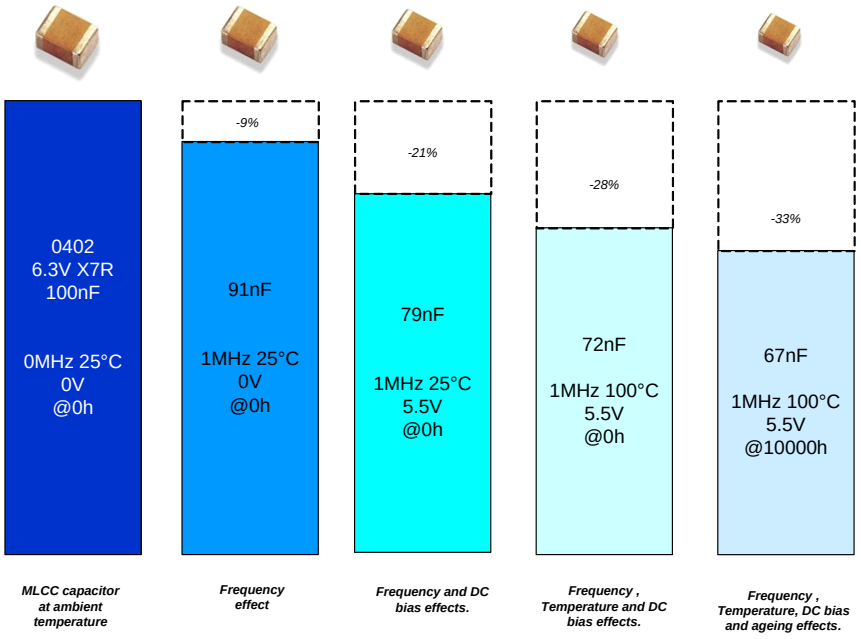

Fig.14 Example of MLCC capacitance variation (X7R)

Reliability

Thanks to the robust silicon process, the reliability is also a major advantage of this technology with a Failure In Time (FIT) ten times better than conventional capacitors (0.017 FIT @ 1 year).

The typical TDDB is **higher than** 10 years @100°C or 12 years @37°C.

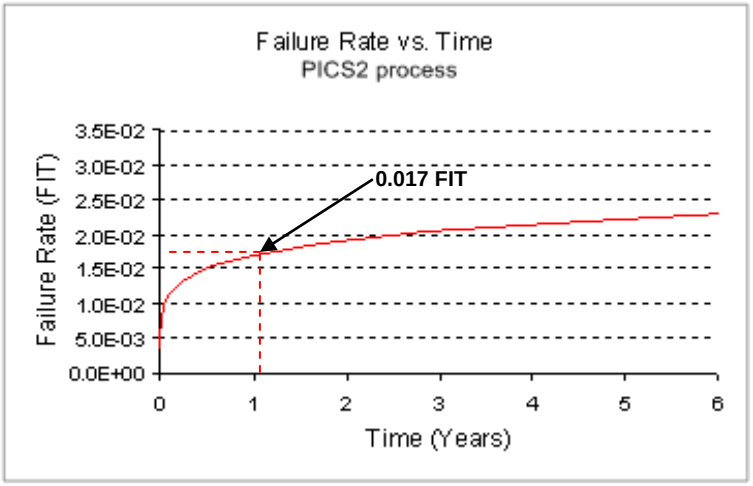

Fig.15 Failure rate for PICS2 process

Integration capabilities with PICS

PICS IPD technology is a silicon based process, allowing various assembly architectures:

- *Wire bonding*
- *Wafer level chip scale packaging (WLCSP)*
- *Die stacking*
- *JEDEC compatible footprints for reflow soldering*

Dies can be molded (plastic compound, glass), used as chip on board, flip-chip on PCB or flex substrate.

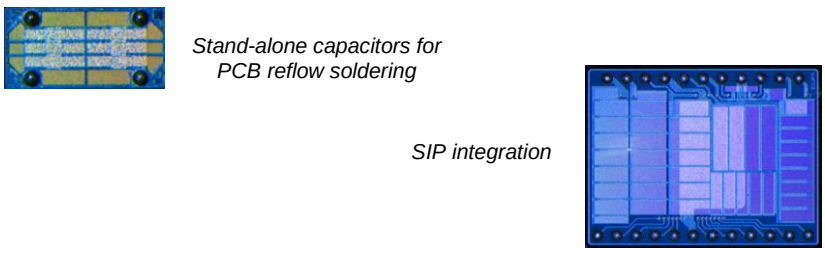

Fig.16 Various integration possibilities with the capacitors in PICS technology

Some stand-alone capacitors with a JEDEC compatible footprint (0805, 0603, 0402, 0201, 01005…) are available and can be customized under request.

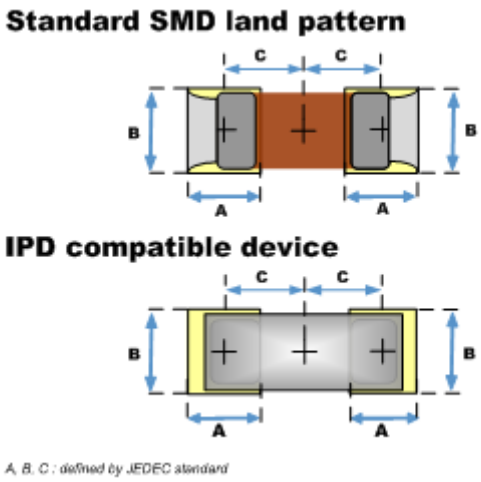

Fig.17 Stand-alone PICS capacitors with SMD compatible footprint

Quality

The IPDiA manufacturing center is certified:

- ISO-9001
- ISO-14001
- ISO-TS16949
- OHSAS-18001

IPDiA is RoHS compliant.

Summary & Conclusion

	MLCC/Tantalum	PICS
Temperature stability	--	++
Voltage stability	-	++
Leakage current	-	++
Reliability	--	+++
Integration	+	+++
Decoupling efficiency	+	+++
Flexibity with values	E6, E12 …series	customized