Rev. 1.3

General description

This document describes the attachment techniques recommended by Murata* for their UESL silicon capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact Murata Integrated Passive Solutions. The solder printing is described in this document but other processes like solder jetting, pre-bumped capacitors, can also be used with the same recommendations.

Handling precautions and storage

Silicon die must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices don't need to be handled in such an environment as the product is already well packed. The remaining quantities have to be repacked immediately after any process step, in the same conditions as before the opening (ESD bag + N2).

Store the capacitors in the manufacturer's package in the following conditions without a rapid thermal change in an indoor room:

• Temperature: -10 to 40 degree C
• Humidity: 30 to 70%RH

Avoid storing the capacitors in the following conditions:

(a) Ambient air containing corrosive gas. (Chlorine, Hydrogen sulfide, Ammonia, Sulfuric acid, Nitric oxide, etc.)
(b) Ambient air containing volatile or combustible gas
(c) In environments with a high concentration of airborne particles
(d) In liquid (water, oil, chemical solution, organic solvents, etc.)
(e) In direct sunlight
(f) In freezing environments

To avoid contamination and damage like scratches and cracks, our recommendations are:

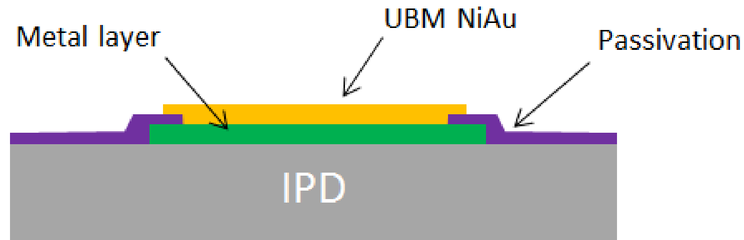
- Die must never be handled with bare hands
- Avoid touching the active face
- Do not store and transport die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD environments
- Plastic tweezers or a soft vacuum tool are recommended to remove the silicon die from the packing.

The capacitors can be delivered in the following packing: tape & reel, waffle pack, gelpak and sawing frame. Please contact the Murata sales contact for drawing and references (mis@murata.com).

*Murata Integrated Passive Solutions

Pad opening

The top surface of the UESL silicon capacitors are protected with a mineral passivation. The finishing of the contact pads are in nickel gold (generally 5μm nickel and 0.2μm gold) conforming with the soldering process.



Murata recommends having an opening on the board which matches the pad of the capacitor (size, position and spacing) – see figure 1. On the substrate, the metal layer can be larger than the varnish coating opening size but in this case, the varnish coating opening has to be mirror with the pad size of the capacitor. No need to change the metal landing pad of the PCB, only the opening in the varnish coating needs to be adjusted (see figure 1). These recommendations will improve the die placement, tilting and will avoid the contact between the solder paste and the bare silicon die - see figure 2.
Please, contact us to evaluate pre-bumping capacitors if serigraphy on board is not possible.

Solder paste after reflow:

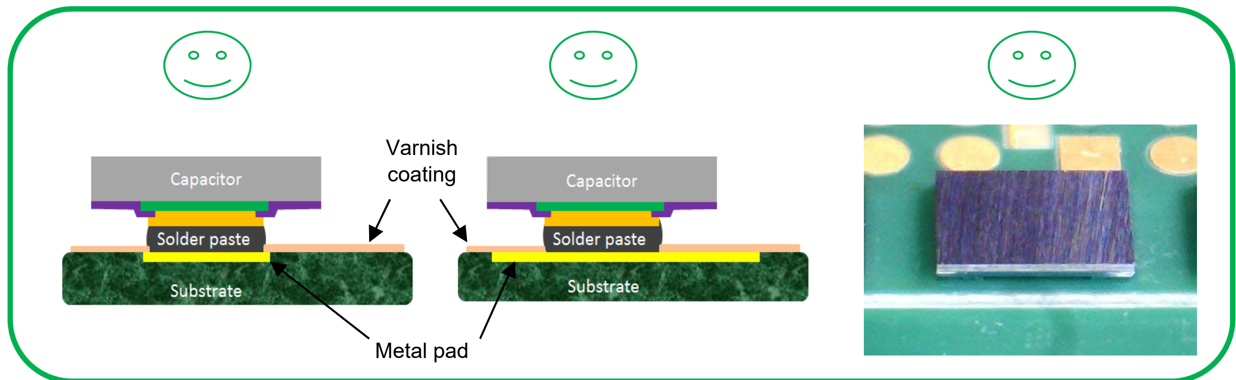


Figure 1: Solder paste after reflow - Targeted

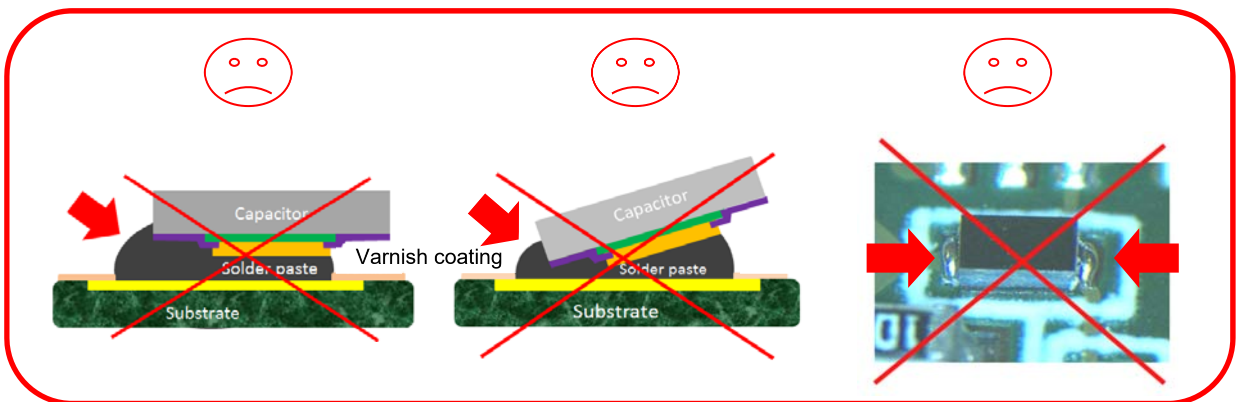


Figure 2: Solder paste after reflow - Rejected

Design of the board:

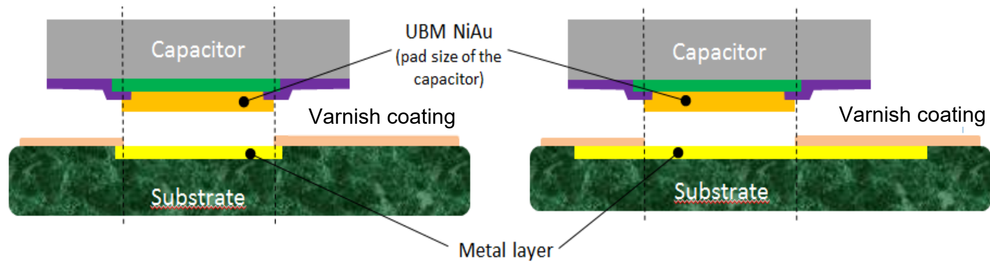
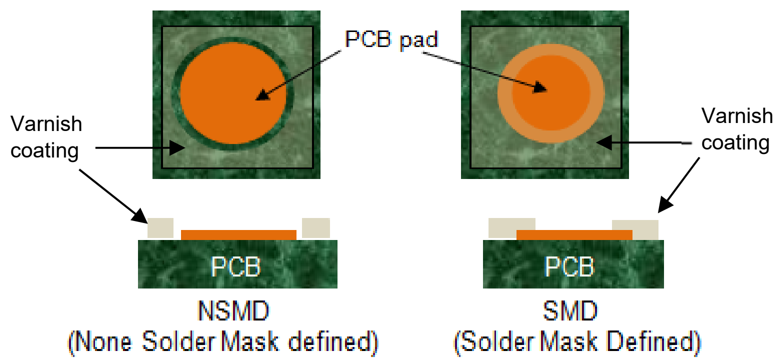


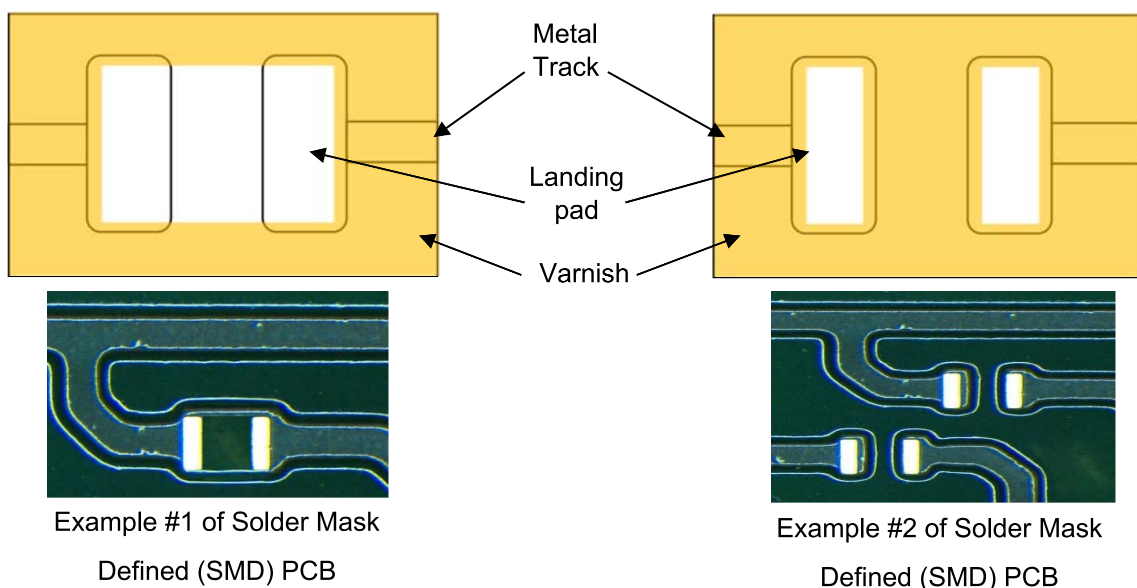
Figure 3: Opening of the metal layer on the customer substrate should match the pad of the silicon die

On the customer substrate, Murata recommends SMD (Solder Mask Design) to control the solder flowing on the tracks but NSMD (None Solder Mask Defined) can also be used with some precautions:



Nota: It is possible to remove varnish between two pads. See figure below:

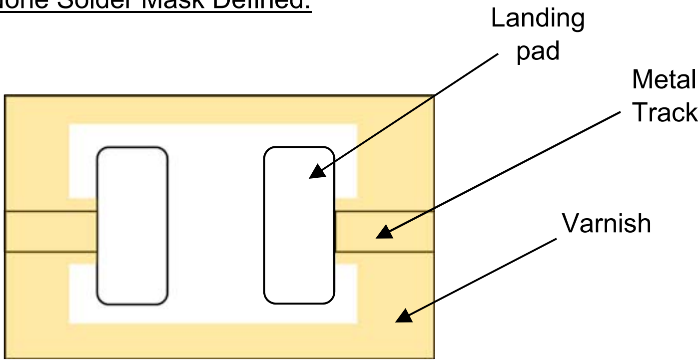
Solder Mask Defined:



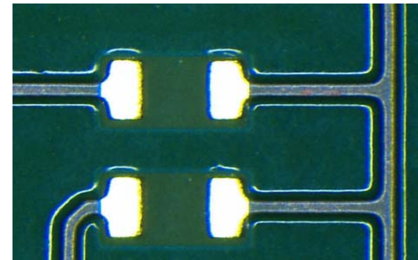
Example #1 of Solder Mask Defined (SMD) PCB

Example #2 of Solder Mask Defined (SMD) PCB

None Solder Mask Defined:



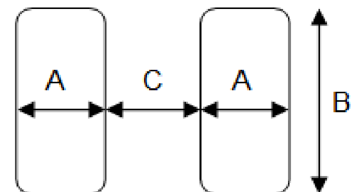
In case of NSMD, it is recommended to place a varnish in the metal track to limit the risk of contact between the solder paste and the capacitor side.



Example #3 of None Solder Mask Defined (NSMD) PCB

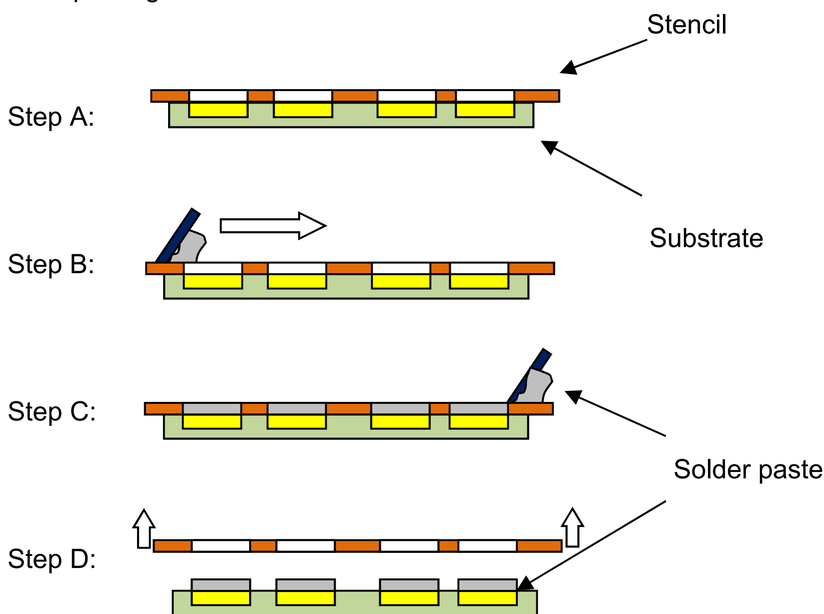
Landing pad for the PCB and die pad dimensions for the UESL silicon die:

Silicon Capacitor Type	Capacitor size (µm²)	Capacitor thickness (µm)	A (µm)	B (µm)	C (µm)
0402	1000 x 500	85	260	300	280
0404	1040 x 1040		300	850	250
0204	500 x 1000		100	800	200
0201	600 x 300		100	150	200



Process Flow

1- Solder printing of the substrate



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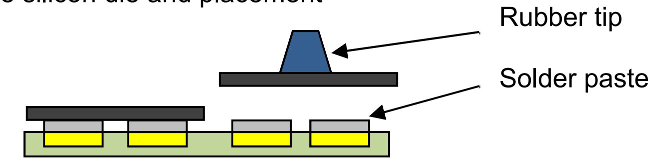
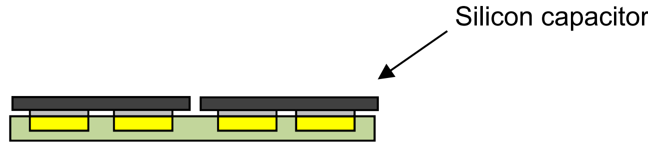
2- Picking of the silicon die and placement



3- Reflowing



4- Cleaning

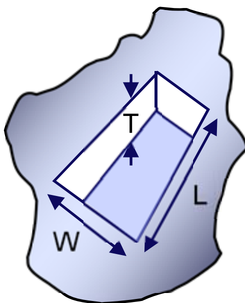
Solder print material and stencil printing recommendations

Solder pastes SnPb63/37 or SAC305 are usually used and recommended but other materials compatible with the die pad finishing are also possible.
In function of the die pad size, powder size could be adjusted. However, compared to type 3, type 6 limits the risk of tilting of the capacitor (see figure 2).

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
Sn63	63Sn, 37Pb	183°c	183°c	Eutectic
SAC305	96,5Sn, 3Ag, 0.5Cu	217°c	217°c	Eutectic

Water soluble and no clean flux can be used. In case of water soluble flux, remove the flux immediately after reflow to avoid the potential issue of leakage current between pads.

Stencil design rules in function of the quality :



INOX LASER: [(L*W)/(2*(L+W)*T)] > 0.66 & W > 1.5*T

NICKEL LASER: [(L*W)/(2*(L+W)*T)] > 0.53 & W > 1.2*T

ELECTROFORMED: [(L*W)/(2*(L+W)*T)] > 0.44 & W > 1.0*T

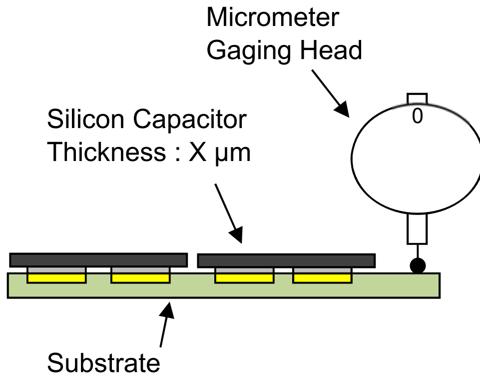
And in all cases : W > 5 * powder size

A solder joint thickness of 40 µm +/-10 is targeted:

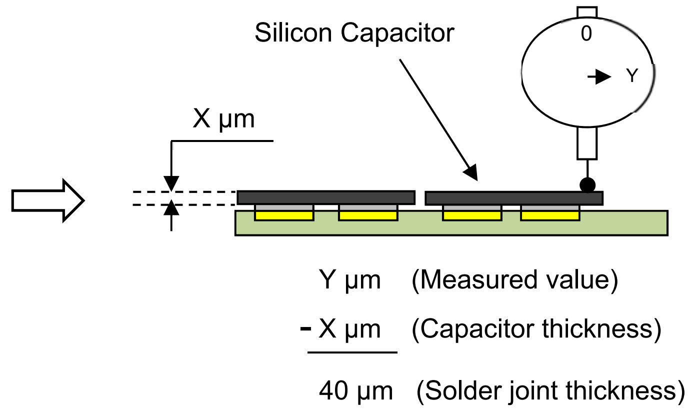
- To limit the risk of contact between the solder paste and the side of the capacitor. Such a contact would have a negative effect and would probably create a high leakage or a short circuit.
- To avoid an excessive tilting of the capacitor.
- To facilitate the cleaning under the capacitor in case of flux removing. However, the solder joint thickness can be reduced in function of the materials used by the customer (No clean flux, type of substrate with a CTE close to the silicon die…).
- To facilitate the underfilling if this step is necessary.

Procedure for the solder joint measurement (After reflow):

STEP 1:



STEP 2:



Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking but manual placement can also be done.

Using a rubber tip is particularly preferred for the die manipulation.

A minimum pressure of 50 grams and a maximum of 150 grams is recommended for the die placement on the solder paste.

Reflow soldering

Murata recommends convection reflow but vapor phase reflow and infrared reflow could be also used.

The reflow must be carried out in accordance with the JEDEC standard.

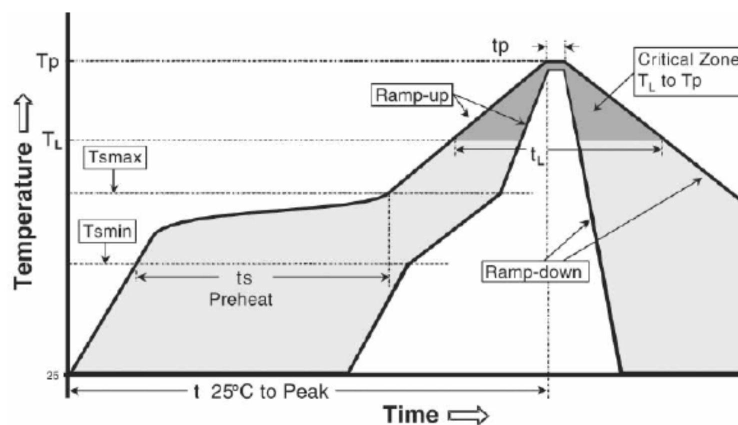


Figure 4: Generic reflow profile according to JEDEC J-STD-020-C

PROFILE FEATURE	SnPb 63/37	SAC305 (Lead-Free Assembly)
Preheat/soak		
Temperature min (Ts min)	100°C	150°C
Temperature max (Ts max)	150°C	200°C
Time (ts) from (Ts min to Ts max)	60 to 120 s	60 to 120 s
Ramp-up		
Ramp-up rate (tL to tp)	3°C/s maximum	3°C/s maximum
Liquidus temperature(TL)	183°C	217°C
Time (tL) maintained above TL	60s to 150 s	60s to 150 s
Peak temperature (Tp)	220°C	260°C
Time 25°C to peak temperature	6 minutes maximum	8 minutes maximum
Ramp-down		
Ramp-down rate (Tp to TL)	6°C/s maximum	6°C/s maximum

Flux removes tarnish films, maintains surface cleanliness and facilitates solder spread during attachment operations. The flux must be compatible with the soldering temperature and soldering times. In case of water soluble flux, please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

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www.murata.com
mis@murata.com