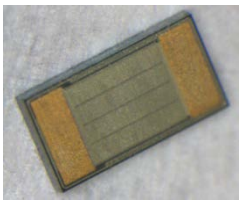
XTSC SiCap 400µm - NiAu finishing - Assembly by soldering

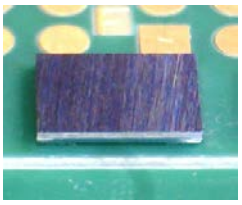
Rev. 1.9

General description

This document describes the attachment techniques recommended by Murata* for their XTSC silicon capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact Murata. The solder printing is described in this document but other processes like solder jetting, pre-bumped capacitors… can also be used with the same recommendations.



Murata Silicon capacitor (1206)



The silicon capacitor mounted on substrate

Handling precautions and storage

Silicon die must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices don't need to be handled in such an environment as the product is already well packed. The remaining quantities have to be repacked immediately after any process step, in the same conditions as before the opening (ESD bag + N2).

Store the capacitors in the manufacturer's package in the following conditions without a rapid thermal change in an indoor room:

- Temperature: -10 to 40 degree C
- Humidity: 30 to 70%RH

Avoid storing the capacitors in the following conditions:

(a) Ambient air containing corrosive gas. (Chlorine, Hydrogen sulfide, Ammonia, Sulfuric acid, Nitric oxide, etc.)
(b) Ambient air containing volatile or combustible gas
(c) In environments with a high concentration of airborne particles
(d) In liquid (water, oil, chemical solution, organic solvents, etc.)
(e) In direct sunlight
(f) In freezing environments

*Murata Integrated Passive Solutions

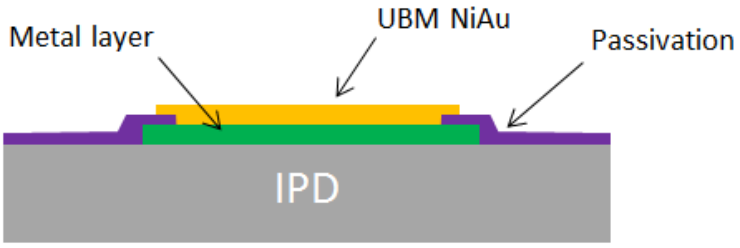
To avoid contamination and damage like scratches and cracks, our recommendations are:

- Die must never be handled with bare hands
- Avoid touching the active face
- Do not store and transport die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD environments
- Plastic tweezers or a soft vacuum tool are recommended to remove the silicon die from the packing.

Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided within waffle pack, gelpak or sawing frame. Please contact the Murata sales contact for drawing and references (mis@murata.com).

Pad opening

The top surface of the Murata silicon capacitors are protected with a mineral passivation. The finishing of the contact pads are in nickel gold (generally 5µm nickel and 0.2µm gold) conforming with the soldering process.



Murata recommends having an opening on the board which matches the pad of the capacitor (size, position and spacing) – see figure 1. On the substrate, the metal layer can be larger than the varnish coating opening size but in this case, the varnish coating opening has to be mirror with the pad size of the capacitor. No need to change the metal landing pad of the PCB, only the opening in the varnish coating needs to be adjusted (see Figure 1). These recommendations will improve the die placement, tilting and will avoid the contact between the solder paste and the bare silicon die - see Figure 2.

Solder paste after reflow:

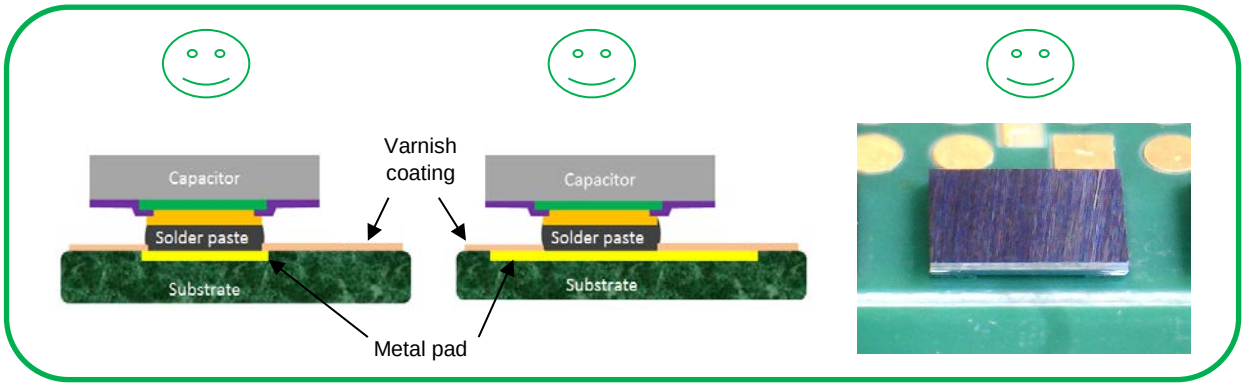


Figure 1: Solder paste after reflow - Targeted

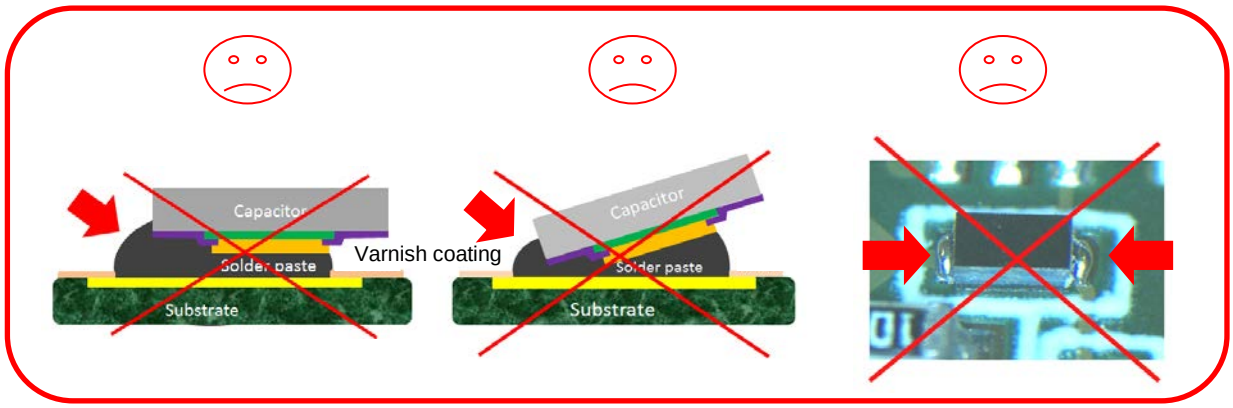


Figure 2: Solder paste after reflow - Rejected

Design of the board:

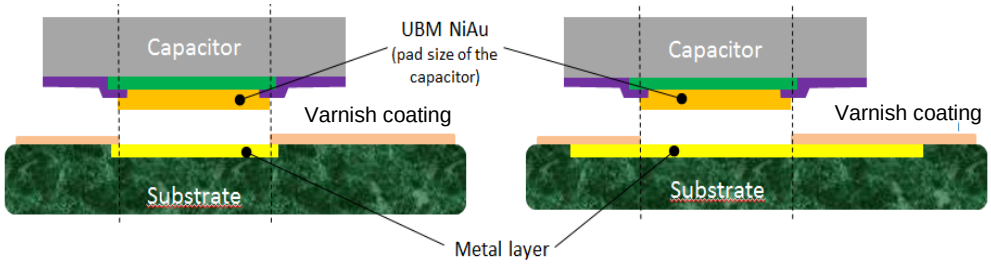
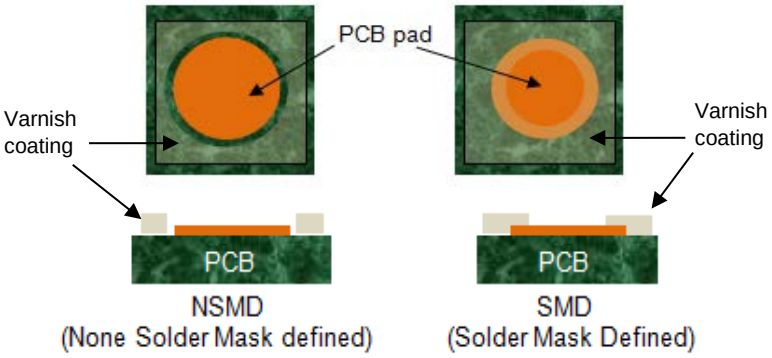


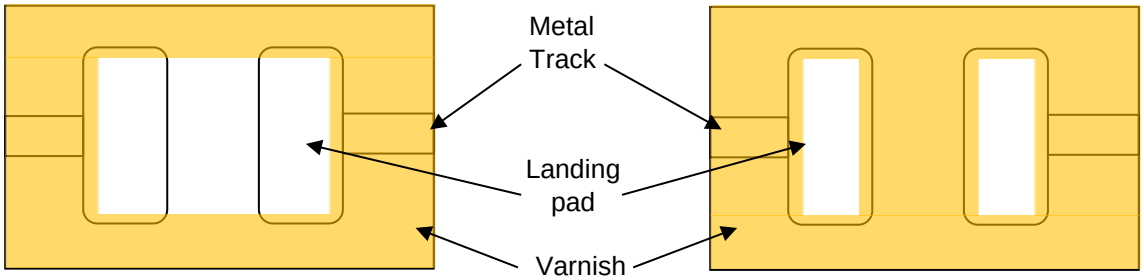
Figure 3: Opening of the metal layer on the customer substrate should match the pad of the silicon die

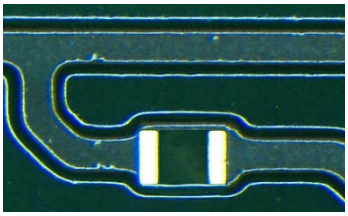
On the customer substrate, Murata recommends SMD (Solder Mask Design) to control the solder flowing on the tracks but NSMD (None Solder Mask Defined) can also be used with some precautions:



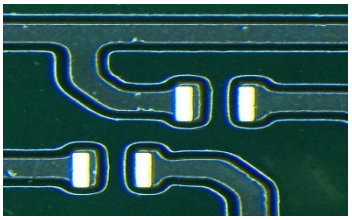
Nota: No varnish between two landing pads can be done. See figure below:

Solder Mask Defined:



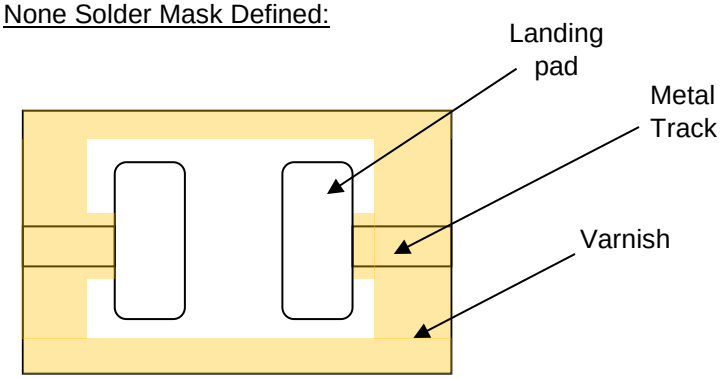


Example #1 of Solder Mask Defined (SMD) PCB

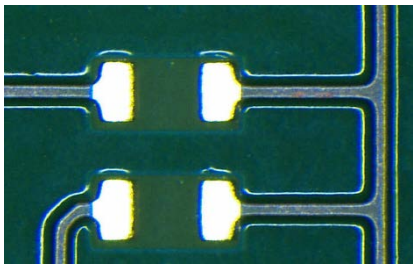


Example #2 of Solder Mask Defined (SMD) PCB

None Solder Mask Defined:



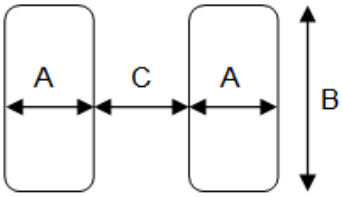
In case of NSMD, it is recommended to place a varnish in the metal track to limit the risk of contact between the solder paste and the capacitor side.



Example #3 of None Solder Mask Defined (NSMD) PCB

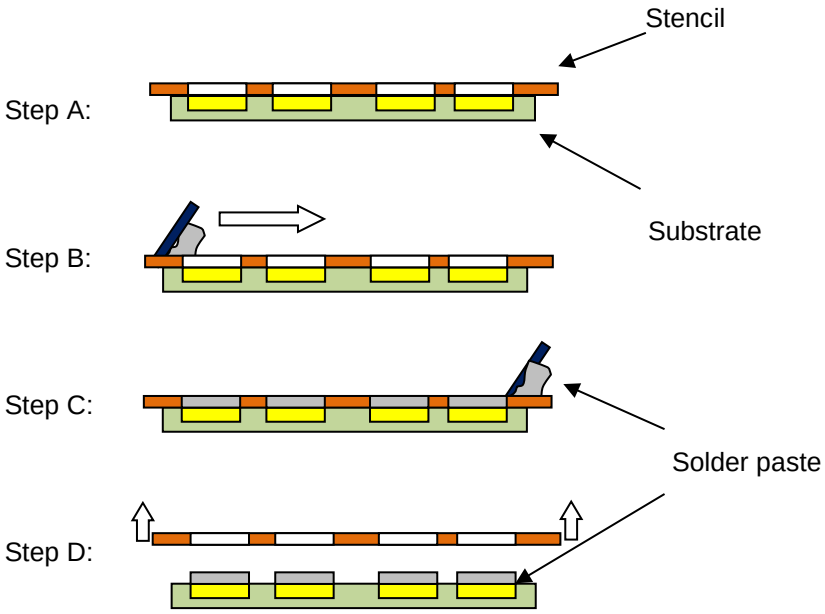
Landing pad for the PCB and die pad dimensions for the Murata silicon die:

Silicon Capacitor Type	Capacitor size (µm²)	Capacitor thickness	A (µm)	B (µm)	C (µm)
0201	800 x 600	100µm minimum	150	400	300
0402	1200 x 700		300	500	400
0603	1800 x 1100		400	900	800
0805	2200 x 1400		500	1200	1000
1206	3400 x 1800		600	1600	2000
1812	4700 x 3600		900	3400	2700

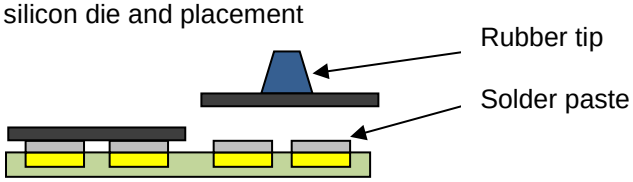


Process Flow

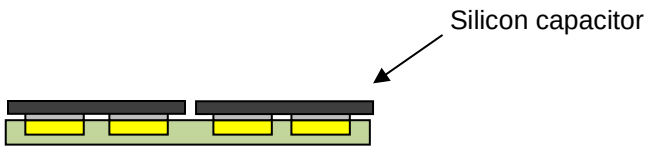
1- Solder printing of the substrate



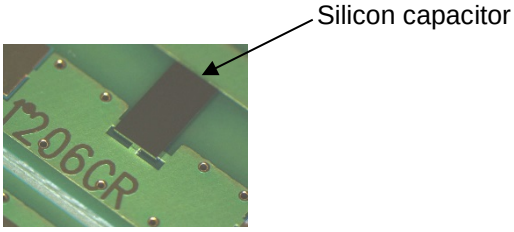
2- Picking of the silicon die and placement



3- Reflowing



4- Cleaning



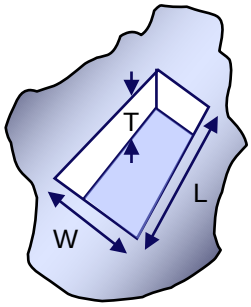
Solder print material and stencil printing recommendations

Solder pastes SnPb63/37 or SAC305 are usually used and recommended but other materials compatible with the die pad finishing are also possible.
In function of the die pad size, powder size could be adjusted. However, compared to type 3, type 6 limits the risk of tilting of the capacitor (see figure 2).

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
AuSn	80Au20Sn	280°c	280°c	
SnPb	95Sn5Pb	308°c	312°c	

Water soluble and no clean flux can be used. In case of water soluble flux, remove the flux immediately after reflow to avoid the potential issue of leakage current between pads.

Stencil design rules in function of the quality :



INOX LASER: [(L*W)/(2*(L+W)*T)] > 0.66 & W > 1.5*T

NICKEL LASER: [(L*W)/(2*(L+W)*T)] > 0.53 & W > 1.2*T

ELECTROFORMED: [(L*W)/(2*(L+W)*T)] > 0.44 & W > 1.0*T

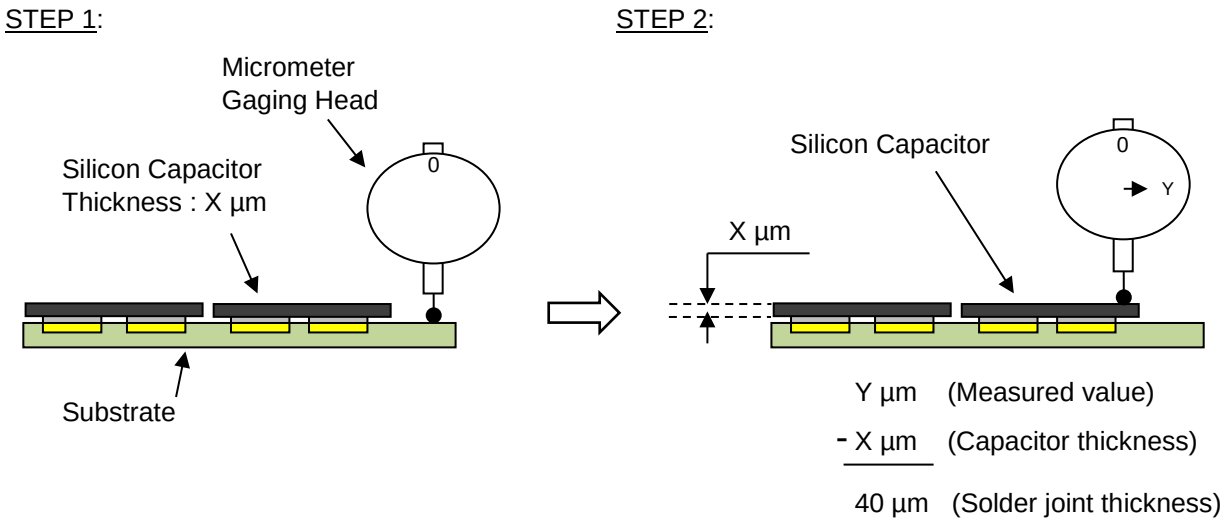
And in all cases : W > 5 * powder size

A solder joint thickness of 40 µm +/-10 is targeted to limit the risk of contact between the solder paste and the side of the capacitor. Such a contact would have a negative effect and would probably create a high leakage or a short circuit. Limited solder joint thickness will also avoid an excessive tilting of the capacitor.

For example, design of stencils done by Murata (SAC305 type 6 with 50% of flux):

Silicon Capacitor Type	Stencil opening size µm²	Stencil thickness µm	Stencil quality
0201	150 x 320	100	ELECTROFORMED
0402	260 x 369	125	NICKEL LASER
0603	300 x 768	125	NICKEL LASER
0805	400 x 960	125	NICKEL LASER
1206	500 x 1229	125	NICKEL LASER
1812	650 x 3012	125	NICKEL LASER

Procedure for the solder joint measurement (After reflow):



Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking but manual placement can also be done.

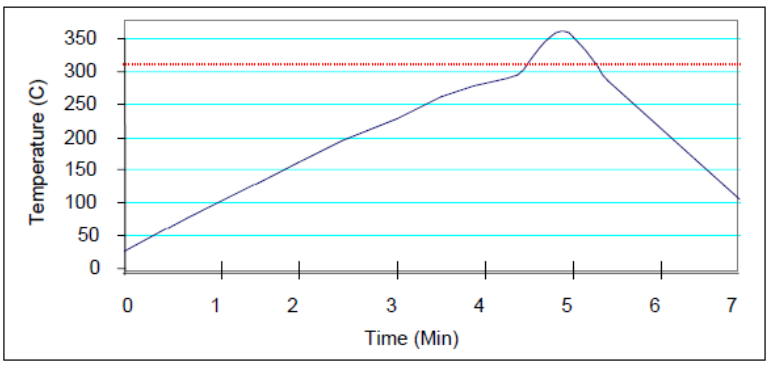
Using a rubber tip is particularly preferred for the die manipulation.

A minimum pressure of 50 grams and a maximum of 150 grams is recommended for the die placement on the solder paste.

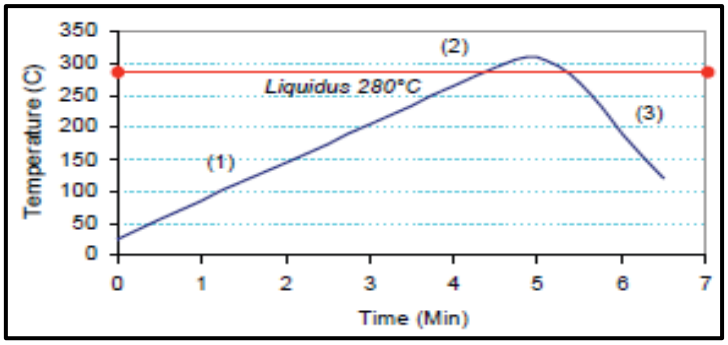
Reflow soldering

Murata recommends convection reflow but vapor phase reflow and infrared reflow could be also used.
The reflow must be carried out in accordance with the JEDEC standard.

SnPb profile: (Murata uses IndalloySn95Pb5 from Indium – ref Indalloy#171)



AuSn profile: (Murata uses Indalloy Au80Sn20 from Indium – ref Indalloy#182)



This profile will serve as a general guideline in establishing a reflow profile for your process when using a forced air convection oven. Other reflow technologies including, but not limited to infrared, hot plate or induction, may require significant changes as may varying board geometry's and densities.

Heating Stage:

1. A linear ramp rate of 1º-2ºC/second allows gradual evaporation of volatile's and prevents defects such as solder balling/beading and bridging as a result of hot slump. It also prevents unnecessary depletion of fluxing capacity when using higher temperature alloys.

Liquidus Stage:

2. A minimum peak temperature of 30º-50ºC above the melting point of the solder alloy is needed to form a quality solder joint and achieve acceptable wetting due to the formation of an intermetallic layer. If the peak temperature is excessive, or the time above liquidus greater than 45-90 seconds, flux charring, excessive intermetallic formation and damage to the board and components can occur. A ramp rate of 2.5º-3.5ºC/second from liquidus to peak temperature is recommended.

Cooling Stage:

3. This stage refers to the temperature range from the peak temperature to approximately 50ºC below the liquidus temperature where the cooling rate has negligible effect. A rapid cool down of <4ºC/second is desired to form a fine grain structure. Slow cooling will form a large grain structure, which typically exhibit poor fatigue resistance. If excessive cooling > 4ºC/second is used, both the components and the solder joint can be stressed due to a high TCE mismatch.

Flux removes tarnish films, maintains surface cleanliness and facilitates solder spread during attachment operations. The flux must be compatible with the soldering temperature and soldering times. In case of water soluble flux, please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

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