UESL

Ultra low ESL and ultra low profile capacitor down to 85 µm

Rev 1.0

Key features

- Ultra-low profile of 85 µm
- Very low ESR and ESL
- High stability
- Low leakage current
- Lead-free NiAu finishing compatible with automatic soldering technologies: reflow or manual. Other terminations available on request.

(please refer to our Assembly Application Note for more details)

Key applications

- **Power Integrity** for High-Speed IC
- Power Supply Noise Suppression
- Decouling in Power Distribution Network
- Embedded Voltage Regulator Bypass
- **Signal Integrity** of High-speed Interface
- High-frequency noise suppression
- Power line decoupling for **application processors in smartphones**
- Any applications with **ultra-low thickness** requirement

The UESL capacitors target **power integrity** and **signal integrity** for **high-speed applications.** With an ultra-low ESL (Equivalent Series Inductance) and an excellent behavior in high frequencies, the UESL capacitors are the perfect match for **power supply decoupling and bypass of high-speed digital IC.**

The UESL capacitors feature **ultra-low thickness** (**85 µm and below**) which enables advanced assembly with strong height restrictions (processor package, BGA land-side, embedded package...). The unique technology of integrated passive devices in silicon developed by Murata* provides **high stability over DC voltage and temperature.** Therefore, the UESL capacitors are not subject to derating. For example:

- the effective capacitance of the UESL 0404 450 nF is comparable to an X5R MLCC of 1 µF;
- the effective capacitance of the UESL 0402 180 nF is comparable to an X5R MLCC of 400 nF;

*Murata Integrated Passive Solutions

Electrical specifications

Parameter	Value
Capacitance range	50 nF to 450 nF(*)
Capacitance tolerances	±15%(*)
Operating temperature range	-55 to 125 °C
Storage temperature range	- 70 to 140 °C(**)
Temperature coefficient	+60 ppm/K
Breakdown Voltage (BV)	4.5 VDC
Capacitance variation versus RVDC	0.1 %/V (from 0 V to RVDC)
Equivalent Series Inductance (ESL)	Typ. 15 pH
Equivalent Series Resistance (ESR)	Typ. 30 mΩ to 120 mΩ (***)
Insulation resistance	100 GΩ @ 3 V, @ 25°C, t>120s, for 100 nF
Aging	Negligible, < 0.001% / 10000h
Capacitor thickness	85 µm
(*) Other values on request (**) w/o packing (***) value depends on products	

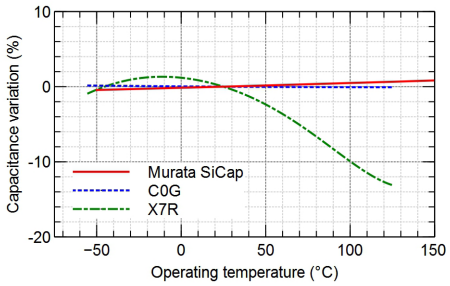


Fig. 1: Capacitance variation vs temperature (for UESL and MLCC technologies)

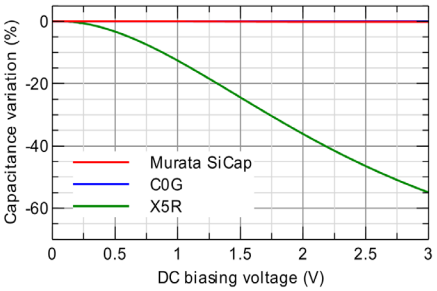
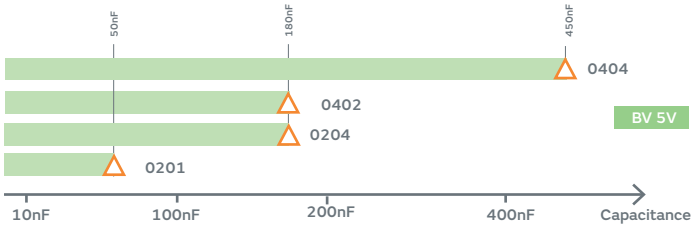


Fig.2: Capacitance variation vs DC biasing voltage @ BV 5 (for UESL and MLCC technologies)

Capacitance range



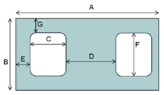
△ *Under development.*

Termination

Lead-free NiAu finishing compatible with automatic soldering technologies (reflow and manual). Other terminations available upon request.

Package Outline

	Case size		Pad dimensions (µm)				
	A	B	C	D	E	F	G
0402	1000	500	260	280	100	300	100
0204	500	1000	75	200	75	800	75
0201	600	300	100	200	100	150	75
0404	1040	1040	300	240	100	850	95
All dimensions in µm. Tolerance ±0.02 µm.							

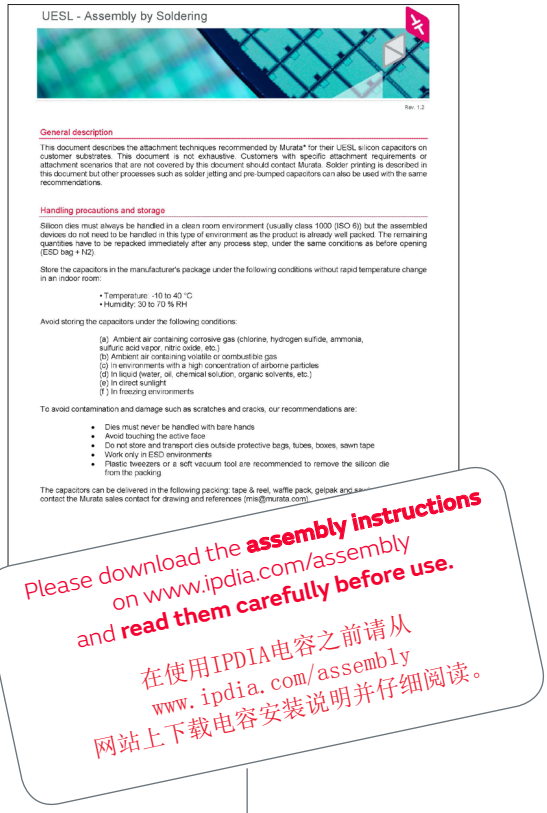


Packaging

Tape & reel or wafer delivery.

Assembly by Soldering

The attachment techniques recommended by Murata for the UESL capacitors on the customers substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata Silicon capacitors **please download the assembly instructions on www.ipdia.com/assembly and read them carefully.**



For UESL assembly instructions, please go to : www.ipdia.com/assembly and download the pdf file called **“UESL Capacitors - Assembly by Soldering”**

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