A 100 MHz, 91.5 % Peak Efficiency Integrated Buck Converter With a three-MOSFETs Cascode Bridge

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***Abstract*—High switching frequency DC–DC converters are present in many applications where wide regulation bandwidth and high efficiency are needed. A three-MOSFETs cascode bridge is presented to get full benefit from digital CMOS technology advancements, and a 3D assembly with a capacitive interposer is proposed for high frequency efficient decoupling. A test-chip is designed in 40 nm CMOS technology, validating the operation and the efficiency performance of the converter using the cascode bridge. An conversion efficiency of 91.5 % is demonstrated when converting 3.3 V to 2.4 V with a 150 mA load current, while switching at 100 MHz.**

***Index Terms*—Buck converter, DC-DC converter, cascode bridge, 3D assembly, capacitive interposer.**

I. Introduction

VOLTAGE conversion is a key enabler of large digital SoCs. The monolithic integration of the full power supply is the ultimate goal for achieving high performance conversion [1]. Particularly large digital SoCs demand many power domains with separate behaviors. Switched-capacitors are interesting when looking towards fully integrated DC-DC converters [2], and they can adapt to various consumption schemes. However, inductive converters generally enable higher power density than capacitive converters [3].

State-of-the-art of integrated, high frequency, inductive DC-DC converters can be presented in the form of various landscapes [4], using performance metrics. Some major trends appear. There is a major impact of both frequency and conversion ratio (defined as V_{OUT} /V_{IN}) on the converter efficiency. Converters manufactured using more advanced technologies tend to offer better efficiency but lower input voltages.

In order to take full benefit from technology shrinking at higher input voltage, it looks interesting to go for a cascode power stage. Figure 1 compares the 3.3 V and the 1.2 V MOSFET efficiency figure of merit, as well as the configuration with three 1.2 V MOSFET in series. Values have been normalized to the minimum R_{ON} value of the 3.3 V MOSFET. The conduction losses are proportional to the on-state resistance R_{ON}, and the gate drive losses to the $V_{GS} \cdot Q_G$ product. Diagonal lines are iso-losses for a given switching frequency and current. A set of three low voltage MOSFETs in series presents better performance figures than a single 3.3 V MOSFET.

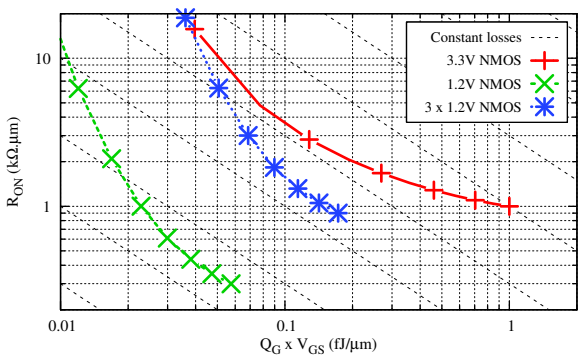

Fig. 1: Figure of Merit of NMOS transistors available in standard 40 nm digital CMOS bulk technology.

High frequency DC-DC converters using a cascode bridge with two MOSFETs in series have been proposed, demonstrating the interest of the structure in advanced CMOS [5]–[7]. A structure using three MOSFET in series is depicted in [8] but no implementation has been reported in literature so far.

Besides, main footprint contributors in inductive converters are still the passive elements. High switching frequency can be used to shrink these passive components by reducing their required values for proper decoupling. Using multiphase converter with coupled inductors is also beneficial for the power density/efficency trade-off as it allows to reduce the switching frequency or the phase inductance value at constant current ripple [9]. Going to a 3D assembly further reduces the overall footprint of the full converter. Appropriate control scheme can also helps reducing some passive components [10].

Based on all these considerations, a final design target for 100 MHz operation would be would be a 2-phase inductive converter with cascode bridge, in a 3D assembly, switching at high frequency [4]. The design case is classical motherboard to micro-controller core conversion. The targeted converter is a 3.3 V to 0.6-1.2 V, 300 mA output current, 100 MHz switching frequency inductive converter.

The paper focuses on the demonstration of the 3 MOSFETs cascode bridge feasibility. One phase is designed in a test-chip and assembled on top of a capacitive interposer, that embeds deep trench capacitors. Section II details the design of both the active and the passive part, along with some assembly considerations. Section III presents the measurement setup and the results obtained during characterization. A comparison

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with relevant state-of-the-art results is also presented.

II. Converter design

A. Active part

Full circuit schematic is depicted in Figure 2. Active part of the converter has been designed using a standard digital 40 nm bulk CMOS technology. Paper focus is the converter core operation in steady-state for demonstration of feasibility.

An external clock signal with a variable duty cycle is sent to the circuit. A level shifter generates three "voltage stacked" driving signals from the clock input – one between 0 V and 1.1 V, one between 1.1 V and 2.2 V and one between 2.2 V and 3.3 V. The level shifter also ensures proper synchronization of the driving signals, as well as a fixed dead-time in order to avoid short-circuit during switching. The optimization of dead-time is out of the scope of the paper. Using "voltage stacked" drivers allows for energy recycling on the drivers, as described in [8].

Except for the level shifter, all transistors in the circuit are core devices of the technology (40 nm gate length). The P-MOSFETs $P_{0,1,2}$ are acting as a single power MOSFET (macro-switch), being all opened or closed at the same time, having all the same width. The N-MOSFETs $N_{0,1,2}$ behave similarly. Each one of the power stage MOSFETs has its body connected to its source. This implies that the transistors $P_{1,2}$, $N_{1,2}$, N_{P2} and P_{N2} have a body with a moving potential during switching operation. This requires a triple-well isolation of the N-MOSFETs body.

The N-MOSFETs N_{P1} and N_{P2} are there to ensure a proper blocking of P_1 and P_2 respectively, by short-circuiting their gate and source. This ensure that each transistor of the $P_{0,1,2}$ macro-switch does not have more than 1.1 V across any terminals pair (gate-to-source, gate-to-drain and drain-to-source). The role of the P-MOSFETs P_{N1} and N_{P2} is equivalent, but for N_1 and N_2 blocking. The width of $P_{0,1,2}$, $N_{0,1,2}$, $P_{N1,N2}$ and $N_{P1,P2}$ has been optimized respectively for maximum efficiency using the global optimization tool under Cadence Virtuoso for an output voltage of 1.2 V and a load current of 150 mA, at 100 MHz.

Circuit is designed to use externally generated voltage references for testing purpose. This allows to measure the current drawn from each driver rail. In a further implementation these voltage rails could be generated internally using a switched-capacitor ladder 3:1 converter. Such a converter would benefit from deep trench capacitors embedded in the interposer.

Table I presents the current that each source is supplying as evaluated from post-layout simulation and during measurements. The current drawn from the driver sources is relatively small for 100 MHz operation, meaning that the charge recycling mechanism is effectively present.

B. Passive part

The converter benefits from a capacitive interposer manufactured by IPDiA [11]. The interposer helps to minimize interconnection parasitic elements (L and R) and embeds high density deep trench capacitors (≈200 nF/mm^2 with 3D PICS structure). The circuit requires five capacitors: a 33 nF (70 mΩ ESR, 330 MHz SRF – Self-Resonant Frequency) for input voltage decoupling, three 11 nF (150 mΩ ESR, 630 MHz SRF) for decoupling of driver supply voltages and a 16 nF (110 mΩ ESR, 490 MHz SRF) for output voltage decoupling. Some capacitors are also included on-chip using MOM capacitors: 1 nF for input and three times 300 pF for the drivers. The values of the capacitors are chosen to ensure a negligible voltage ripple (<10 mV) when the converter converter is operating at nominal power point, considering that the voltage sources are delivering a DC current – i.e. assuming large parasitic inductances between sources and the circuit.

TABLE I: Current drawn from each voltage source at 150 mA output load, 50 % conversion ratio.

	Post-layout simulation		Measurements	
	100 MHz	150 MHz	100 MHz	150 MHz
V_{IN} - power	82.38 mA	83.80 mA	83.91 mA	85.52 mA
V_{IN} - drivers	2.55 mA	3.70 mA	2.12 mA	3.10 mA
$2\,V_{IN}/3$ - drivers	−0.54 mA	−0.83 mA	0.10 mA	0.11 mA
$V_{IN}/3$ - drivers	2.51 mA	3.75 mA	2.16 mA	3.31 mA

The inductor used is an 0402 60 nH commercial SMD inductor from Coilcraft (PFL1005-60NMRx). Inductor DC resistance is 42 mΩ, with a 1.2 A saturation current and a 2.1 GHz SRF.

C. Assembly

The inductor and the IC are assembled on top of the capacitive interposer. The IC is flipped on the interposer, using a pad matrix for the interconnect to the interposer. The inductor is soldered on an 0402 landing pattern. A picture of the converter assembly is shown in Figure 3.

III. Measurements results

The goal of the measurement is to validate the proper behavior of the 3 MOSFETs cascode bridge and evaluate the efficiency of the DC-DC converter in steady-state and in CCM operation.

A. Tests setup

Figure 4 is a picture of the PCB utilized for testing. The assembly – IC and inductor on top of capacitive interposer – is wire-bonded on the PCB using 50 µm diameter gold wire. There are no additional passive components on the PCB, except two 10 kΩ resistors for purpose of clock input pull-down. Four voltage sources are connected to the converter. These sources are the input voltage and the three voltage sources for the drivers. The clock signal is generated externally. The load allows for constant output current testing.

B. Results

The converter is measured for various load currents, duty cycles and switching frequencies. Figure 5 shows the measured waveforms at the V_{LX} and the V_{OUT} nodes. These measurements are obtained at 100 MHz, 150 mA load current, 50 %

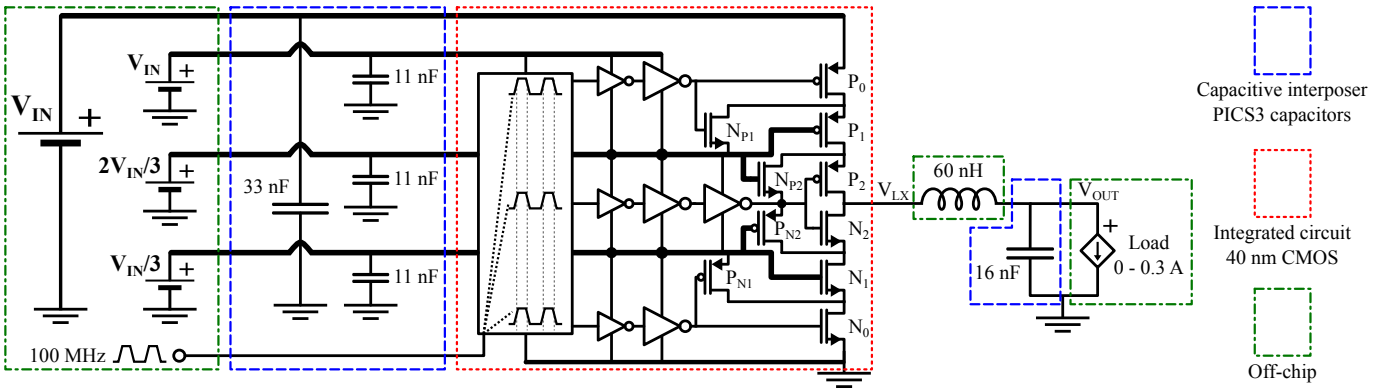

Fig. 2: Schematic of the circuit designed in 40 nm CMOS and experimentally verified.

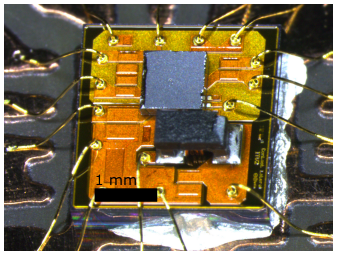

Fig. 3: Converter assembly.

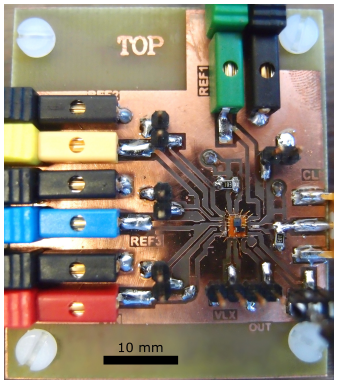

Fig. 4: Measurement test-board

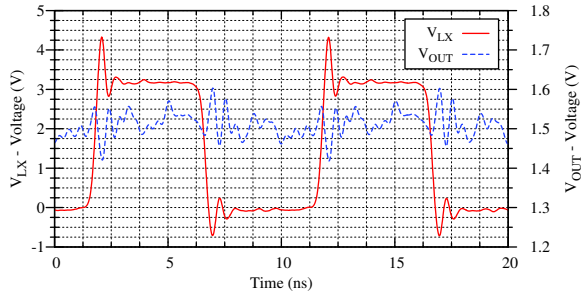

Fig. 5: Measured waveforms at the V_{LX} and V_{OUT} nodes of the converter, at 100 MHz, 150 mA load current, 50 % duty cycle.

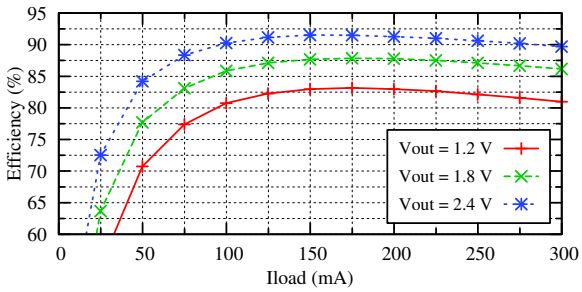

Fig. 6: Measured efficiency for various load current and output voltages, at 100 MHz.

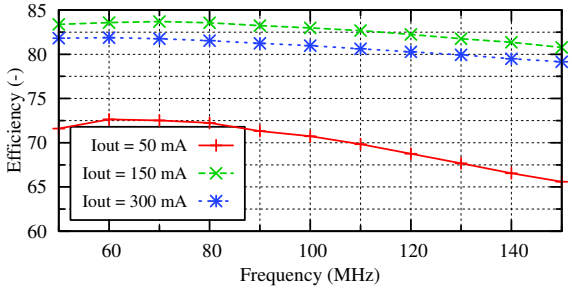

Fig. 7: Measured efficiency for various frequencies and load currents, at 1.2 V output voltage.

duty cycle using a high frequency active probe. These measurements confirm the proper operation of the three-MOSFETs cascode bridge. It behaves like a standard synchronous bridge.

The converter is then fully characterized in steady-state operation. Table I shows that measurement results are close to post-layout simulation results For the min voltage source, current is slightly higher in measurements than in PLS, because PLS doesn't include the inductor – because of post-layout simulation runtime issue. For the drivers, current measured is slightly lower when measured. When looking at output power, results are very close (400 µW difference on driver losses). When going from 100 MHz to 150 MHz, the losses of the drivers increase by 4.5 mW for both PLS and measurements, giving approximately 90 µW/MHz for driving the power MOSFETs (90 pJ per switching cycle).

Figure 6 presents the measured converter efficiency – including all losses except the close-loop circuit – variation with load current, for various output voltages. 91.5 % efficiency is reached while converting 3.3 V to 2.4 V and supplying 150 mA. At 1.2 V output voltage, an efficiency of 83 % is achieved. Figure 7 shows the evolution of the converter efficiency with the switching frequency for various load current values at 1.2 V output voltage. The efficiency decreases linearly with the switching frequency, except when it goes below 70 MHz, where it decreases for light load. This means that the losses due to current ripple are starting to be dominant.

A comparison with state-of-the-art is presented in figure 8.

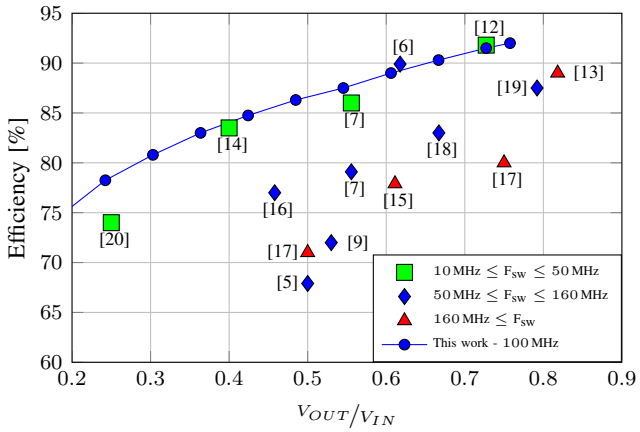

Fig. 8: Efficiency comparison with state-of-the art converters.

Efficiency is plotted across the conversion ratio of relevant state-of-the-art converters. The proposed converter features a very good efficiency across the whole range of conversion ratio. The use of the cascode bridge helps achieving high efficiency while handling 3.3 V input voltage.

IV. Conclusion

The design of integrated, high switching frequency converters in advanced technology processes is limited to low input voltages. This limitation reduces the interest of such converters as they can not benefit from technology enhancement and achieve high conversion efficiency. Using a cascode bridge for DC-DC conversion gives the full benefit of advanced technologies while handling a higher input voltage than the technology nominal voltage rating. The design of such a converter has been presented and its operating principle has been explained. Converter feasibility and performance have been validated using a test-chip in a 3D assembly context, with a capacitve interposer. Measurement results are in line with post-layout simulation, validating the interest of this kind of power stage for efficiency enhancement. Additional techniques such as using multiphase converters with coupled inductors are expected to improve the efficiency value.

Acknowledgment

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