Aerospace Performances of IPDiA -250°C up to 250°C Grade Silicon Capacitors

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Abstract
This paper covers technological results achieved with silicon capacitors for Aerospace applications, including stability, reliability and frequency data at high temperatures, as well as thermal stress, vibration & shock tests and radiations stress, according to ESA TRP reference (n° T723-325QT).

Keywords
Space evaluation capacitor, Radiation tests, high reliability capacitor, High temperature capacitor, Space grade capacitor, Space level capacitor, Cryogenic ultra low temperature down to 4 K, Miniaturization, High frequency performances.

Introduction

IPDiA silicon capacitors, already used extensively for a number of years in miniaturized high reliability equipment, show unique stability and reliability performances coupled with high temperature ratings and miniaturization in x, y axis, but also in z axis (low profile down to 100 µm thick) as well as extremely low total weight/µF. IPDiA R&D center, with the help of Alter Technology, is evaluating the Silicon Technology for Aerospace applications, under ESA TRP reference (n° T723-325QT).

The manufacture of IPDiA passive components is based on the PICS technology (Passive Integration Connecting Substrate). The benefits of this integrated passive silicon technology have already been demonstrated in terms of extremely high reliability, low leakage current, high stability, low aging and compliancy with high operating temperature. Due to their close integration to active components and innovative assembly technology, passive devices “on silicon die” offer significant improvements for signal integrity and space savings compared with the commonly used SMD components.

This paper reports on IPDiA high-density silicon capacitors for Aerospace applications, where miniaturization, weight saving with enhanced reliability are targeted. It presents some results on capacitance stability, voltage derating, leakage current, lifetime and electromagnetic compatibility.

Challenge of Miniaturization of electronics devices while increasing reliability

The most common trend in military & aerospace applications is reduction in feature sizes, while targeting higher reliability over performances, hence growing functionality and the overall content of electronics. In the passive components category, Multi-Layer Ceramic Capacitors (MLCC) are trying to follow this trend. According to several reliability models, it is proven that as capacitance per volume has increased, the long term reliability of the capacitor has been significantly impacted due to inherent MLCC technology (thinner layers of stack ceramic dielectric & electrode thickness) (See graph below).

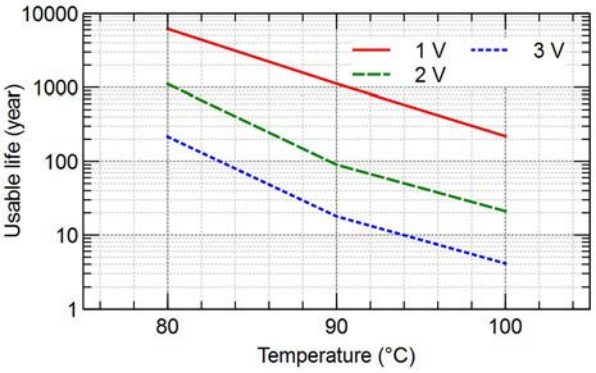


Figure 1a: MLCC usable life vs temperature

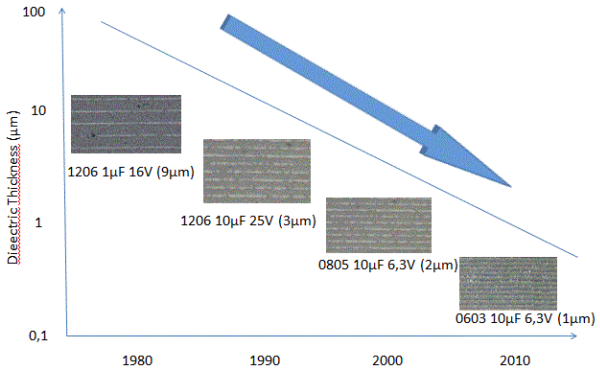


Figure 1b: Dielectric thickness evolution over the years

Going forward, reliability concerns impacting Military & Aerospace roadmaps are posing an increased risk for applications using decoupling MLCCs. As this race to more and more miniaturization in Military & Aerospace

devices is the daily concern of electronic designers, where increasingly compact devices are required in order to minimize their volume and weight in the final system, and as it has been shown above that MLCC reliability is reaching its limits, the next step into miniaturization and integration solution is high-density silicon capacitors.
IPDiA Silicon capacitors are a solution to reduce the dimensions of the electronic board. These capacitors in ultra deep trenches have been developed and implemented in a process called PICS (Passive Integration Connective Substrate) in order to integrate passive components such as resistors, accurate planar MIM capacitors and trench MOS capacitors for numerous applications, such as switched capacitor voltage multiplier or buck converter, decoupling and filtering. This process provides a fully CMOS-compatible solution for integration on chip or multiple chip modules. Its potential for miniaturization means smaller component size, reduced manufacturing costs per product, low power consumption and integration of more basic functions into a single product (figure 2).

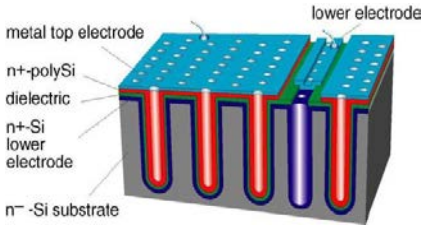


Figure 2: Schematic of a PICS capacitor

The capacitors are manufactured in etched arrays of macropores by reactive ion etching with high aspect ratios of up to 60 with a typical width of 1 µm. A range of high temperature and/or low profile silicon capacitors using this technology has thus been specifically developed. The following table shows some of the capacitance vs size & weight achievements vs MLCC.

Capacitance	Case size	Sicaps Weight	MLCC Weight
10 nF	0201	0.13 mg	0.9 mg
100 nF	0402	0.23 mg	1.6 mg
330 nF	0603	0.56 mg	6.6 mg
470 nF	0805	0.88 mg	20 mg
1 µF	1206	2 mg	51 mg
3,3 µF	1812	6 mg	195 mg
4,7µf	2016	7 mg	NA

Table 1: IPDiA Sicaps weight vs MLCC weight

Challenges for Airborne RF applications

IPDiA Silicon capacitors - for example the Extreme Range EXSC (-55°C/+250°C) - with Oxide/Nitride/Oxide dielectric stacks and polysilicon top electrodes yield a capacitance density of 250 nF/mm², an electrical breakdown voltage of 11 V and very low leakage current (< 0.5 nA at the working voltage and room temperature).
They also show tunable low loss factors (equivalent series resistance ESR < 10 mΩ and equivalent series inductance ESL < 100 pH) which improve significantly the RF performances of the devices due to these extremely low parasistics (figures 3 & 4). This allows Silicon technology to be perfectly suitable for Power GAN RF devices, multiple array active antennas or airborne GPS navigation systems.

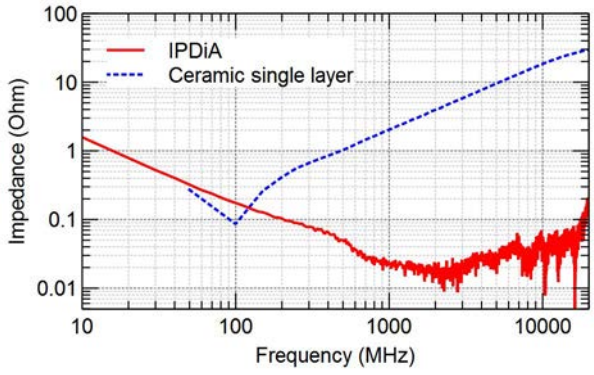


Figure 3: Comparison of MLCC Impedance vs Sicaps

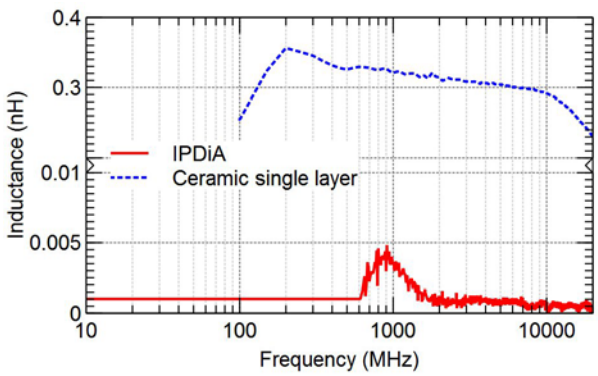


Figure 4: Comparison of MLCC ESL vs Sicaps

As mentioned previously, Military & Aerospace electronic components need to withstand extremely harsh conditions throughout their lifecycle. The following paragraphs will show the results obtained with IPDiA silicon capacitors in terms of capacitance stability, voltage derating behavior and leakage current.

Capacitance stability over temperature. Deratings no longer required

The 3D Silicon Capacitors developed by IPDiA for harsh environment are compatible with operating temperatures demonstrated from -250°C up to +250 °C. The temperature dependence of capacitance is expressed in parts per million (ppm) per °C. A linear function is obtained even at extreme temperatures (see Figure 5). The temperature coefficient is positive and equal to + 62 ppm per °C. The capacitance variation of a 1616 3.3µF capacitor is around 1.5 % from room temperature to +250 °C.

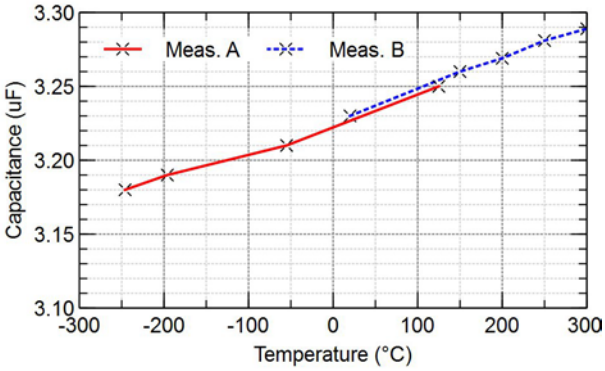


Figure 5: Capacitance dependence on temperature for an EXSC capacitor, 1616 3.3µF

Silicon capacitors offer very stable performance compared with typical MLCC components. The IPDiA 3D Silicon capacitor also exhibits highly stable capacitance as a function of temperature and voltage (see results on figure 6 plotted at 3 temperatures -55°C, 125°C and 200°C).

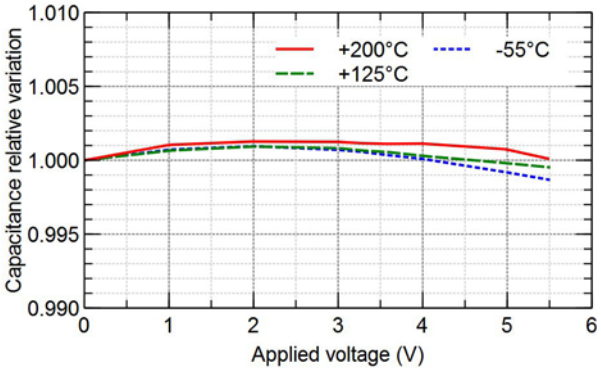


Figure 6: IPDiA Sicaps capacitance relative variation vs voltage @ -55°C, 125°C and 200°C

At temperatures above 150°C, the X7R and X8R capacitors suffer from severe reduction in capacitance and degradation of reliability performance, especially under DC bias conditions. In order to avoid reliability issues when using MLCC, one approach commonly used is to apply a voltage derating factor of at least 3. This means that very high rated voltage capacitors (i.e. 50 V) must be designed for a typical operating voltage of 10 V. Voltage derating improves MLCC reliability, but generates a significant overspecified voltage, hence bigger case size and therefore poor miniaturization. In order to confirm the compatibility of the EXSC series with Aerospace applications, reliability data have been obtained by testing the lifetime of a 100 nF 0605 capacitor. Time-Dependent Dielectric Breakdown (TDDB) measurements are used to model the intrinsic behavior of the capacitor dielectric under elevated temperature and strong electric fields. The acceleration factors for temperature and electric field are used to extrapolate the capacitor lifetime under typical operating conditions. IPDiA technology can solve this miniaturization issue. Derating is no longer even required, in fact, as the PICS3HV EXSC range is

specified to operate at 250 °C continuously, under 10 V for more than 50 years. As a comparison, X8R capacitors show a useful life of 1 year at 125 °C at the rated voltage. The results are shown on Figure 7.

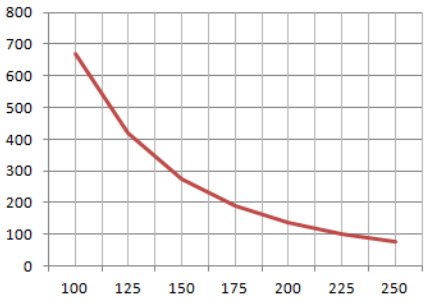


Figure 7: Lifetime vs temperature

Leakage current concern at high temperature

Leakage is currently one of the main factors limiting performance at high temperature. The leakage current must be measured under a range of time, voltage, and temperature conditions. The leakage current of an IPDiA XTSC 0402 100 nF capacitor was measured after 120 s stabilization at 3,3 V. The results at 25 °C and 300 °C are given in table 2. Even at 300 °C (Fig 8), the leakage current does not exceed 2 nA. This is a very impressive result compared with the other high temperature capacitors available on the market which demonstrate, when they are still functional, a leakage current 1000 times higher.

Capacitance	Case size	Leakage current (pA) @ 85 °C	Leakage current (nA) @ 300 °C
100 nF	0402	< 10 pA	< 2 nA

Table 2: Leakage current at temperature up to 300 °C

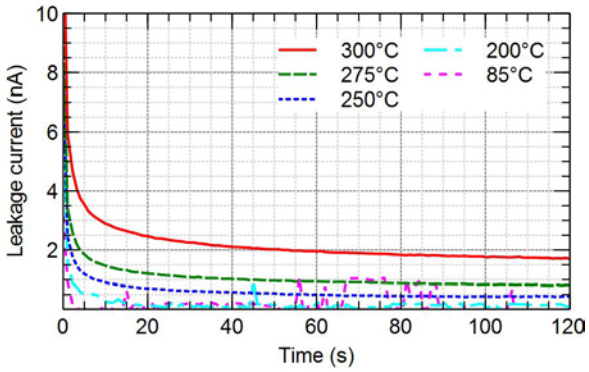


Figure 8: Variation of leakage current over the temperature range of 25°C to 300°C

This ‘leakage current’ through the dielectric is usually converted to the expression "insulation resistance" by using Ohm's law. The Insulation Resistance (ΩF) of the IPDiA 3D Silicon capacitors is compared with NPO/COG dielectrics and the result is shown in Figure 9. The 2 orders of magnitude observed between the 2 types of capacitor are primarily due to the type of dielectric used. The thickness of the dielectric and the magnitude of the charge voltage have a comparatively minor effect on the leakage current. The effect of the insulation resistance value is quite critical in circuitry where leakage of current through the capacitor can cause a malfunction or undesirable results. Prime examples of this type of application are those involving DC and low AC frequencies in most blocking, coupling, and timing circuits.

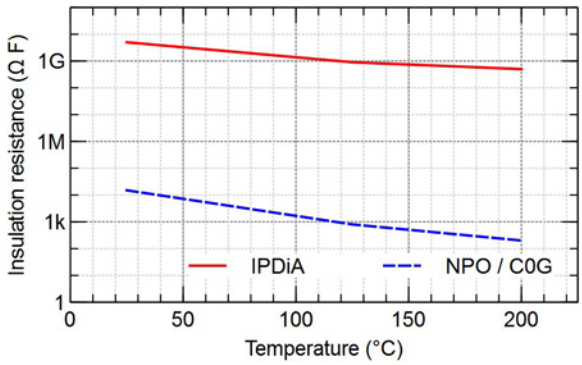


Figure 9: Typical insulation resistance (ΩF) over the temperature range of 25 °C to 200 °C

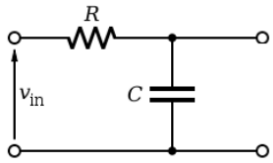
Assembly, vibration & shock

According to MIL-STD-750, Rev D, method 1051, which refers to thermal cycling caracteristics for bare silicon dies (such as ICs or Silicon capacitors), IPDiA performed 300 cycles (5°C/min) from -65°C/+200°C, which places the technology well above condition MIL "D" (100 cycles from -65°C/+200°C). As previously mentioned, Alter Technology, according to ESA contract reference 400010740/NL/SFe, performed mechanical tests (vibration and shock) with 3 boards. For vibration, the capacitors were subjected to Tests 'Fc' of IEC Publication No. 68-2-6 and for shock, test 'Ea' of IEC Publication No. 68-2-2. In the latter case, each of the boards supported shocks in a different perpendicular axis (X, Y & Z). Capacitor leakage currents and electrical quantities such as capacitance and tangent of the loss angle were measured. After tests, 100% of the capacitors were inside the leakage current electrical tolerance after vibrations & shocks.

Radiation performances

Furthermore, Alter Technology populated a custom board with several capacitors of different technologies (PICS3, PICS3HV), to be submitted to total dose radiation.

The silicon capacitors were mounted according to schematic [1] below, under 3 V, with a 1 Mohm Resistor.



Schematic 1

The radiation tests were performed at Radlab in Seville from June 2015 till August 2015. The following table [3] shows the estimated cumulative dose deposited in the components.

EXPERIMENTAL STEPS	1	2	3	4	5	6	7
PROCESS	Irrad.	Irrad	Irrad.	Irrad.	Irrad.	Ann	Ann
Dose [krad (Si)]	**9.29**	**13.60**	**41.77**	**36.96**	**93.58**	-	-
Cumulative Dose [krad (Si)]	**9.29**	**22.89**	**64.65**	**101.61**	**293.49**	-	-
Dose Rate [rad(Si)/h]	**196,4**	**196,4**	**196,4**	**196,4**	**196,4**	-	-
Temperature (°C)	**25,0**	**25,0**	**25,0**	**25,0**	**25,0**	**25,0**	**100,0**

Table 3: Radlab ^{60}Co gamma cumulative radiation dose received by the boards

After these total dose radiation tests, the capacitors were exposed to 293.49krad. 24 hours after end of the tests, all electrical quantities were measured and inside the operational range [courtesy of Alter Technology Madrid].

SEE radiations

The IPDiA silicon capacitors have shown a low sensibility to ion effects when the working voltage is at its rated voltage or less (5.5 V). In these conditions, the samples have been tested up to 62.5 MeV cm^2/mg without failures. The capacitors do not show any effects with low LETs (3.3 & 10 MeV cm^2/mg), even working at breakdown voltage (11 V).

LET (MeV cm^2/mg)	Flux (ion/s cm^2)	Bias Conditions Capacitor (V)							
		1	3	5	5.5	6	7	9	11
3.3 (Ne)	100 up to 1e5	OK	OK	OK	OK	OK	OK	OK	OK
	1000 up to 1e6	OK	OK	OK	OK	OK	OK	OK	OK
	10000 up to 1e7	OK	OK	OK	OK	OK	OK	OK	OK
10.0 (Ar)	100 up to 1e5	OK	OK	OK	OK	OK	OK	OK	OK
	1000 up to 1e6	OK	OK	OK	OK	OK	OK	OK	OK
	10000 up to 1e7	OK	OK	OK	OK	OK	OK	OK	OK
20.4 (Ni)	100 up to 1e5	OK	OK	OK	OK	OK	OK	OK	
	1000 up to 1e6	OK	OK	OK	OK	OK	OK	OK	
	10000 up to 1e7	OK	OK	OK	OK	OK	OK	OK	
32.4 (Kr)	100 up to 1e5	OK	OK	OK	OK	OK	OK		
	1000 up to 1e6	OK	OK	OK	OK	OK	OK		
	10000 up to 1e7	OK	OK	OK	OK	OK	OK		
62.5 (Xe)	100 up to 1e5	OK	OK	OK	OK	OK			
	1000 up to 1e6	OK	OK	OK	OK				
	10000 up to 1e7	OK	OK	OK					

Conclusion

The electrical properties of the IPDiA 3D Silicon capacitors over the entire temperature range from -250°C to +300°C were presented in this paper.The capacitance dependence on DC bias and temperature exhibits almost flat response and the reliability is maintained at a very high level with 1 FIT at 225°C (more than 105 lower than the competition).The leakage current is very low and the insulation resistance is still above 1 ΩF at 300°C. Low parasitic characteristics make this technology extremely popular in airborne RF applications. IPDiA technology offers a very high capacitance density, typically 250 nF/mm² in production, enabling large capacitor values in extremely small form factors, hence achieving major downsizing in overall size & weight requirements. In Hi-Rel applications - requiring miniaturization while improving overall reliability performances - IPDiA Silicon capacitors must be considered in future Mil-Aerospace applications.