Analysis of Ultra large band Wire bondable vertical Silicon Capacitors Performance in a GaN power amplifier

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Abstract — This paper presents Ultra large band Wire bondable vertical Silicon Capacitors (UWSC) performances in high-frequency high-power applications up to 26GHz. These capacitors combine ultra-deep trench MOS capacitors of few nF and single layer MOS capacitors of few 10's pF in a single package. The performances of these capacitors have been compared to conventional commercialized vertical capacitors. The benefits to use these capacitors are quantified thanks to their integration in a power amplifier.

Index Terms — silicon capacitors, ceramic capacitors, power amplifiers, integrated passive devices, high density silicon capacitor, low ESR and ESL, PICS™ technologies, memory effects.

I. Introduction

The UWSC capacitors are suitable for DC decoupling, DC noise cancellation, matching networks and harmonic / noise filtering functions in all RF, microwave, and millimeter-wave power applications for wireless communication, radar and data broadcasting systems. This technology provides industry-leading performance particularly in terms of capacitor stability over the full operating DC voltage & temperature range. In addition, intrinsic properties of the silicon lead to a low dielectric absorption and a close to zero piezo electric effect resulting in no memory effect. This Silicon based technology is RoHS compliant.

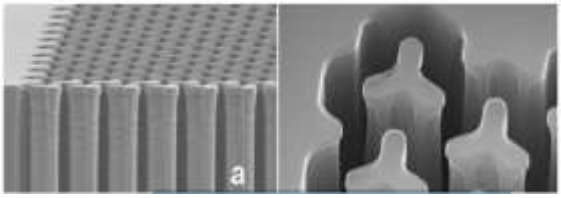
II. UWSC Capacitors Building

The SiCap technology of IPDiA with advanced 3D topology is comparable to a total area of 80 ceramic layers. The use of a very efficient silicon based dielectric avoids the compromise between capacitance value and electrical performance.

These high density 3D capacitors make up the beating heart of the IPDIA PICS™ technologies: the combination of patented [1] high aspect-ratio micrometric 3D structures (50:1 pores or trenches, drilled in the silicon by Deep Silicon Reactive Ion Etching, see Figure I) with standard dielectrics (silicon oxide and/or nitride) from the semiconductor industry in single (or multiple) Metal Insulator Metal (MIM) architectures (Figure II) enables the process of capacitors with densities as high as 250 nF/mm².

3D trench capacitors, as shown in figure I, provide outstanding density integration performances as well as remarkable electrical characteristics (low ESR, ESL) thanks to the individual components proximity and layout flexibility inside the circuit, compared to external components described in [2], [3], [4], [5].

Figure I
Cross-sectional SEM images of 3D MOS embedded trench capacitor manufactured by IPDiA



These Si capacitors in ultra–deep trenches enable the integration of high capacitance density from 1.3nF/mm² to 250nF/mm², as shown in figure II (with a break-down voltage of respectively 450V to 11V). A dielectric stack of silicon nitride and silicon dioxide associated to an N-type very low-ohmic silicon substrate are used to produce these small devices.

Figure II presents the capacitance densities currently available at IPDIA. The increase in minimum break-down voltage from one generation to the next one is the combination of advances in dielectric material deposition, etching techniques, and device geometry to keep the highest capacitance density versus voltage.

Figure II
UWSC capacitance density versus min break-down voltage

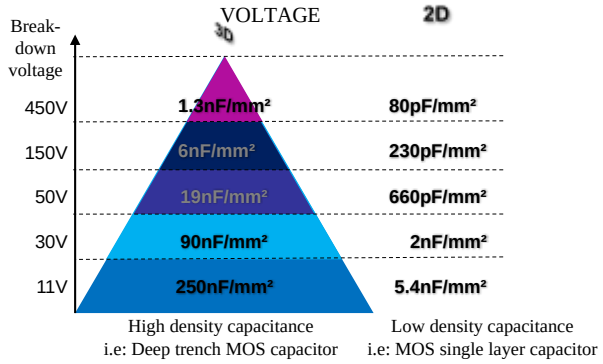
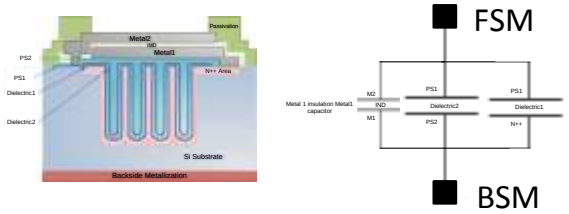


FIGURE III

On the left: cross sectional view of the MIMIM ARCHITECTURE USED IN THE IPDIA PICS™ TECHNOLOGY. On the right: SCHEMATIC (VOLUNTARY SIMPLIFIED) OF THE CAPACITORS PARALLELIZED IN A MIMIM ARCHITECTURE TO OFFER A HIGHER CAPACITANCE VALUE THAN IN SINGLE MIM IPDIA PICS™ TECHNOLOGIES

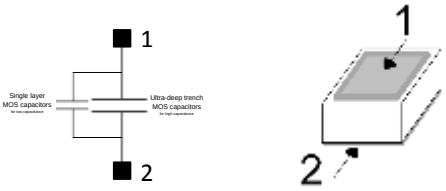


As in figure III, $C_{TOTAL} = C_{MIM} + C_{PS1\text{-}PS2} + C_{PS1\text{-}N++}$

In this paper, the 19 nF/mm² capacitance density node is considered. For this technological node, both electrodes are connected to a first aluminum metal layer and then to a second aluminum metal layer. The number of contacts to the capacitor electrodes is maximized to reduce resistive losses. This UWSC Capacitor combines ultra-deep trench MOS capacitors for high capacitance value of 10 nF and single layer MOS capacitors for low capacitance value of 100 pF, both in a 0303 package size.

FIGURE IV

10nF//100pF-0303 UWSC CAPACITOR BLOCK DIAGRAM AND 3D VIEW OF UWSC CAPACITOR PIN CONFIGURATION



III. UWSC CAPACITORS STABILITY OVERVIEW AND RF CHARACTERIZATION

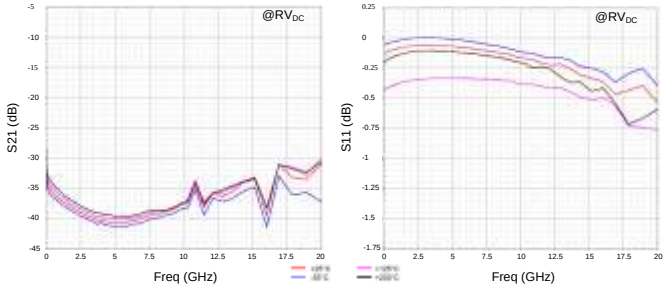
These devices exhibit high Q-factor (low ESR < 14 mΩ), very high self-resonance frequency (SRF) (low ESL < 6 pH), very low capacitance change over temperature and voltage variation (respectively Graph I: +/-0.5% from -55°C to +150°C and Graph II: 0.02%/V) as well as a very high reliability and low leakage current. The dielectric stack deposited using a high temperature process (900°C) is leading to an excellent uniformity and stability of the capacitance value, and also to a memory effect close to zero. Moreover, the silicon substrate brings low dielectric absorption leading to almost no piezo effect as shown in table I.

FIGURE V: UWSC capacitor test bench

Temperature and voltage measurements show that UWSC capacitors behave as robust devices in various configurations. For instance, the ΔC/C variation is lower than 80 ppm/°C in the –50 °C/+150 °C temperature range. As shown in Graph I for the case of a 10nF//100pF UWSC capacitor, ΔC/C variations are linear over temperature.

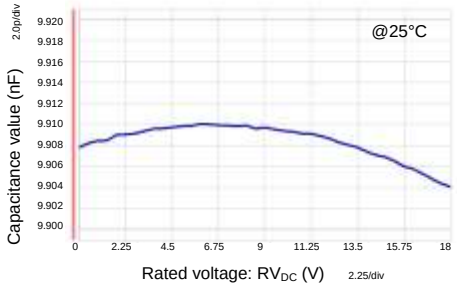
GRAPH I

S-PARAMETER OF 10NF//100PF - 0303 UWSC CAPACITOR VERSUS OPERATING TEMPERATURE AND FREQUENCY: 0.5%



GRAPH II

10NF//100PF - 0303 UWSC CAPACITANCE VALUE VERSUS RATED voltage: 0.02%/V



Concerning the variation over the voltage range, the ΔC/C of a 10nF//100pF UWSC capacitor is lower than 0.2 % for a 18 V to +18 V voltage variation.

TABLE I

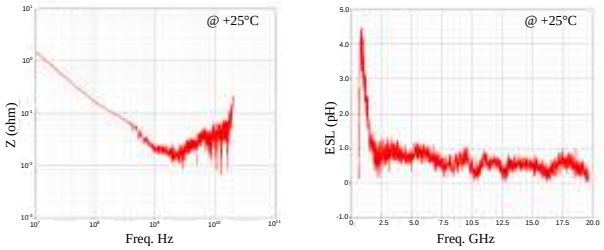
DIELECTRIC ABSORPTION COMPARISON

Type of capacitor	Dielectric absorption
Class-1 ceramic capacitors, NP0	0.6%
Class-2 ceramic capacitors, X7R	2.5%
Silicon capacitors	0.1%

Thanks to our Silicon substrate, our UWSC capacitors have at least 6 times lower dielectric absorption than ceramic capacitors.

GRAPH III

10nF//100pF - 0303 UWSC IMPEDANCE AND ESL CHARACTERISTIC VERSUS FREQUENCY IN SHUNT MODE



Graph III shows the extracted ESL values resulting in shunt mode. This measurement mode allows to mathematically eliminate the extrinsic parasitic elements like wire bonding without de-embedding them; only a de-embedding of access line is needed.

TABLE II
10nF//100pF - 0303 UWSC CAPACITOR PERFORMANCES

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value		-	10	-	nF
L	Capacitor length	±0.01mm		0.8		mm
W	Capacitor width	±0.01mm		0.8		mm
h	Capacitor heigth	±0.005mm		100		mm
T_{OP}	Operating temperature		-55	20	150	°C
DC_T	Capacitance temperature variation	-55°C to 150°C	-0.5	-	+0.5	%
BV	Breakdown Voltage		50	-	-	V
DC_{RVDC}	Capacitance voltage variation	From 0V to RV_{DC}	-	-	0.02	$\%/V_{DC}$
IR	Insulation resistor	@ 25°C & RV_{DC}	10	-	-	GΩ
ESL	Equivalent Serial Inductance	@ SRF	-	-	6	pH
ESR	Equivalent Serial Resistance		-	-	14	mΩ

The self-resonance frequency (SRF) can then be simplified as follow:

$SRF = \frac{1}{2\pi\sqrt{ESL.C}}$ where C is the capacitance value of capacitor and ESL is the Equivalent Serial Inductance.

The extracted ESL including the top electrode interconnect is approximately 6 pH for a 10nF//100pF UWSC capacitor, resulting in a frequency resonance close to 1 GHz, thanks to appropriate interconnect strategy chosen. When the ESL is lower, the SRF is higher. Therefore, a capacitor can be used to provide capacitive impedance for a higher frequency range.

IV. UWSC CAPACITORS COMPARISON

GRAPH IV
10NF//100PF - 0303 UWSC IMPEDANCE AND ESL COMPARISON VERSUS CERAMIC CAPACITOR

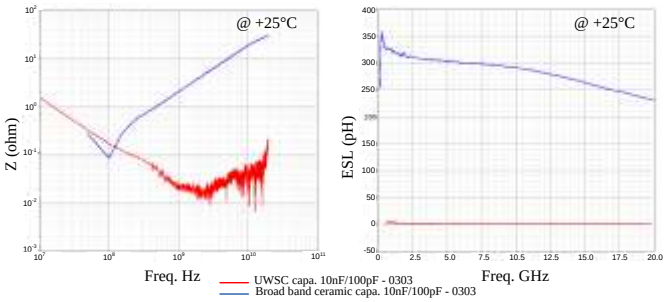


TABLE III
CAPACITORS COMPARISON

Symbol	Parameter	Conditions	UWSC	Cer. Capa.	Unit
C	Capacitance value		10nF//100pF	10nF//100pF	nF
ESL	Equivalent Serial Inductance	@ SRF	6	350	pH
ESR	Equivalent Serial Resistance		14	100	mΩ

To confirm the out-coming results, the performance of the UWSC capacitor has been compared to two conventional commercialized 10nF//100pF vertical ceramic and silicon capacitors.

Graph IV shows that the intrinsic parasitic elements in broadband ceramic capacitors is too high in the 0303 case size compared. The silicon capacitors from competitors don't allow to achieve 10nF in 0303, but only a few of 100pF.

V. EXAMPLE OF UWSC CAPACITORS INTEGRATION WITH MOS POWER AMPLIFIER

The high-frequency communication infrastructure market, including base stations for mobile communications and broadband capable wireless systems continuously expand.

As the designs of circuit modules become smaller and require lower power consumption, lower-profile and high-frequency low-loss (low ESR & ESL), capacitors are necessary for equipment related to these applications.

FIGURE VI
CIRCUIT APPLICATION OF CELLULAR BASE STATION AMPLIFIER

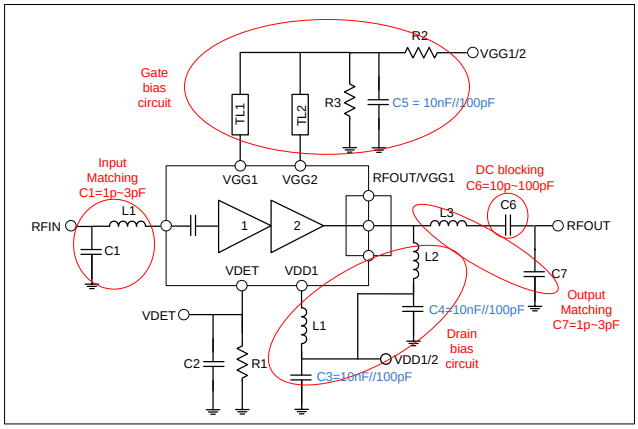


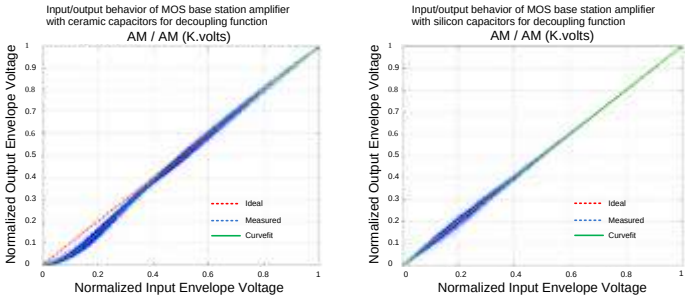
Figure VI shows an example of amplifier circuits used for the base stations of mobile communication systems. Since UWSC capacitors have low intrinsic parasitic elements, high capacitance density and use a silicon base substrate, they are the most adequate capacitors for the ultra large band decoupling function in these applications. In most cases, for the decoupling function the UWSC capacitor resonates with either coils or resistors and can produce resonance at a specific high frequency.

Measurement Results:

The base station MOS power amplifier for WCDMA, is running at 35% PAE, Pout = 30.9 W, with 9.98 dB gain. The sequence RMS error was 3.5% with ceramic capacitors and typically below 2.7% afterwards using UWSC capacitors (without intrinsic memory effect).

GRAPH V

INPUT/OUTPUT BEHAVIOR OF MOS BASE STATION AMPLIFIER.



Nevertheless, the UWSC low capacitance density with only single layer MOS capacitors can be used for impedance matching and DC blocking functions.

For impedance matching function

A UWSC capacitor is connected to a circuit in parallel or in series in order to match the transistor input and output. A product with narrow deviation capacitance can be used to reduce the reflection characteristic.

For DC blocking function

When circuits are coupled, a UWSC only passes the signal by cutting the direct current portion. Because a UWSC capacitor has low signal loss and high voltage resistance, it is suitable for high power circuits. Meanwhile, its low self-heat generation can increase its power capacity.

VI. CONCLUSION

The UWSC Capacitors from IPDiA show high power, broadband frequency, lifetime, miniaturization and performance stability and are therefore ideal for demanding applications such as wireless communication, radar and data broadcasting systems. The very last large band vertical PICS™ process generations can propose a large range of break down voltage while preserving an interesting capacitance density with broad band performances without any equivalence.

This paper has highlighted the memory effects contribution from decoupling ceramic capacitors of an RF power amplifier, which is solved by replacing them by decoupling UWSC capacitors.

Developments are now focused on extending “Large band vertical process” to larger elements and to demonstrate co-integration resistance and inductance intended to be used in the field of the high frequency DC/DC conversion or wideband filtering/matching networks.

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