

# New Ultra Low ESR Mosaic PICS Capacitors For Power Conversion

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**Abstract**—This paper presents a new architecture of capacitive elements (MOSAIC), where the global capacitance is constructed out of a massive network of parallelized elementary cells. Electrical measurements in the RF domain are presented and show a very low ESR results combined with a high stability versus frequency up to hundreds of MHz. Being given that there is a trend towards higher frequencies for DC-DC converters and taking into account the electrical performances combined with the design flexibility, this paper demonstrates the benefits of using such Mosaic PICS capacitor for power conversion applications. These Mosaic trench capacitors could be a part of an IPDiA silicon interposer on top of which magnetic inductors and Power Management Integrated Circuits (PMIC) are flip chipped. Thick copper routing (up to 12 $\mu$ m) is used to connect the passive components to the PMIC.

**Keywords**—PICS technology; ultra low ESR; high density silicon interposer; integrated passive devices; High frequency Power Conversion; High stability ; RF domain;

## I. INTRODUCTION

New concepts for power management have emerged, based on granular system architecture where networked ICs are using on-chip power regulation. Advantageously, each IC adapts its supply voltage to continuously optimize its power consumption accounting for activity.

This implementation requires miniaturized local DCDC regulators, integrating low profile capacitors and thin film magnetics, achieving sufficient electrical performances for conversion efficiency above 90%. The Passive Integration Connective Substrate (PICS) silicon based capacitor technology developed by IPDiA [1], is a good candidate for DCDC converters applications operating in the 10MHz/100MHz+ domain (figure Fig.1), at which point the footprint of the power passives and the on-chip DC-DC converter blocks becomes comparable (~1mm<sup>2</sup>).

In this frequency domain, the Equivalent Serial Resistance and Equivalent Serial Inductance performances of the silicon integrated capacitors are very critical for conversion efficiency and voltage stability. It is therefore essential to develop a capacitor architecture allowing sufficient freedom to tune the capacitors ESR and ESL.

We present in this paper, a new architecture of capacitive elements (MOSAIC), where the global capacitance is constructed out of a massive network of parallelized

elementary cells. The parallelization is obtained by leveraging the sub-micronic lithographic capability of the PICS process. Physical model is developed, allowing predicting the electrical behavior of any larger MOSAIC capacitive networks. Finally, to illustrate this concept, we present the electrical characteristics in the RF domain (300Khz-1Ghz) of a set of PICS MOSAIC capacitors designed with this approach. The benefit in term of component parasitic (ESR/ESL) is discussed and compared to the prior art. The simulation results are compared to the experimental characterization and are demonstrating an excellent agreement.

In conclusion, we present typical application schemes for those MOSAIC capacitors in the field of the high frequency power conversion.

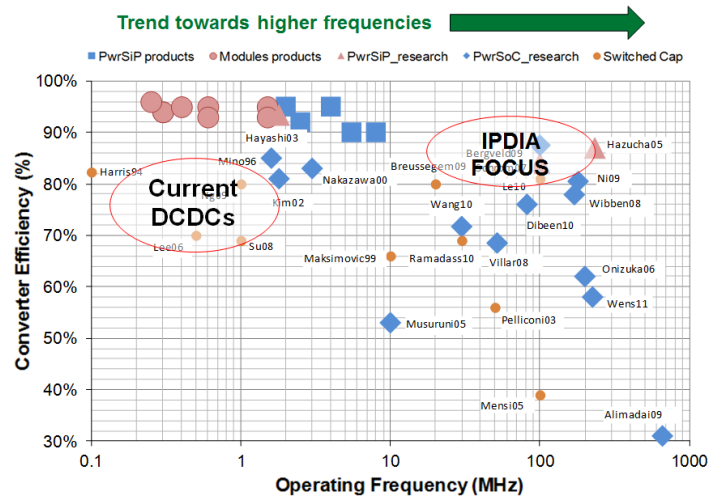


Fig. 1. IPDiA Focus Plan

## II. MOSAIC PICS CAPACITOR

The standard way to design PICS<sup>TM</sup> capacitors consist in defining a block of high aspect-ratio 3D micrometric structures [2] (i.e. tripods for the PICS3<sup>TM</sup> process) that enable to reach the specified value and then in sizing the required areas for contacting the three electrodes from the MIMM architecture (see figure Fig.2). These contact dimensions are defined according to each electrode

material sheet resistor with the objective to maximize capacitance density while maintaining contact areas large enough to obtain reasonable ESR (i.e., in the 100m $\Omega$  range for a 1 $\mu$ F capacitor).

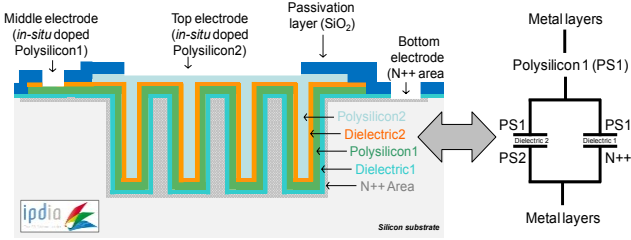
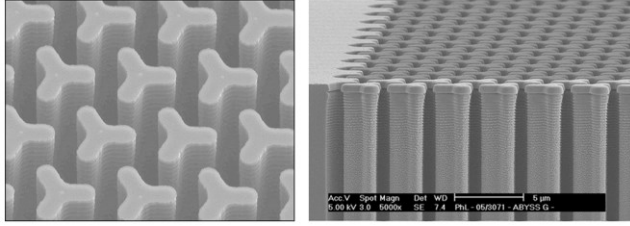


Fig. 2. SEM micrographs example of the high aspect-ratio structures etched in the silicon substrate / cross sectional view of the MIMIM architecture and its simplified equivalent schematic

With this style of design, the current is mostly flowing in the electrodes along large distances to reach individual PICST<sup>TM</sup> pores. As a consequence the ESR is driven by the capacitor shape/outer extend and the ESR is hardly tunable by design. As explained in the following, the Mosaic design overcomes this issue with a global capacitor element designed as a grid of localized capacitors elements that are all parallelized.

#### A. Structure Presentation

With this approach, the design of the localized element can be tuned to match any requirements in term of ESR or Capacitance (C). Indeed:

- The global capacitor targeted value C, is correlated to the number N of localized elements to be parallelized on the grid such that the capacitance value of the localized element is C\*N (see figure Fig.3)
- The global ESR target taken as a function of 1/N that is forcing the ESR of the localized element
- The ESR of the localized element being correlated to the local density of metallization contact to capacitor electrodes

This approach has several obvious advantages among which a perfect scalability, and a lower sensitivity to electrode quality (i.e. resistivity) as long as contact are

provided locally, resulting in a lower ESR and constant contact density overall the structure. In other words, the more the elementary cell repetition (i.e. the higher N), the higher the device capacitance and the lower the device resistance and inductance.

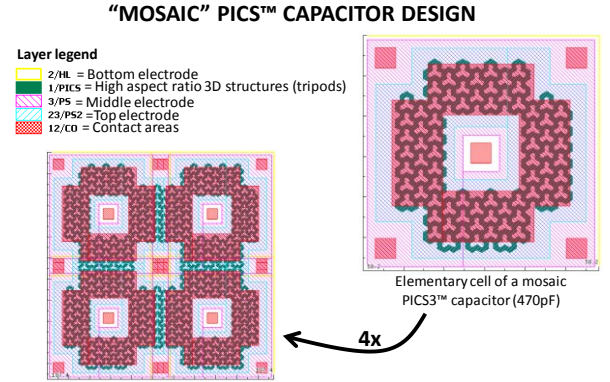


Fig. 3. 58.2 $\mu$ m\*58.2 $\mu$ m elementary cell of a mosaic-style PICS3<sup>TM</sup> capacitor (420pF)

#### B. Optimal cell calculation

As mentioned in the previous paragraph, there is a direct correlation of the ESR to contact density. Then, the design and optimization of the elementary cell is very important. The objective is to find an appropriate cell sizing that provides:

- Sufficiently low intrinsic ESR capability when repeated N times in parallel to meet ESR target.
- The lowest possible contact density to meet the target.
- 1/1 aspect ratio cell

It is expected that Self Resonance Frequency (SRF) should be independent from C scaling (as long as LC product is nearly constant) and thus be only a function of the localized element design. Same reasoning applies to the cutoff frequency as long as the RC product remains also constant.

### III. PHYSICAL MODEL

To understand the frequency behavior of the capacitors, a physical model is developed, allowing predicting the electrical behavior of any larger MOSAIC capacitive networks.

#### A. Modeling Methodology

Mosaic capacitor is considered as three levels structure: placing together tripods forms a cell then placing and connecting together these cells forms the capacitor. Based on this reasoning, three level modeling is adopted. As shown in figure Fig.4, an electrical model is established for each level

and takes into account the geometry parameters as well as the interdigitated access.

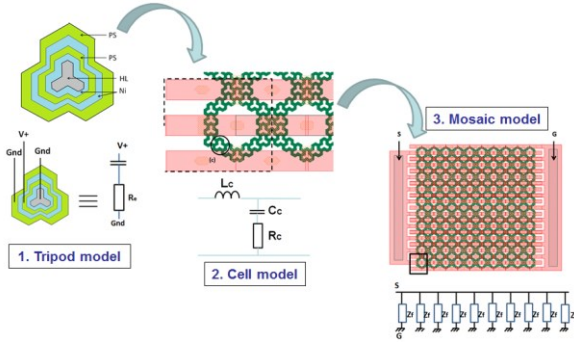


Fig. 4. Modeling methodology

### B. Mosaic capacitor modeling

- Tripod model:

As shown in figure Fig.5 and for calculation simplicity point of view, the tripod shape could be assimilated to a cylindrical shape. Indeed, the internal perimeter difference is about 1% and the external perimeter difference is around 3%. For low density cells (~20 tripods by cell), the elementary tripod capacitance is around 5pF while the elementary capacitance is around 3.5pF for high density cells (~400 tripods by cell). The tripod equivalent resistance is estimated to be 79.8Ω.

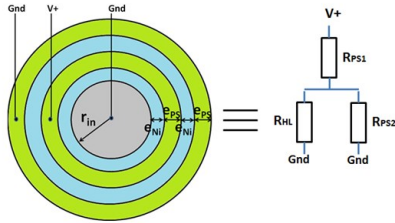


Fig. 5. Model of tripod resistance

- Cell electrical model:

As shown in figure Fig.6, RLC equivalent circuit is used for the cell modeling. C and R parameters are related to the tripod configuration and number. For 22.5 tripods, the cell presents a capacitance of 113pF and an equivalent resistance of 16Ω. Regarding the equivalent inductance, a coplanar line electrical model is used [3] and the inductive contribution is about 5pH.

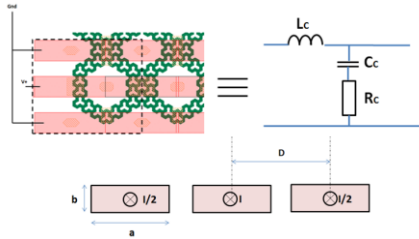


Fig. 6. Cell electrical model

- Finger electrical model: cells cascading.

At macro level, the mosaic capacitor is obtained by cascading and connecting cells together. As illustrated in figure Fig.7, the capacitor is composed of repetition of finger lines. The global capacitance value is given by the capacitance of one cell multiplied by the number of cells.

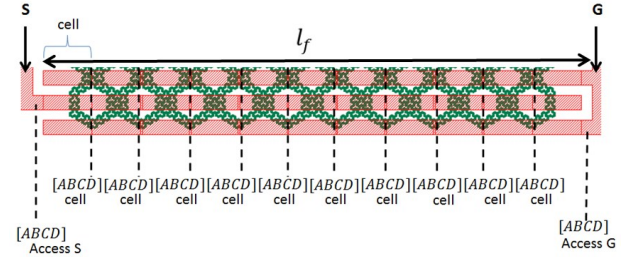


Fig. 7. Finger electrical model

To calculate the impedance of the capacitor, the electrical parameters of the finger line are calculated in first (equation (1)).

$$\gamma_{cf} = \frac{\text{acosh}(A_f)}{l_f} \quad Z_{cf} = \frac{B_f}{\sinh(\gamma_{cf} \cdot l_f)} \quad (1)$$

Then, the impedance of the open-circuited line is calculated (equation (2)).

$$Z_f = Z_{cf} \cdot \coth(\gamma_{cf} \cdot l_f) \quad (2)$$

Finally, the global impedance value is defined as the impedance of the open-circuited line divided by the number of fingers (equation (3)):

$$Z = \frac{Z_f}{N} \quad (3)$$

## IV. ELECTRICAL CHARACTERISTIC IN THE RF DOMAIN

A test reticle has been designed embedding a wide coverage in term of C and ESR. This reticle is embedding test structures that are suitable for HF/RF characterization. Those designs are derived from the design concept presented in section II. Several different architectures of capacitive elements (MOSAIC), where the global capacitance is constructed out of a massive network of parallelized elementary cells, were manufactured. The parallelization is obtained by leveraging the sub-micronic lithographic capability of the PICS process. Out of the set of characterized capacitance, two elementary cells A and B are presenting significantly lower ESR values compared to prior art. Type A Mosaic capacitors are fully optimized in terms of ESR while cell B present a compromise ESR with minimum derating on density (200nF/mm<sup>2</sup>). Both configurations are available with two different interconnection strategies (strap/unstrapped, see figure Fig.8) which provides ways to further lower ESR at the cost of slightly higher ESL (optimization of current loops). Those capacitors have remarkably low parasitic inductance in comparison with equivalent MLCC, and thus are excellent candidates for high speed power decoupling.



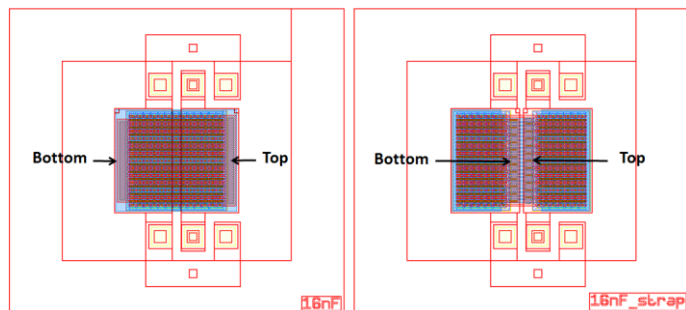


Fig. 8. Layout of 16nF Mosaic capacitor with two interconnection strategies (unstrapped on the left / strapped on the right)

Figure Fig.9, presents a summary of the electrical characteristics obtained in the RF domain (300 KHz-1Ghz) of both A and B PICS MOSAIC capacitors. The Blue dots corresponds to the prior art, while the other dots are corresponding to capacitor architecture based upon Mosaic approach.

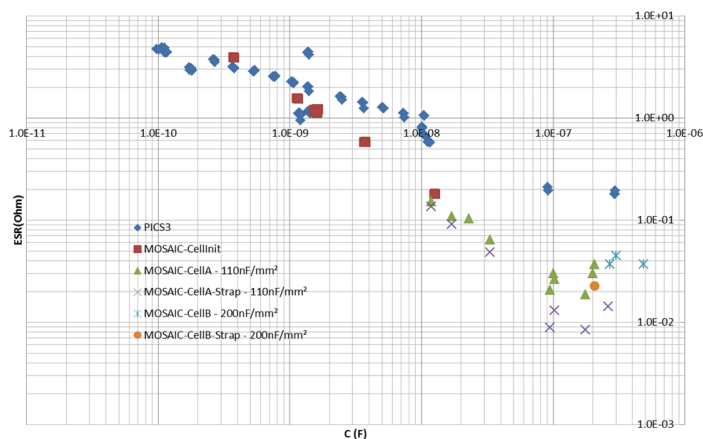


Fig. 9. Electrical characteristics in the RF domain (300 Khz-1Ghz)

As indicated in the table TABLEI, good matching is obtained between model and measurement for different capacitor values. One can also notice that capacitors self resonance frequencies are very high.

TABLE I. COMPARISON BETWEEN MODEL AND MEASUREMENTS

	C (nF)		R (mΩ)		L (pH)		f <sub>0</sub> (MHz)	
	model	measure	model	measure	model	measure	model	measure
<b>11 nF</b>	11.4	11.6	164	156	5.4	5.3	640	643
<b>16 nF</b>	16.3	16.7	113	117	6.1	5.5	505	525
<b>33 nF</b>	33.1	33.5	56	71	5.9	6.7	360	335
<b>222 nF</b>	223.2	224	8	28	4.2	4.1	165	167
<b>470 nF</b>	473	468	4	24	2.9	2.2	136	157
<b>404 nF</b>	390	392	4	40	4.91	1.53	115	205
<b>406 nF</b>	390	391	3	35	5.3	3.31	110	140

## V. CONCLUSION

New ultra low ESR MOSAIC capacitors were presented in this paper. Based on this new design, the PICST<sup>TM</sup> capacitor exhibits the following outstanding characteristics:

- Linear dependency of capacitance with  $C_{\text{Global}} = N \cdot C_{\text{Local}}$  where N is the number of repetitions of the localized element
- Inverse linear dependency for the ESR and ESL with  $L_{\text{Global}} = L_{\text{Local}}/N$  and  $\text{ESR}_{\text{Global}} = \text{ESR}_{\text{Local}}/N$ .
- Constant  $\text{ESR} \cdot C$  and  $\text{ESL} \cdot C$  resulting in constant cutoff and self-resonance frequencies

As shown in figure Fig.10, this way of design, combined with the IPDiA silicon interposer using thick (12 $\mu$ m) copper top metallization routing, are leveraging large ESR and ESL reduction and are therefore suitable to be used in the field of high frequency DC-DC conversion.

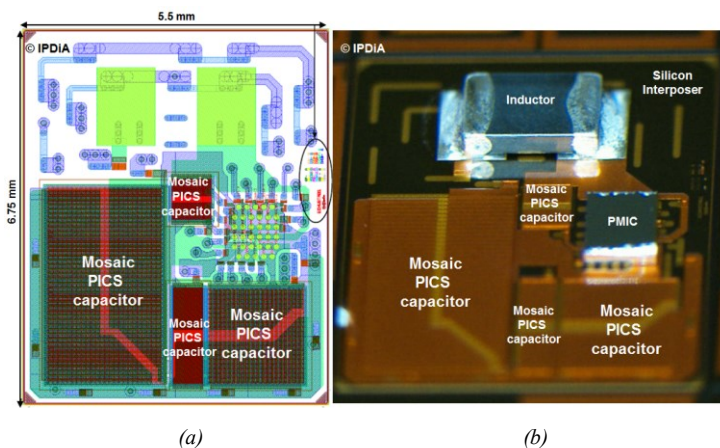


Fig. 10. (a) Layout view of IPDiA PICS silicon interposer; (b) Final prototype with mounted inductor and flip-chipped PMIC (PowerSWIPE project)

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## REFERENCES

- [1] Ludovic Fourneaud, Mohamed Mehdi jatlaoui, Frederic Voiron, "Silicon integrated capacitance for power conversion applications", International Power Supply On Chip Workshop; October 6, 7, & 8, 2014; Northeastern University; Boston Massachusetts; USA
- [2] F. Roozeboom, J. Klootwijk, L. Guiraud, F. Le Cornec and D. Chevie, "Integrated Ultrahigh-Density Capacitor based on multiple dielectric/conductor layer stacks deposited on pillar arrays in silicon". Patent 686403, 17 01 2006.
- [3] Edward B. Rosa, "Inductance of Linear Conductors"; Bulletin of the bureau of standards. Vol4. No2

- [3] Edward B. Rosa, "Inductance of Linear Conductors"; Bulletin of the bureau of standards. Vol4. No2