

Performiniaturization of 4-channel driver with bypass grounding silicon capacitor flip chipped (FCOM architecture)

CSICS 2015, Oct 11th - 17th, New Orleans, LA, US

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Abstract — This paper presents the co-integration of a 4 channel driver IC optimized to be DC decoupled in chips. The bypass grounding silicon capacitor is flip-chipped on the CMOS Driver (CD) and is connected by copper pillar bumps with a form factor of 10/13. The stacked face to face assembled product is a complete assembly ready for mounting and wire-bonding by using the perimeter pads of the CD. This bypassing optimizes the DC noise immunity from the CD to the output and is possible thanks to our Ultra Broadband Silicon Capacitors (UBSC) low ESL and low ESR (up to 60+ GHz). These capacitors combine ultra-deep trench MOS capacitors of a few nF and single layer MOS capacitors of few 10's pF in a single package. The performances of these capacitors have been analyzed. Their benefits are quantified thanks to the S-parameters measurements in shunt mode, as well as the flip-chip on module (FCOM) architecture optimized for the broadband application.

Index Terms — ultra broadband silicon capacitors, flip chip devices, 4 channel driver, low Equivalent Series Inductance.

I. INTRODUCTION

The UBSC^(*) capacitors are designed for DC bypass grounding application in all broadband optical communication systems (ROSA/TOSA, SONET and all optoelectronics) as well as high speed data systems or products. This technology provides industry-leading performance particularly in terms of capacitor stability over the full operating DC voltage & temperature range, fully compatible with the CMOS driver requirements. In addition, intrinsic properties of the silicon lead to a low dielectric absorption and a close to zero piezoelectric effect resulting in no memory effect. This Silicon based technology is RoHS and REACH compliant.

(*) : Ultra Broadband Silicon Capacitor

II. UBSC CAPACITORS BUILDING

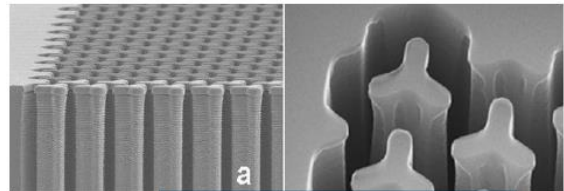
The SiCap technology of IPDiA with advanced 3D topology is equivalent to a total area of 80 ceramic layers. The use of a very efficient silicon based dielectric avoids the compromise between capacitance value and electrical performance.

The deep trench MOS capacitor technology of IPDiA combined with MOS capacitor and distributed trench capacitor drives to an unprecedented level of RF/microwave electrical performances compared to any other existing capacitor technology. Thanks to the full modelization of the elementary cell, the values of the ESL and ESR are optimized to reach the performances required on the ultra-broadband market. These high density 3D capacitors make up the beating heart of the IPDiA PICSTM technologies: the combination of

patented [1] high aspect-ratio micrometric 3D structures (50:1 pores or trenches, drilled in the silicon by Deep Silicon Reactive Ion Etching, see Figure I) with standard dielectrics (silicon oxide and/or nitride) from the semiconductor industry in single (or multiple) Metal Insulator Metal (MIM) architectures (Figure II) enables the process of capacitors with densities as high as 250nF/mm².

3D trench capacitors, as shown in figure I, provide outstanding density integration performances as well as remarkable electrical characteristics (low ESR, ESL) compared to external components (described in [2], [3], [4], [5]). These good characteristics are achieved thanks to the individual components proximity and layout flexibility inside the circuit.

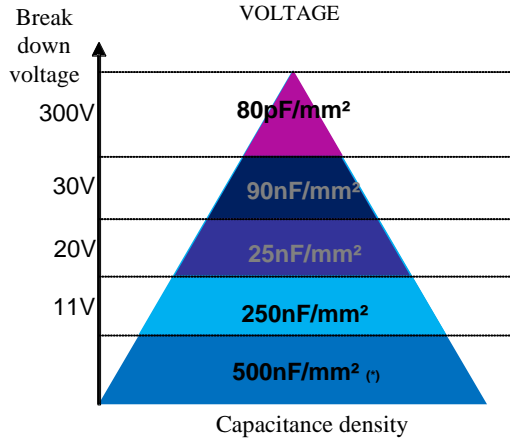
FIGURE I
CROSS-SECTIONAL SEM IMAGES OF 3D MOS EMBEDDED
TRENCH CAPACITOR MANUFACTURED BY IPDiA



These Si capacitors in ultra-deep trenches enable the integration of high capacitance density from 90nF/mm² to 250nF/mm², with a break-down voltage of respectively 30V to 11V (figure II). A dielectric stack of silicon nitride and silicon dioxide associated to an N-type very low-ohmic silicon substrate are used to produce these small devices.

Figure II presents the capacitance densities currently available at IPDiA. The increase in minimum break-down voltage from one generation to the next one is the combination of advances in dielectric material deposition, etching techniques, and device geometry to keep the highest capacitance density versus voltage.

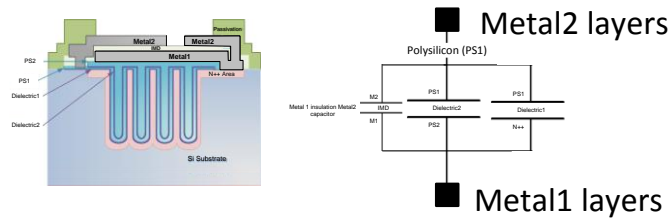
FIGURE II
UBSC CAPACITANCE DENSITY VERSUS MIN BREAK-DOWN VOLTAGE



(^{*)}: process only for pre-sampling

FIGURE III

ON THE LEFT: CROSS SECTIONAL VIEW OF THE MIMIM ARCHITECTURE USED IN THE IPDIA PICS™ TECHNOLOGY. ON THE RIGHT: SCHEMATIC (VOLUNTARILY SIMPLIFIED) OF THE CAPACITORS PARALLELIZED IN A MIMIM ARCHITECTURE TO OFFER A HIGHER CAPACITANCE VALUE THAN IN SINGLE MIM IPDIA PICS™ TECHNOLOGIES



As in figure III, $C_{TOTAL} = C_{MIM} + C_{PS1-PS2} + C_{PS1-N++}$

III. NEW PICS™ DESIGN CONCEPT FOR LOW ESR APPLICATIONS

The standard way to design PICS™ capacitors consists in defining a block of high aspect-ratio 3D micrometric structures (i.e. tripods for the PICS™ process as shown in figure I). This enables to reach the specified value and then in sizing the required areas for contacting the three electrodes from the MIMIM architecture. These contact dimensions are defined according to the material sheet resistance of each electrode with the objective to maximize capacitance density while maintaining contact areas large enough to obtain reasonable ESR.

With this style of design, the current is mostly flowing in the electrodes along large distances to reach individual PICS™ pores. As a consequence the ESR is driven by the capacitor shape/outer extend and the ESR is hardly tunable by design.

The “mosaic” style of design overcomes this issue with a global capacitor element designed as a grid of localized capacitors elements that are all parallelized.

With this approach, the design of the localized element can be tuned to match any requirements in term of ESR or Capacitance (C). Indeed:

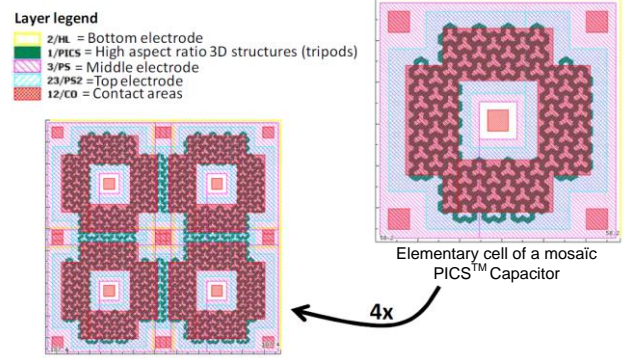
- The global capacitor targeted value C, is correlated to the number N of localized elements to be parallelized on the grid such that the capacitance value of the localized element is $C*N$,
- The global ESR target is a function of $1/N$ that is forcing the ESR of the localized element,
- The ESR of the localized element is correlated to the local density of metallization contact to capacitor electrodes.

This approach has several obvious advantages including a perfect scalability and a lower sensitivity to electrode quality (i.e. resistivity) as long as contacts are provided locally. This results in a lower ESR and in a constant contact density overall the structure.

The Figure IV represents a “mosaic” PICS™ capacitors built up with four repetitions of a localized capacitor cell (containing the high aspect ratio 3D structures and the oversized contacts areas all around).

The Figure V gives a projection of the ESR to Capacitance dependency, extracted out of real elements (interpolated) and idealized projection (extrapolated). The perfectly linear slope in a Log.Log representation of the ESR as a function of Capacitance corresponds to the behavior of an idealized grid where perfect discrete RC (localized element) are connected in parallel on the grid.

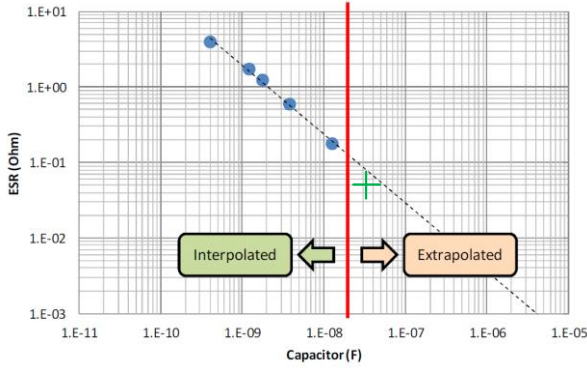
FIGURE IV: “MOSAIC” PICS™ CAPACITOR DESIGN



In the Figure IV, the $58.2\mu m * 58.2\mu m$ cell size is the optimized elementary cell (470pF) of a mosaic-style PICS™ capacitor with $250nF/mm^2$ capacitance density node. Elementary cells are parallelized as necessary to reach the required capacitance value.

To insure the validity of the above approach and the ESR prediction, several mosaic PICS™ capacitors were designed, assembled from a 470pF elementary capacitor building block which was repeated 4x, 9x or 30x.

FIGURE V: ESR EXPERIMENTALLY REACHED WITH PICS™ MOSAIC DESIGNS



The Figure V shows the typical ESR performances obtained with PICS™ capacitors when designed in the “mosaic” way. Note that the green cross is the new value measurement with the product detailed in this paper.

Using this unique technology, we are able to optimize ESL and ESR to reach the lowest possible value. Our 22nF Low ESR UBSC capacitor is made of 47 elementary cells of 470 pF distributed over the chip (ultra-deep trench MOS capacitors) and are combined with a 10 pF single layer MOS capacitors in parallel to lower the impedance at higher frequency. This UBSC is composed of dual capacitor and embedded in single package size (Figure VI & VII).

FIGURE VI

DUAL 22nF//10pF-0303 UBSC CAPACITOR BLOCK DIAGRAM AND 3D VIEW OF DUAL UBSC CAPACITOR PIN CONFIGURATION

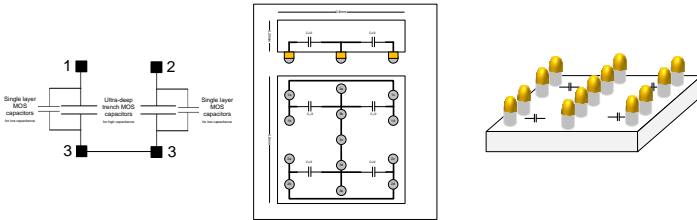
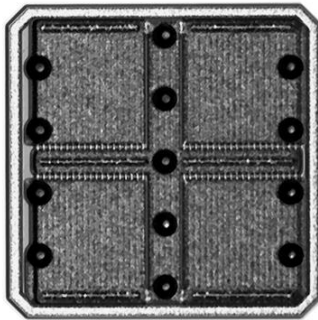


FIGURE VII: MICRO-PICTURE OF DUAL UBSC capacitor



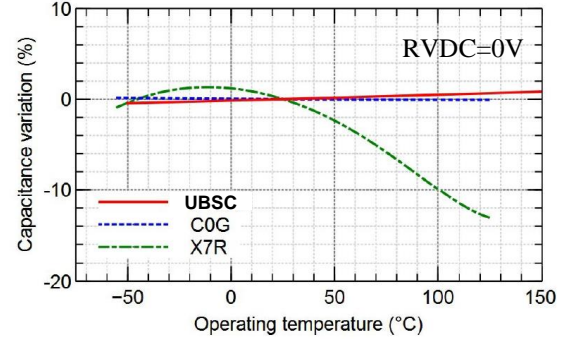
IV. DUAL UBSC CAPACITORS STABILITY OVERVIEW AND RF CHARACTERIZATION

These devices exhibit an ultra-broadband rejection obtained by a low ESR (50mΩ) and a low ESL (10pH). These performances can be kept over temperature and voltage variation (respectively Graph I: $\pm 0.5\%$ from -55°C to $+150^\circ\text{C}$ and Graph II: $0.1\%/V_{DC}$) thanks to a very low capacitance change as well as a very high reliability and low leakage current. The dielectric stack deposited using a high temperature process (900°C) is leading to an excellent uniformity and stability of the capacitance value, and also to a memory effect close to zero. Moreover, the silicon substrate brings low dielectric absorption leading to almost no piezo effect as shown in table I.

Temperature and voltage measurements show that UBSC capacitors behave as robust devices in various configurations. For instance, the $\Delta C/C$ variation is lower than $80 \text{ ppm}/^\circ\text{C}$ in the $-50^\circ\text{C}/+150^\circ\text{C}$ temperature range. As shown in Graph I for the case of a dual 22nF//10pF UBSC capacitor, $\Delta C/C$ variations are linear over temperature.

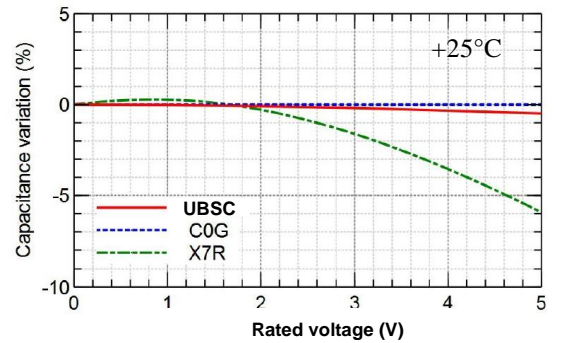
GRAPH I

DUAL 22nF//10pF - 0303 UBSC CAPACITANCE VALUE VERSUS TEMPERATURE: 0.5%



GRAPH II

DUAL 22nF//10pF - 0303 UBSC CAPACITANCE VALUE VERSUS RATED VOLTAGE: 0.1%/V



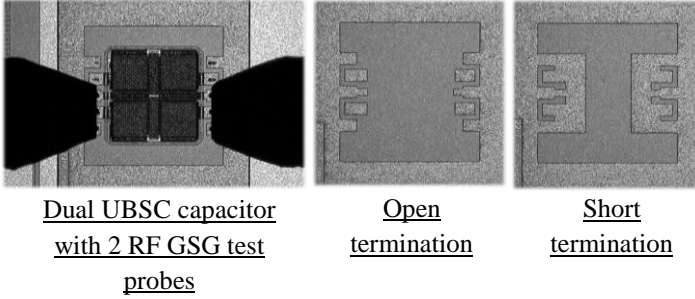
Concerning the variation over the voltage range, the $\Delta C/C$ of a 22nF//10pF UBSC capacitor is lower than 0.2% for a -5 V to $+5 \text{ V}$ voltage variation.

TABLE I
DIELECTRIC ABSORPTION COMPARISON

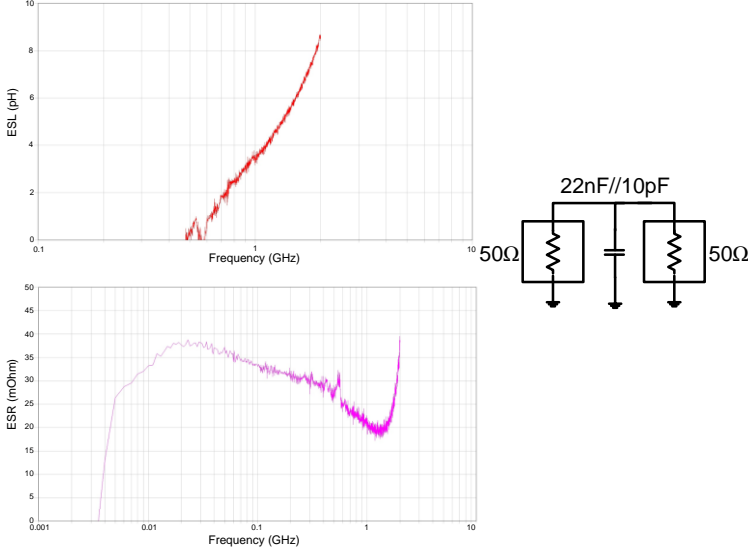
Type of capacitor	Dielectric absorption
Class-1 ceramic capacitors, NP0	0.6%
Class-2 ceramic capacitors, X7R	2.5%
Silicon capacitors	0.05%

Thanks to our Silicon substrate, our dual UBSC capacitors have at least 12 times lower dielectric absorption than ceramic capacitors.

FIGURE VIII:
DUAL UBSC CAPACITOR TEST BENCH
IN SHUNT MODE



GRAPH III
DUAL 22nF//10pF - 0303 UBSC ESL & ESR CHARACTERISTIC
VERSUS FREQUENCY IN REFLECTION MODE



The two plots from Graph III show the extracted Equivalent Series Inductance values (ESL) and the extracted Equivalent Series Resistance values (ESR) resulting from measurement in shunt mode. This measurement mode allows to mathematically remove the extrinsic parasitic elements without de-embedding them as shown in Figure VIII. Note that the characteristic impedance of the transmission line used is at 50 Ohm nominal.

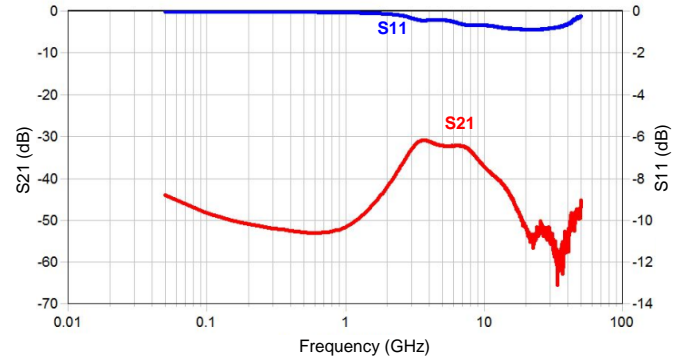
TABLE II
DUAL 22nF//10pF - 0303 UBSC CAPACITOR PERFORMANCES

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C1 & C2	Capacitance value	@25°C	-	22	-	nF
L	Capacitor length	±0.01	-	0.8	-	mm
W	Capacitor Width	±0.01	-	0.8	-	mm
h	Capacitor height	±0.01	-	0.2	-	mm
ΔC_p	Capacitance tolerance	@25°C	-15	-	+15	%
ΔC_M	Capacitance matching	Between C1 & C2	-1	-	+1	%
RV_{DC}	Rated voltage		-	3.6	-	V _{DC}
BV	Breakdown voltage		11	-	-	V
T _{OP}	Operating temperature		-55	20	150	°C
T _{STG}	Storage temperature		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C	-0.5	-	0.5	%
ΔC_{RVDC}	Capacitance voltage variation	From 0V to RV_{DC}	-	-	0.1	%/V _{DC}
Rej	Rejection	Up to 50GHz	-30	-	-	dB
ESR	Equivalent Serial Resistance	@25°C	-	50	-	mΩ
ESL	Equivalent Serial Inductance	@25°C & SRF	-	10	-	pH

V. DUAL UBSC CAPACITORS BROADBAND BEHAVIOR

The dual UBSC capacitor testing up to 50GHz were performed directly on wafer, thanks to GSG structures and RF test probes (Figure VIII). The measurements summarized in Table II and in Graph IV have been done in reflection mode. Note that the characteristic impedance used is at 50 Ohm nominal.

GRAPH IV
DUAL 22nF//10pF - 0303 UBSC S-PARAMETERS VERSUS
FREQUENCY IN REFLECTION MODE



VI. COPPER PILLAR BUMPS FOR LEAD FREE FLIP CHIP ON MODULE (FCOM) PACKAGING

Copper pillar interconnects are a popular interposing option due to the advantages of fine pitch, lead free, small pillar size and good thermal and electrical performance, making copper pillar interconnects very useful for high-frequency and high-density flip-chip-on-module (FCOM) packages. However, the challenges associated with the technology include controlling the formation of brittle intermetallic compounds (IMC) and weak interfaces during heat-related processes, and also preventing copper migration during bonding and reliability testing. As the reliability of the joint is significantly affected by the property of the surface finishing, it is important to understand the influence of different surface finishings on the reliability of copper pillar interconnections.

Nevertheless, the flip-chip process using copper pillar bump is one of the solutions:

- Cu pillar bump possesses a lower joint resistance than solder interconnect
- Cu pillar bumps exhibit a Mean Time To Failure (MTTF) 2.3 times better than standard bumps.

The Cu pillar is a cylindrical bump with a SnAg solder cap (instead of the usual solder bump SAC305) used to connect together two silicon chips. Figure IX and Table III show the characteristics of the Cu pillar bump with SnAg2.5% lead free solder. The total bump height is equal to 65µm including 40µm of copper and 25µm of cap (max cap height is equal to half of Cu pillar diameter). The pad top passivation opening diameter is defined by Polyimide (PI) and must be the same for both silicon chips.

Copper pillar is processed using standard techniques. A thin TiCu layer is deposited by sputtering to act as barrier and seed layer for further electroplating steps. Then, the lithography step using a thick photoresist is realized to define the bumps areas. Cu pillars and then SnAg caps are deposited by electroplating technique. Afterwards, photoresist is removed and the thin TiCu layer is wet etched to isolate the Cu pillars. Last step is the final reflow of the Cu pillar (Figure IX & X).

TABLE III
DUAL UBSC BUMPING DEFINITION

Item	Unit	Size
Pad top passivation opening size (diameter)	µm	40
Pad metal size (diameter)	µm	60
Copper Pillar diameter	µm	50
Copper Pillar height (Cu+SnAg cap) after reflow	µm	65±9
Max. copper pillars coplanarity	%	10
Minimum pad pitch – x direction	µm	300
Minimum pad pitch – y direction	µm	150
Scribe lane width	µm	100.0

FIGURE IX
DUAL UBSC CROSS SECTION OF COPPER PILLAR DEFINITION
AFTER REFLOW

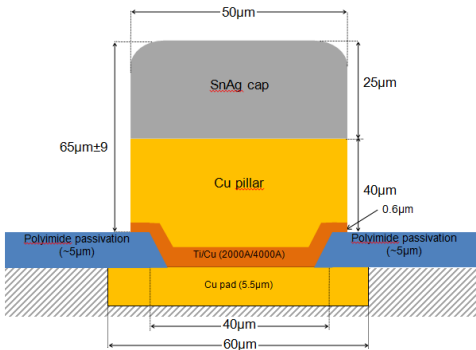
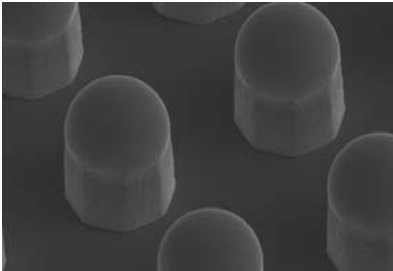


FIGURE X
DUAL UBSC MICRO PICTURE OF COPPER PILLAR
AFTER REFLOW



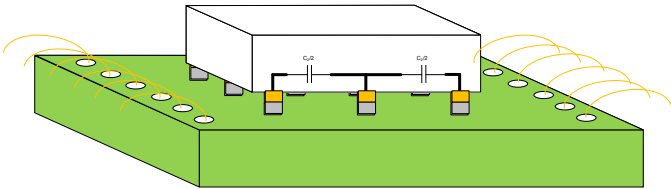
VII. FLIP CHIP ON MODULE (FCOM) ARCHITECTURE

This chapter explains how to flip-chip the dual UBSC capacitor on top of the CMOS driver using the copper pillar bumps (See Figure XI). Solder bumps have been deposited on the CMOS dies to allow the flip-chip process. These solder bumps consist in a Ni plated bump covered by a SnAg cap.

Flip-chip process can then be realized by flipping the UBSC capacitor with the matching pads of the CMOS die. Reflow soldering is done to finalize the electrical connections. Underfill is dispensed to avoid empty spaces between the dies and to provide a stronger mechanical connection. It also creates a heat bridge and ensures that the solder joints are not stressed due to differential heating in the FCOM architecture. The underfill distributes the thermal expansion mismatch between the chip and the board, preventing stress concentration in the solder joints which would lead to premature failure.

The wafer is finally sawn to separate the individual devices. To finalize the interconnections, the FCOM is wire-bonded from CMOS pads to the Printed Circuits Board (PCB).

FIGURE XI
VIEW OF DUAL UBSC FLIP-CHIPPED ON THE TOP OF CMOS DIE



The main advantage of flip chip assembly is to get much less parasitics than a traditional carrier-based system due to shorter interconnections; also, the chip sits directly on the circuit board. The short wires greatly reduce inductance, allowing higher-speed signals, and also conduct heat better.

VIII. CONCLUSION

Single UWSC capacitors and array from IPDiA show outstanding broadband frequency behavior, lifetime, miniaturization and performance stability and are therefore ideal for demanding applications such as data broadcasting systems.

A new way of designing PICS™ capacitor, called “mosaic”, implementing localized elements set in a parallel grid has been demonstrated. When built with this approach, the PICS™ capacitor exhibits the following remarkable characteristics:

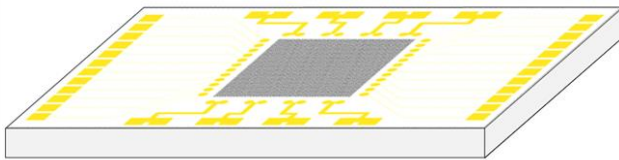
- Linear dependency of capacitance with $C_{TOTAL} = N \cdot C_{Elementary}$ where N is the number of repetitions of the localized element,
- Inverse linear dependency for the ESR and ESL with $L_{Total} = L_{Elementary} / N$ and $ESR_{Total} = ESR_{Elementary} / N$.
- Constant $ESR \cdot C$ and $ESL \cdot C$ resulting in constant cut-off and self-resonance frequencies
- These frequencies are driven by the design of the localized block.
- With this approach, the resistivity of the electrodes becomes secondary with respect to the total capacitor performance as long as C and ESR/ESL can be tuned almost independently by design.

Development are now focused on extending “mosaic” concept to larger elements and to demonstrate co-integration into advanced silicon interposer intended to be used as carrier to embed capacitors and redistribution layers.

In combination with the PICS, its packaging technology is enabling further miniaturization and performances. Depending on customer applications, product and technology platforms proposed may be used at different integration scales, where the optional enablers are either only the distribution layers, passive components and/or protection diodes capability onto silicon. 2D interconnection with external die flipped over for example as shown in the Figure XII is an easy access to the PCB world in terms of design rules, usage and development costs.

FIGURE XII

2D INTERCONNECTION WITH 3D SI CAPACITORS EMBEDDED



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