Physical Implementation of 3D Integrated Solenoids within Silicon Substrate for Hybrid IC Applications

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***Abstract*— This paper presents an original concept of a 3D solenoid realized in a 300µm depth High Resistivity Silicon (HRS) using the Through Silicon Via (TSV) interconnection technology. Electrical performances deduced from two-ports S-parameters are reported. A comparison is performed considering first conventional O-shaped planar BiCMOS (Al Back-end) inductor, then a CMOS (45 nm node, Cu Back-end) O-shaped inductor respect to area occupation together with electrical performances. A predictive electrical model is proposed and compared to measurement results. Correlations between simulation and measurements are found satisfactory.**

I. INTRODUCTION

Implementing the right inductors remains a challenge that every back-end designer needs to face within common RF blocks (LNA, VCO). RF applications require competitive inductors with constraints such as high Q-factor, small area consuming, limited parasitic coupling, ease of layout and manufacturing. Indeed high Q-factor means lower current needed for the same level of performances as well as wider tuning range of the VCO and therefore wide frequency band coverage.

At present, there are still some challenging difficulties in the development of planar inductors with high performances. Trades off still exist between a large inductance and a large Q-factor. Serious losses occur at high frequencies and it further degrades the Q-factor due to an increase in the total tracks length and due to an increase in parasitic capacitive coupling between tracks in case of high inductance values required. Several recent approaches have been proposed to decrease the overall footprint of the inductors together combined with their drawbacks clearly limiting their implementation [1]. Moreover, inductors using low resistivity substrates are victim of losses dominated by the magnetic coupling to the substrate named "substrate skin effect". But the increase of the Q-factor is possible in particular with a decrease of the substrate losses. A solution can be to etch the silicon underneath the inductor [2] or consider a substrate transfer technology [3].

The recent emergence of 3D interconnects such as TSV (Through Silicon Vias) and via holes has offered the possibility to consider new inductors architectures. Both low-temperature co-fired ceramic (LTCC) and organic laminate technologies enable integration of passives such as inductors in a multilevel ground plane concept [4]. The footprint of the inductor in surface can be repeated on each LTCC layer and then connected by the vias.

We have made the choice to develop an original type of 3D solenoid using an emergent interconnect technology, the TSV, fabricated in the NXP Semiconductors Caen factory. Our 3D solenoid uses the thickness of the silicon as the third dimension. Indeed each turn of our solenoid is fabricated with the TSV as the vertical sides. A front side and backside metallization of the bulk wafer leads to connect the top and bottom tracks thanks to the TSV, allowing to create loops embedded within the silicon. Thereby we obtain a square section 3D solenoid architecture.

In that sense the first section of this paper describes the original solenoid architecture developed for the 3rd generation of customized NXP Semiconductors low cost high resistivity silicon process suitable for Multi-Chip Module (MCM) applications. The second section presents analysis results based on RF characterization for various geometric variants. An equivalent circuit model is then described in the third part to predict the electrical response of the solenoid. A comparison between both measured and simulated data is proposed to support the modelling investigations.

II. 3D COIL DESCRIPTION

As mentioned in introduction, an elementary spire of our 3D solenoid consists of metal tracks connected between them with two TSV. Copper is deposited onto front and back sides of a 300µm depth high resistivity silicon according to a pattern defined in Fig. 1. The vias are partially filled with the same metal (external sides only). Consequently a N-turns 3D solenoid consists of N elementary spires placed side by side and connected in the respect of the pitch between two consecutive vias as show in Fig. 2. Due to the TSV technology process, parameters such as vias diameter and vias height are fixed and so can not be modified. To avoid mechanical stress, the pitch between two vias is set to a minimum value equal to 125µm. Nevertheless the dimensions of the metal tracks in front and back sides can be modified. Hence the solenoid is defined of course according to his number of turns (N), his width (D_y) and the metal track width (W). A change in the metal track width will also impact the spacing (SP) between two consecutive metal tracks.

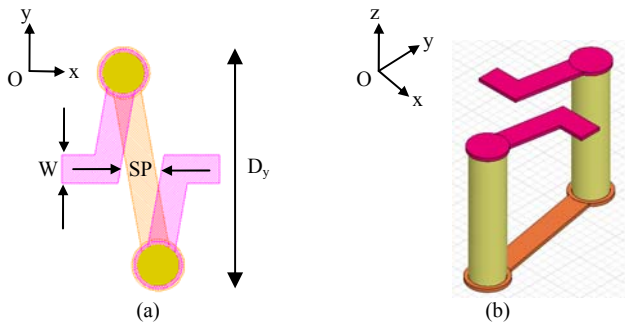


Fig. 1 Layout top view (a) and 3D view (b) of a 1-turn 3D solenoid

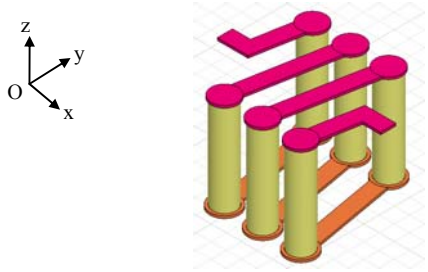


Fig. 2 A 3D view of a 3-turns 3D solenoid

To support our theoretical investigations, five solenoids with 1 to 5 turns were designed. The dimensions are given in table I. The estimated inductance value L of the solenoid has been decomposed in a sum of elementary inductance values L_i (either a metal track L value or a via L value). Each of the elementary inductance values L_i has been evaluated respect to the partial inductance concept [5].

TABLE I

GEOMETRIC VARIANTS FOR THE FIVE DESIGNED 3D SOLENOIDS AND THE ASSOCIATED ESTIMATED SELF-INDUCTANCE VALUE (dimensions are given in micrometers except for the area in square millimeters)

Device	N	Area	D_y	W	# Vias	Estimated L (nH)
1	1	0,126	445	50	2	0,9
2	2	0,182	445	50	4	1,8
3	3	0,238	445	50	6	2,9
4	4	0,293	445	50	8	4,0
5	5	0,349	445	50	10	5,1

III. MEASUREMENTS RESULTS

A set of 3D solenoids have been characterized in a high resistivity silicon substrate. The designed test case inductors were measured using a network analyser PNA8364B from Agilent Technologies, with high frequency micro-probes. Full two port S-parameter measurements were performed for each device in the wide frequency range 100MHz to 50GHz. During the RF characterization, the wafer is stacked to a grounded chuck to ensure a global reference ground to the wafer, the network analyser and the micro-probes. If no precautions are taken, a short circuit appears between the grounded chuck and the bottom metal tracks of the wafer. As a consequence, a sheet of an insulating material (~100µm thick, $\varepsilon_r = 2.0$) has been placed between them. Self-inductance and resistance values as well as Q-factor have been extracted from measurements according to the following expressions:

$$R = \text{real}\left(1/Y_{11}\right) \quad (1)$$

$$L = \frac{\text{imag}\left(1/Y_{11}\right)}{2\pi \text{freq}} \quad (2) \qquad Q = -\frac{\text{imag}(Y_{11})}{\text{real}\left(Y_{11}\right)} \quad (3)$$

where freq represents the working frequency. The values R, L and Q have been plotted against frequency in the following figures.

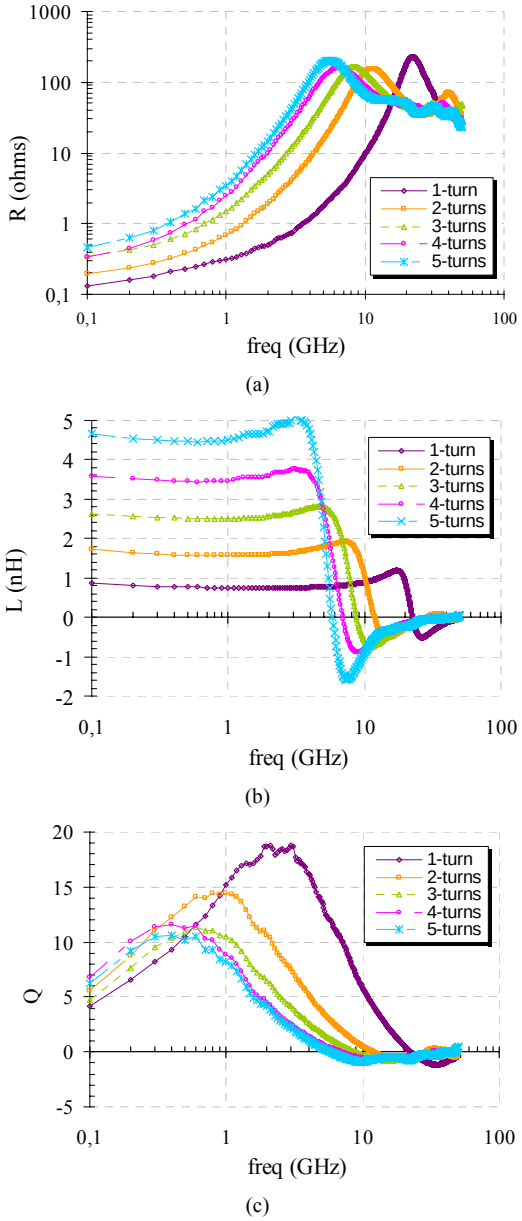


Fig. 3 Experimental variations of R (a), L (b) and Q (c) of 3D solenoids with 1 to 5 turns against frequency

For each of the five devices, the resistance increases rapidly due to skin effect. Skin effect is usually described as the

tendency of current to flow primarily on the surface (skin) of a conductor as frequency increases. Because the inner regions of the conductor are thus less effective at carrying current than at low frequencies, the useful cross-sectional area of a conductor is reduced, thereby producing a corresponding increase of resistance. Some other parasitic effects can appear and introduce additional resistive losses. Indeed proximity effects can exist between two nearby metal tracks or vias. Contrary to the skin effect, the current distribution will be constrained only to the metallic surfaces facing each other. Table II sums up extracted measured values of resistance, self-inductance, peak Q-factor and self-resonant frequency (SRF) for 3D solenoids with 1 to 5 turns. If we have a look at this table, we see that L is almost proportional to the number of turns. This reveals a weak coupling between turns due to a large pitch between two consecutive vias (125µm) and in the same manner a large spacing between metal tracks (80µm). Nevertheless, our solenoid proposes an honourable Q-factor at low frequencies. We obtain a Q-factor above 10 since 200MHz, the best reaching 18,8 at 3GHz (1-turn).

We have compared our 1-turn 3D solenoid with a 1-turn O-shaped inductor made in two customized NXP processes (0,25µm BiCMOS and 45nm CMOS) having both 0,88nH. For similar footprint and self-inductance, the solenoid performances in terms of Q-factor are better up to 3GHz.

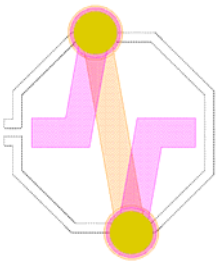


Fig. 4 Layout top-view of a 1-turn O-shaped inductor (dashed line) and a 1-turn 3D solenoid with a self-inductance value of 0,88nH

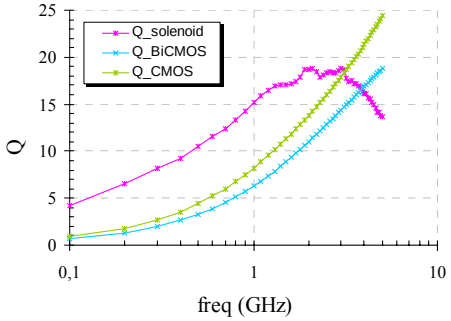


Fig. 5 Q values for a 3D solenoid and an O-shape inductance in two different processes: BiCMOS and CMOS

In the solenoid description section, we have estimated analytically the inductance value for solenoids with 1 to 5 turns with the help of the partial inductance concept. A comparison with extracted self-inductance values from measurements is shown in Fig. 6. The estimation is in good agreements with extracted measured values.

TABLE II

SUMMARY OF MEASURED RESISTANCE, SELF-INDUCTANCE, PEAK Q-FACTOR AND SERIAL RESONANCE FREQUENCY (SRF) VALUES FOR FIVE SOLENOIDS
(resistance and self-inductance extracted respectively at 100MHz and 1GHz)

Device	N	R (mΩ)	L (nH)	Peak-Q	SRF (GHz)
1	1	131	0,882	18,8 @ 3,0GHz	22,4
2	2	193	1,716	14,4 @ 1,0GHz	11,9
3	3	351	2,636	11,3 @ 0,6GHz	8,7
4	4	333	3,596	11,6 @ 0,4GHz	6,9
5	5	465	4,662	10,5 @ 0,4GHz	5,8

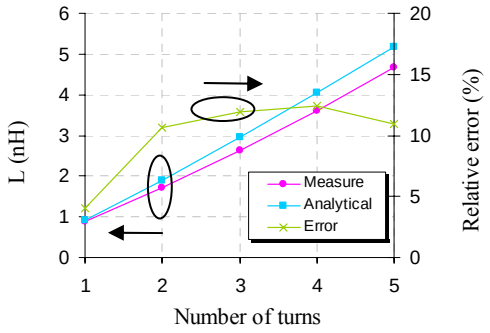


Fig. 6 Inductance values comparison between measurements and analytical calculation using the partial inductance concept for solenoids with 1 to 5 turns

IV. SOLENOID MODEL

Traditionally classical planar inductors are modelled with the help of the 9-elements scheme [6]. This technique is not suited in the case of 3D solenoids because of the backside metallization and parasitic 3D effects due to the vias.

Our choice has been to follow the physical configuration of a 1-turn solenoid to deduce an RLC equivalent circuit model in the frequency range 100MHz – 50GHz as shown in Fig. 7.

Knowing that each of both vias is modelled by two equivalent half-vias, the self-inductances of the top and bottom metal tracks as well as the vias are characterized respectively by L_{line_top}, L_{line_bot} and L_{half_via}. The metal tracks and the vias are sensitive to the skin effect. The skin depth in the copper, with a conductivity of 5,8 S/m, at 100MHz and 1GHz equals 6µm and 2µm respectively. Hence an RL ladder scheme [7] has been used to predict the increasing resistance against frequency for each of the metal tracks (R_{line_top} and R_{line_bot}) and the vias (R_{half_via}). Regarding the coupling between two adjacent vias, we can distinguish several contributions. The first one is the capacitance C_{via_ox} introduced by the oxide between the via and the substrate. The second one corresponds to the capacitance C_{sub} and the resistance R_{sub} of the substrate. As mentioned in the measurements results section, the backside of the wafer has been protected from the grounded chuck with a sheet of an insulating material. Nevertheless a capacitance C_{chuck} exists between them and needs to be evaluated. The capacitance between the two consecutive top metal tracks (i.e. due to the spacing SP) is characterized by C_{lines}. In the case of 1-turn 3D solenoid, C_{line} is very weak because of the small area of the top metal tracks facing each other.

The parameters values of the equivalent model are given below. All the presented values have been calculated according to physical equations and then fitted to the extracted measured parameters with the help of the optimize block under ADS.

$C_{ox\_via} = 5{,}28pF$, $C_{sub} = 49fF$, $R_{sub} = 21k\Omega$,

$C_{lines} = 1{,}5fF$, $C_{chuck} = 75fF$,

$L_{line\_top} = 175pH$, $L_{line\_bot} = 255pH$, $L_{half\_via} = 70pH$

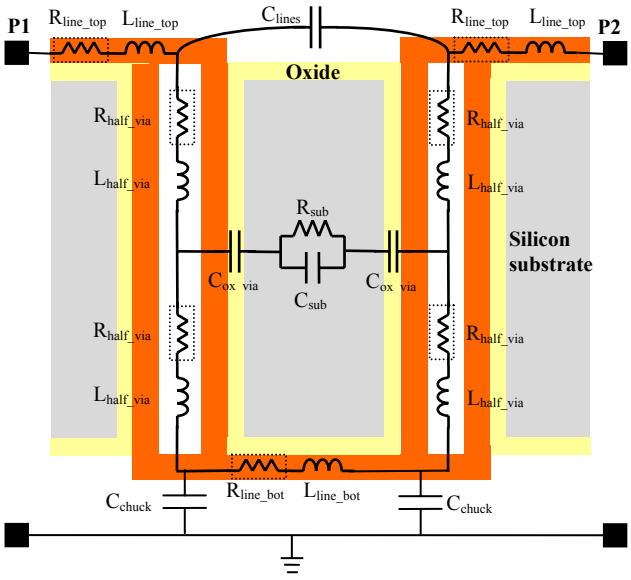
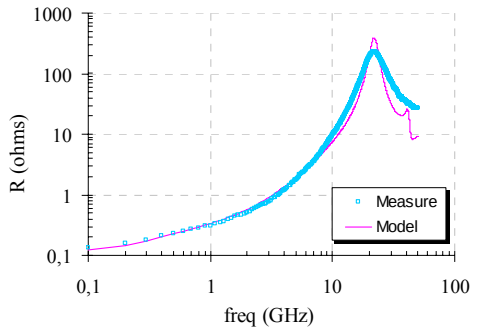
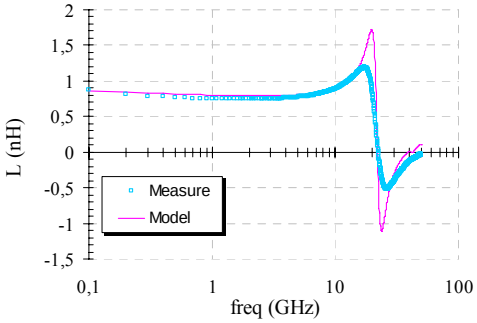


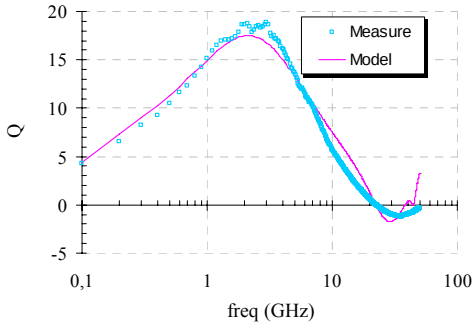
Fig. 7 The equivalent model of a 1-turn 3D solenoid



(a)



(b)



(c)

Fig. 8 Comparison between modelled (line) and measured (dot) R (a), L (b) and Q (c) for a 1-turn 3D solenoid

The relevancy of our first model is demonstrated above in Fig. 8 where measurement-extraction and model-based extraction for R, L and Q of a 1-turn 0,75nH solenoid case are compared.

V. Conclusions

In this paper, an original 3D inductor integrated in silicon and using the TSV technology is presented. Such a configuration proposes a quality factor better than planar inductors below 3GHz in CMOS and BiCMOS processes. Electrical RF characterization has been performed for 3D solenoids with 1 to 5 turns. We have demonstrated a weak coupling between vias. Hence our solenoid can easily be integrated in silicon near vias used as interconnection to bring signal or ground.

Acknowledgment

The presented structures with TSV technology were fabricated by the NXP foundry in Caen. RF characterization of the devices was realized by Dominique Bosquet.

References

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