SILICON HIGH-DENSITY CAPACITORS FOR POWER DECOUPLING APPLICATIONS

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Abstract — **Capacitors linearity and reliability at high temperature are essential for embedded Point of Load regulation applications. RL parasitic are also becoming crucial for high frequency regulators. In that perspective, we present a silicon-integrated capacitor technology enhanced for high temperature linearity and reliability. A layout approach is proposed to optimize the capacitor RL parasitic to level equivalent to best known technologies (Multilayer Ceramic Capacitors) with better frequency stability.**

Keywords—silicon capacitor; reliability; temperature; power; parasitic

I. INTRODUCTION

High density silicon based trench-capacitor technologies have been developed over the past decade by several industrial players. Their application in the field of decoupling for power management applications remained marginal because of their limited charge storage and larger Equivalent Serial Resistance. However, with the raise of converters switching frequencies (10-100MHz) application requirements for decoupling are shifting toward mid-range capacitance with low ESL/ESR and high linearity. For integration closer to the source, low temperature coefficient and ultra-low profile are becoming crucial. In that perspective, the section II of this paper presents a 3D-silicon based capacitor optimized for high temperature operation. The section III details the dielectric structure and links its electrical characteristics to reliability parameters. The section IV presents a layout method and associated model to control the ESR/ESL and PICS3 is compared with MLCC components. Finally, the section V presents an example of implementation in the field of integrated power processing.

II. THE PICS3 CAPACITOR TECHNOLOGY

The PICS3 silicon based capacitor [1] is combining a high aspect-ratio trench structure, with a multi Silicon-Isolation-Silicon capacitor. A schematic cross section of the PICS3 structure is presented on the Fig.1. The bottom capacitor electrode (HL on fig.1) is obtained by a high temperature / high dose phosphorous drive-in into the trench, enhancing the bottom electrode linearity and limiting its resistance. The upper electrodes are in-situ phosphorus doped poly-silicon layer (Ps/Ps2 on fig.2) deposited by a high temperature CVD process. Their thicknesses are maximized to obtain the best compromise between electrode resistance and

hole filling capability. Thus, the thickness of the first Ps1 electrode is reduced to facilitate deposition of the upper SIS structure.
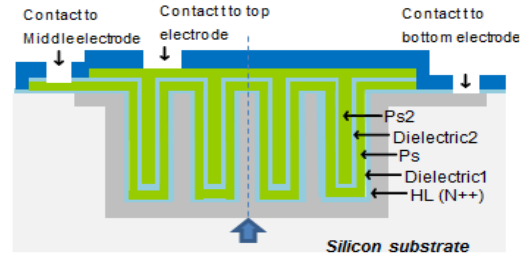

Fig.1: schematic overview of the PICS3 structure.

As a consequence, its sheet resistance is relatively high (typ. 14ohm/square) and it is the main contributor to the global capacitor ESR. Both dielectric1 and dielectic2 are oxy-nitride composites. Their contribution to the capacitor performance will be discussed in the section II.

Finally, three metal levels are available for interconnections, combining aluminum and thick copper for power routing

III. ENHANCING RELIABILITY ASPECTS

A. Dielectric processing for reliability

The main defect mechanism for PICS3 capacitors is dielectric breakdown. As for common MOS capacitors, the breakdown is mainly activated by thermal and voltage induced stresses [2], [3]. Other failure mechanisms, like current related aging effects on electrodes and interconnections, are managed by design (line width, redundancy etc…).

The dielectric strength and leakage properties are very dependent on dielectric nature. Dielectrics with large bandgap are preferred for leakage and strength control while high-*K*s are needed to increase capacitance. The optimal compromises are obtained with composite structures [2] implementing a barrier material with a large bandgap to limit charges injection combined with a high-*K* material. An illustration of this implementation for an oxy-nitride composite is presented on the fig.2, where relative thicknesses of the barriers have been varied with respect to the higher-*K* dielectric [4]. For equivalent apparent permittivity, the dielectric strength is increasing with the thickness of the barriers. Different variations of the relative thickness of the oxy-nitride

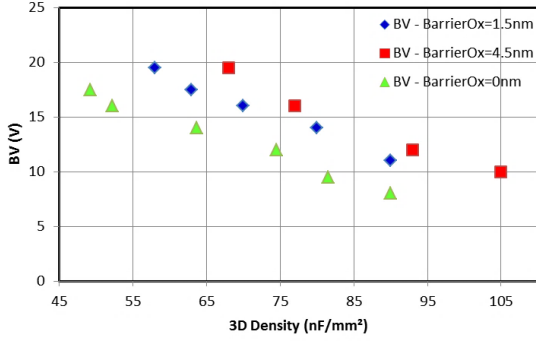composite are used in PICS3 to adapt to the application voltage span.

Fig.2: evolution of the dielectric strength with respect to composite dielectric build-up.

Besides thickness, structural defects into the dielectric layer are playing a significant role with respect to leakage and dielectric reliability [2], [5]. Indeed, dielectric aging under high field is assisted by charges circulation across the layer. Un-recombined carriers having sufficient energy, yield additional defects creation, ultimately driving to a catastrophic failure by runaway mechanisms.

Conduction mechanisms in dielectrics have been widely reported in the literature [6], [7], [8]. For relatively thick oxy-nitrides used in the PICS3 technology the Poole-Frenkel conduction dominates [6], [7]. It corresponds to a trap assisted conduction mechanism, where leakage magnitude relates to trap characteristics through the normalized relation:

$$\frac{J}{E} \propto a \; e^{\frac{-q\phi}{kT}} . e^{\frac{\beta\sqrt{E}}{kT}} \tag{1}$$

where a is a proportionality constant (related to trap density and section capture), J the leakage density, E the electrical field, β a constant related to the dielectric permittivity and Φ the traps barrier height.

The Fig.3 presents a Poole-Frenkel plot for a PICS3 oxy-nitride composite, exhibiting a linear behavior at high field with a remarkably low intrinsic leakage level.
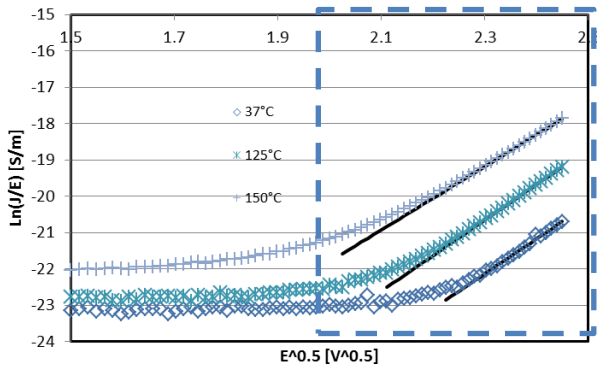

Fig.3: Poole-Frenkel plot of the leakage for the PICS3 dielectric. The black lines represent the PF fit and blue dash the typical use voltage window.

Several causes leading to the presence of traps in the oxy-nitride dielectrics [8], [9] have been identified. They are related to materials stoichiometry and processing conditions. In PICS3, the optimized leakage and strength properties are obtained through the reduction of traps density to level below

$5E^{10}$q/cm^2. This is obtained through a high temperature deposition process, including a thermal processing in dry O$_2$ for the first oxyde barrier, SiH$_2$Cl$_2$ based LPCVD for the nitride, and TEOS LPCVD for the second oxide barrier.

B. PICS3 high temperature relaiability

The dielectric lifetime of the PICS3 capacitors follows the common voltage/temperature exponential acceleration models for MOS capacitors [1]:

$$TTF \propto e^{-\gamma E_{ox}} . e^{\frac{Ea}{kT}} \tag{2}$$

where γ represents the field acceleration and Ea the thermal activation energy, the other parameters having their usual meaning. Those parameters are extracted from a Time Dependent Dielectric breakdown experiment [1]. Typical lifetimes for PICS3-LV technology are presented in the Tab.1. Remarkably the TTF model remains linear for high temperature and is validated up to 225°C.

Vg(V)	37°C	100°C	150°C	225°C
3.6	57 years	16 years	8 years	4 years
4.5	9 years	2.6 years	1.3 years	202 days
5	3.2 years	338 days	163 days	72 days

TABLE1: TTF predictions with TDDB E-model at 0.1% cumulative failures.

III. ENHANCING FUNCTIONAL ASPECTS

A. A holistic design approach to reduce parasitic

As presented in the previous sections, the PICS3 technology is using polysilicon electrodes that are intrinsically limiting the performance in term of ESR.
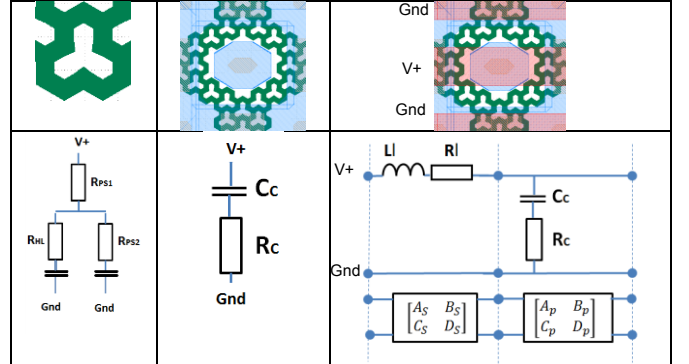

Fig.4: representation of cascading from tripod to cell level with equivalent schematic.

To overcome this issue, a layout methodology has been developed to reduce the PICS3 parasitic. It is implementing redundant contacts to successively parallelize a group of tripods in a cell interconnected to a copper grid forming the capacitor. The fig.4 gives a detailed representation of the parallelization process from the micro to macro scale. Assuming a global Π network where capacitor is inserted in reflection to the ground, the tripod distributed model is calculated using RC calculation formulas for coaxial lines. The R_cC_c scaling to cell level corresponds to the parallelization of the RC obtained at tripod level with the

addition of the resistance induced by contact and local routing. The L_l calculation for the global routing corresponds to the terms of self and mutual inductance between adjacent wires [10], and R_l corresponding to line resistance is neglected. The respective interconnection $[ABCD]_s$ and cell $[ABCD]_p$ transfer matrixes are built using following lines equations:

$$\begin{bmatrix} A_S & B_S \\ C_S & D_S \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \quad \begin{bmatrix} A_P & B_P \\ C_P & D_P \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \quad (3)$$

By cascading matrixes, the interconnected cell transfer matrix is expressed as:

$$[ABCD]_{cell} = [ABCD]_s \cdot [ABCD]_p \quad (4)$$

The distributed model for a cascade of n cells is expressed as:

$$[ABCD]_g = ([ABCD]_{cell})^n \quad (5)$$

The equivalent ESR and Self Resonance Frequency for a group of n cells can be calculated by converting the $[ABCD]_g$ matrix in $[Z]$ matrix and considering the term Z_{12} corresponding to the impedance of the vertical branch in a Π network. The fit between the model (black line) and experimental results (dots) as presented on the fig.5 is excellent. It is remarkable that ESR and SRF scale down as an inverse power function of n.
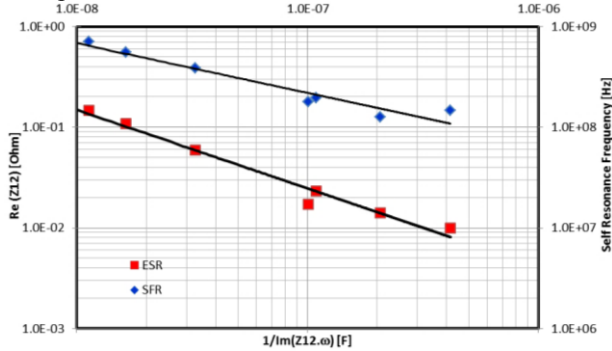
Fig.5: representation of the ESR and SRF as a function of C for groups of cells with n varying from 16 to 1064. Impedance measurements are performed at 0dBm, 25°C, 1Mhz.

As a consequence, the ESR and ESL can be set to any value by adjusting n and the number of tripods per cell for a given capacitance.
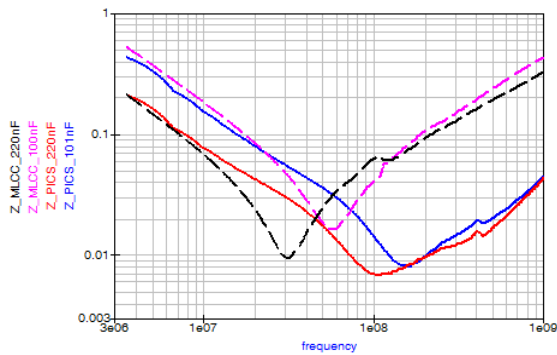
Fig.6: impedance modulus of a 100nF and 220nF capacitors. Plain line corresponds to PICS and dashed line corresponds to low-ESL commercial MLCC. Impedance measurement is performed at 0dBm, 25°C.

It must be noted that lowering the number of tripods per cell increases the relative surface used by the contacts, thus reducing the overall capacitance density.

To compare the PICS3 performance level in terms of ESR, and ESL, 100nF and 220nF reference components have been characterized and benchmarked with commercial low-ESL MLCCs. Measurements have been performed in reflection to the ground, and the impedances modulus extracted from the vertical branch of a Π network are presented on fig.6. Remarkably, the PICS3 components ESR are lower at the resonance frequency than the equivalent MLCC. Also the PICS3 resonance frequency is higher, indicating a lower ESL. In the considered range of capacitance, the ESL is varying from 3pH to 8pH giving resonance frequencies above 200MHz.

B. Voltage and temperature linearity

The linearity of a 100nF PICS3 capacitor has been characterized over its usage voltage and temperature span and compared to an equivalent low ESL commercial MLCC. As presented on the fig.7 the PICS3 voltage de-rating is extremely low and remains <0.5%.
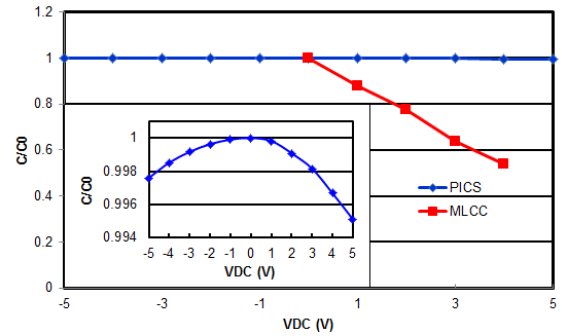
Fig.7: Voltage linearity for a 100nF capacitor. Impedance measurement at 1 Mhz, 25°C.

Similar comparison is performed with respect to temperature de-rating and corresponding results are presented on the fig.8. Remarkably the C de-rating over the temperature span remains <2%.
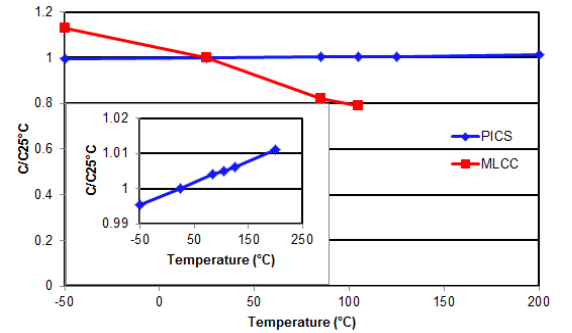
Fig.8: Temperature linearity for a 100nF capacitor. Impedance measurement at 1 Mhz, 3.5V DC bias.

IV. EXAMPLE OF APPLICATION TO BUCK CONVERTERS

The emerging embedded power processing applications, like buck converters, are using conversion frequency well above 10MHz [11]. This has the advantage to reduce components footprint, and thus gives denser integration scheme with lower parasitic which is beneficial for internal ringing and output ripple control. For those applications, C or LC interposer embedding the other active components are

becoming an obvious choice for performance (see fig.9). In this configuration the C interposer is draining the system heat and its working temperature can exceed 100°C for a large part of the product lifetime. Also, on load current step, the voltage trip on the capacitor terminals can largely exceed the nominal capacitor rating. For these reasons, voltage and temperature linearity are essential for the functional stability of the system, and suppress need for capacitance oversizing.

Reduction of the ESR is also important as it contributes to voltage drop, ripple increase and results in efficiency loss by heat dissipation.
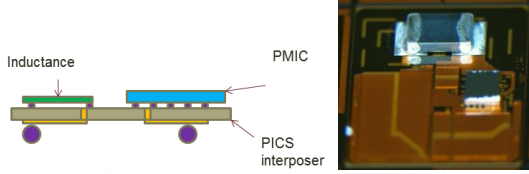

Fig.9: example of implementation of a PICS3 passive interposer embedding CIn and COut for an 11MHz embedded 15V to 3.6V POL regulator.

This is illustrated on the fig.10 where is presented the evolution of the output ripple for a 20MHz/1W single phase buck converter, with respect to the output capacitor *ESR*. The RMS contribution to the system power loss is reported on the same figure.
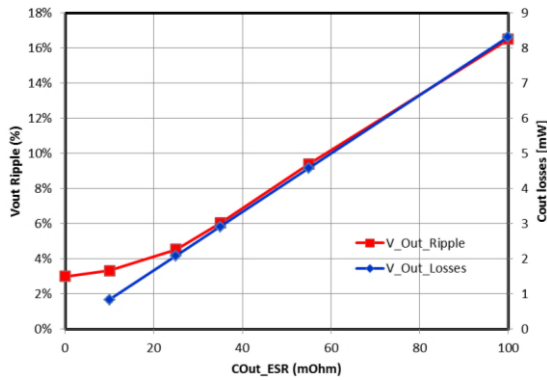

Fig.10: impact of the COut ESR onto the output voltage ripple and associated power losses on a 20MHz/1W embedded converter.

However, capacitors presented in this paper, ranging in the window from 400-10nF for an ESR of 10–100mOhm correspond to the typical targets for CIn and COut for buck converters working in the frequency space of 10-200MHz.

Additionally, reduction of the ESL allows reducing the ringing in the switches stage by lowering the VDD and GND planes loop-inductance to value <100pH. This is mostly achieved by drastic reduction of routing distances in the interposer compared to board level implementation. Furthermore, the reduced intrinsic ESL of the PICS3 capacitors < 10pH for the capacitors, are yielding resonance frequencies well above the converters switching frequencies.

V.   CONCLUSION

In this paper, a PICS3 silicon based capacitor technology is presented, that exhibits superior performances in term of linearity and reliability at high temperatures. The component lifetime de-rating model is presented and extracted

and remains very linear at temperature as high as 200°C. This result is explained by the low level of defects embedded in the composite dielectric layer, leading to reduced leakage and limited wear-out under high electrical field.

A layout approach is presented allowing tuning of the capacitors ESR and ESL that are usually the limiting factors for silicon integrated capacitors. An [ABCD] matrix cascading model is presented that allows scaling of the capacitor RLC from micro to macro-scale. The model gives an excellent fit with experimental measurements and is currently used in the pre-design phase for layout tuning. Reference PICS3 components resulting from the above design methodology have been characterized over a wide frequency range and are showing better frequency stability than MLCCs with a comparable level of ESR.

Finally, examples of application are presented in the field of embedded POL regulators. Applicative advantages resulting from more linear, low resistive capacitor are discussed.

The methodology described in this paper to enhance dielectric reliability and to optimize parasitic has led to insights to further improve the latest PICS4 technology, implementing a 500 nF/mm^2 3D SIS capacitor based upon high-*K* nano-laminates [12].

REFERENCES

[1]   F. Murray *et al* , **"**Silicon Based System-in-Package : Breakthroughs in Miniaturization and "nano"-integration Supported by Very High Quality Passives and System Level Design Tools", Session W2/V1, MRS Fall Meeting, 2006

[2]   J. Robertson, "New High-K Materials for CMOS Applications. In Comprehensive Semiconductor Science and Technology", R. Fornari (Ed.), Elsevier Amsterdam, The Netherlands, vol. 4, pp. 132–176, 2011.

[3]   "Foundry process qualification guidelines", JEDEC JP001.01, May 2004

[4]   S. Jacqueline, "Etude du dépot de diélectriques fins dans des systèmes à fort rapport d'aspect", Thèse de doctorat en Chimie des matériaux, Université de Caen, 2007

[5]   S. Mori *et al*, "ONO inter-poly dielectric scaling for nonvolatile memory applications", IEEE Trans. Electron Devices, Vol.38, pp. 386-391, 1991

[6]   J.G. Simmons, "Conduction in thin dielectric films", Journal of Physics D: Applied Physics, Vol. 4, pp. 613-657, 1971

[7]   S. Jacqueline, B. Domengès, F. Voiron and H. Murray, "Conduction mechanisms in 2D and 3D SIS Capacitors", Semiconductor Science Technologies, 28, 2013

[8]   A Dogan, "The reliability of the silicon nitride dielectric in capacitive MEMS switches", Thesis in Materials Science and Engineering, The Pennsylvania State University, 2005

[9]   "LPCVD Silicon Nitride and Oxynitride Films, Material and Applications in Integrated Circuit Technology", F. H. P. M, Habraken (Ed.), Springer-Verlag, 1991

[10]   E.B. Rosa, "The self and mutual inductances of linear conductors", Bulletin of the Bureau of Standards, Vol. 4, N°2, PP. 301-343,1908

[11]   B Allard, "State of the art of high switching frequency inductive DC-DC converters in SoC context", Power SOC 2014

[12]   A. Lefevre ,H Grampeix, F Lallemand , U Luders, W Prellier, G Parat, F Voiron, "Development of HfO2/Al2O3nanolaminates for MIM applications", WoDiM 17th Workshop on Dielectrics in Microelectronics, Dresden Germany, 2012