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Full-Wave Analysis of Inhomogeneous Deep-Trench Isolation Patterning for Substrate Coupling Reduction and Q-Factor Improvement

Sidina Wane, *Member, IEEE*, and Damienne Bajon, *Member, IEEE*

***Abstract*—Full-wave analysis of deep-trench isolation patterning (DTP) is presented for substrate coupling reduction and Q-factor improvement. Effects of the buried layer (BL) doping level and grounding mechanisms on substrate coupling are analyzed. Influences of induced depletion regions on substrate coupling are investigated. Q-factor improvement of on-chip RF inductors resulting from the interruption of BLs and part of the lossy substrate by DTP to limit electric and magnetic energy dissipation is studied. The combination of DTP with topological optimization demonstrates high Q-factor enhancement. Distributed capacitances and resistances resulting from the BL and substrate grating are evaluated. Coupling between inductors and limits of representations by lumped-element equivalent circuits to account for distributed effects are discussed. Comparison of obtained results with two-and-one-half- and three-dimensional-based commercial electromagnetic tools and with measurement data for reference structures are presented.**

***Index Terms*—Deep-trench isolation patterning (DTP), depletion regions, eddy current, floating ground plane, local and global ground reference, Q factor, RF inductors, seal ring, substrate coupling, transverse wave formulation (TWF).**

I. Introduction

MAJOR limitations of silicon-based RF integrated circuits to meet the high-performance requirements of present and next-generation communication systems principally concern parasitic couplings between sensitive function blocks and the low Q factor achievable for on-chip spiral inductors and transmission line interconnects. In order to reduce electromagnetic (EM) parasitic couplings and improve the Q factor of on-chip spiral inductors, different methodologies classified in [1] into three categories have been proposed and investigated in recent research. These three categories are, respectively, related to the optimization of inductor intrinsic parameters (thick metal interconnects [2]–[5]), architecture-based techniques (differentially driven inductors [6], [7]), and substrate stack-modification-based techniques (proton implants [8], patterned ground shields [9]–[11], micromachining substrate cavities [12], trench isolation [13], [14]). All these techniques aim at reducing various energy dissipation origins involving complex physical mechanisms that include skin effect, eddy currents, and polarization/dielectric/radiation losses. To analyze energy dissipation and coupling causes in order to select or innovate appropriate isolation strategies, EM simulation tools are required. While the Q factor of on-chip spiral inductor enhancement techniques associated with inductor intrinsic parameter optimization and architecture-related approaches can be accurately analyzed using standard EM simulators, techniques and methodologies associated to substrate stack modifications remain very challenging for numerical EM methods. Accurate incorporation in EM simulations of substrate features as depletion regions, PWells, NWells, or insulating deep-trenches, as shown in Fig. 1, necessitates the modeling of stacks of inhomogeneous layers with arbitrary doping profiles. Two-and-one-half-dimensional (2.5-D) numerical integral methods well known to provide reliable results are still limited, to the authors' best knowledge, to multilayered structures with homogeneously doped layers [15]. Three-dimensional (3-D) numerical methods, suitable for the analysis of multilayered structures with arbitrarily doped layers, are penalized by extremely implosive computation complexity resulting from the high discrepancy between the substrate features scale, on the one hand, and the layout geometrical dimensions on the other. Small geometrical details impose, for an accurate discretization, space step size often a lot smaller than what can be dictated by the smallest wavelength enclosed in the simulation-domain limits. This leads to important memory requirement and CPU computation delays even if adaptive meshing procedures are associated to frequency or time interpolations. Design rules usually elaborated from experimental studies, generally based on costly trial-and-error procedures, are highly dependent on signal frequencies, as well as on substrate stack doping profiles and, therefore, must be adapted to each new technologies.

In this paper, an original EM analysis of inhomogeneous deep-trench isolation patterning (DTP) is presented for Q-factor improvement and substrate coupling reduction. Section II discusses effects of the buried layer (BL) doping level on substrate coupling. Different grounding configurations for the BLs are considered, to estimate the impact of spatial distribution of the ground contacts on the global isolation performances between sensitive blocks. In addition, the influences of induced depletion

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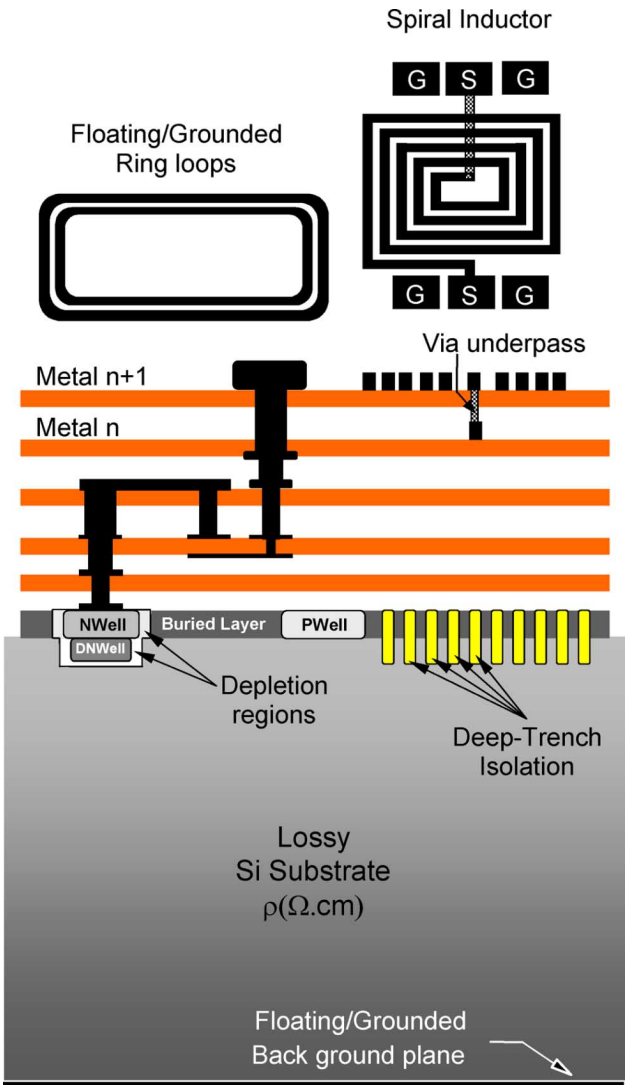

Fig. 1. Cross section of a typical RF integrated circuit showing substrate features (deep-trench isolation, PWell, NWell, depletion regions) of disparate scales and doping profiles.

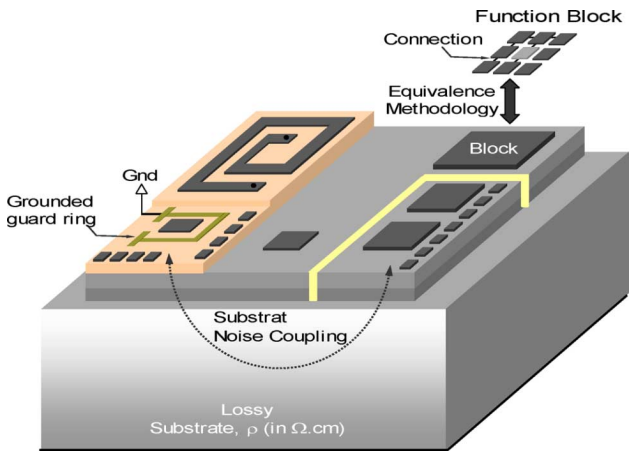

Fig. 2. Methodology replacing a function block (e.g., block 1) by a pad of similar dimension for substrate coupling analysis.

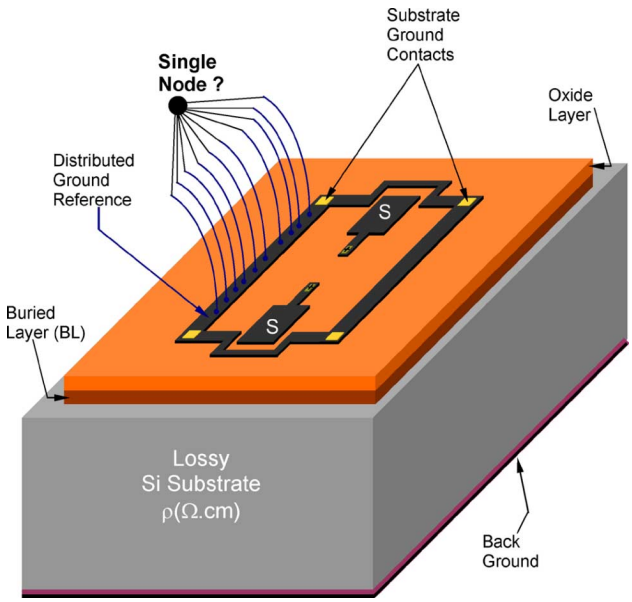

Fig. 3. View of the test structure for investigation of BLs conductivity and grounding configuration.

regions on substrate coupling are investigated. Section III discusses Q-factor improvement of on-chip RF inductors resulting from the interruption of BLs, and part of the lossy substrate by deep-trench patterning to limit electric and magnetic energies dissipation. The EM analysis is carried out using the hybrid transverse wave formulation (TWF) method [15] that associates the advantages of integral methods to the benefits and flexibility of differential approaches. Impacts of different deep-trench patterning options, as well as the influence of BL grounding on Q-factor enhancement are presented. The tradeoff between reduction of magnetic or electric energy dissipation is analyzed through the effects of deep-trench patterning penetration inside the substrate. The distributed capacitances resulting from the BLs and substrate grating are evaluated using a general methodology for extraction of circuits compact models. Comparisons of obtained results with 2.5-D- and 3-D-based commercial EM tools and with measurement data for reference structures show satisfactory agreement.

II. Effects on Substrate Coupling of Buried Layer Conductivity and Grounding: Modeling of Depletion Regions

A. Influence of the BLs Doping Level

Since complete full-chip EM analysis including couplings between integrated components and sub-block and block functions is difficult to achieve with today's available EM design tools, a methodology to simplify circuit complexity should be considered. A simple methodology, commonly used in substrate coupling analysis, consists of replacing sensitive blocks or components by pads (p+ or n+ implants, as shown in Fig. 2) of equivalent shape and geometric dimensions. For instance, at the component level p+ plugs can represent source/drain regions and n+ buried diffusions can correspond to collectors of NPN transistors. Fig. 3 shows a test structure for the investigation of substrate coupling dependence on the BL doping level. The signal

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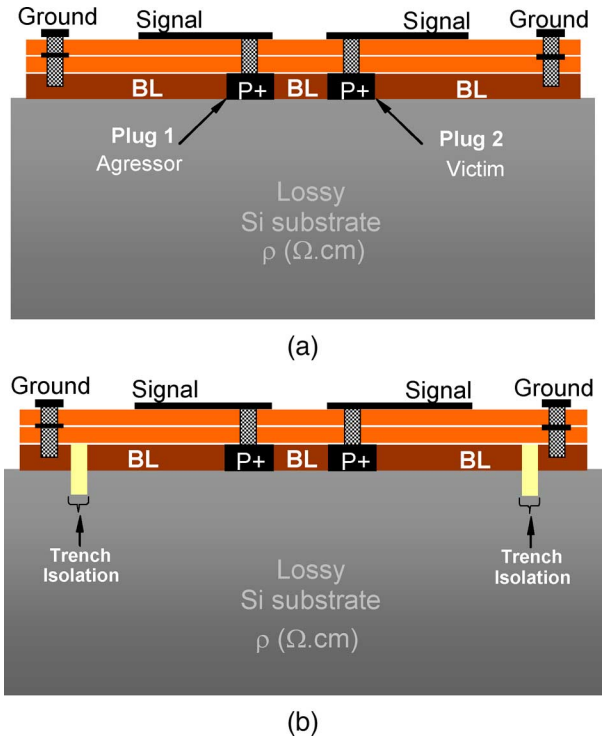

Fig. 4. Cross-sectional view of the reference structures with: (a) BL grounded and (b) BL floating by insertion of deep-trench isolation. (a) Configuration with BL grounded. (b) Configuration with BL floating.

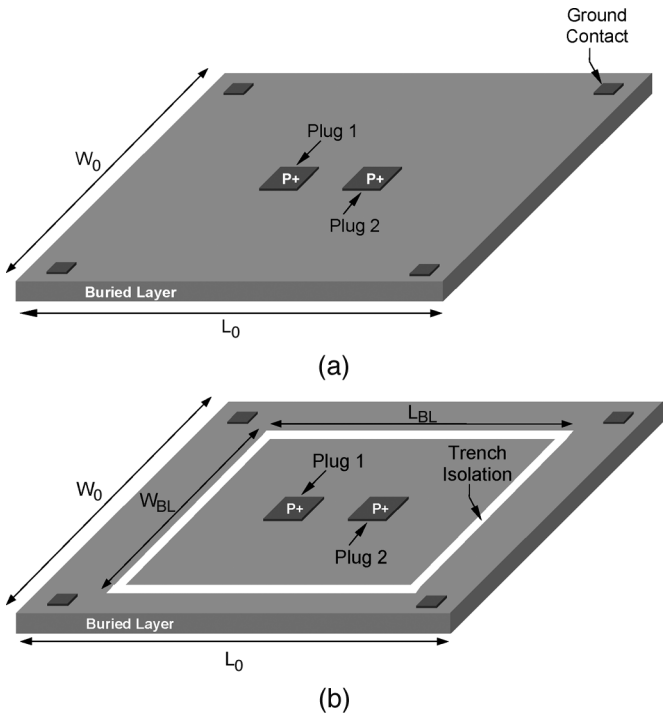

Fig. 6. Top view of the BL: (a) grounded and (b) floating configurations. (a) Configuration with continuous path between p+ plugs and ground contacts; (b) Configuration without continuous path between p+ plugs and ground contacts.

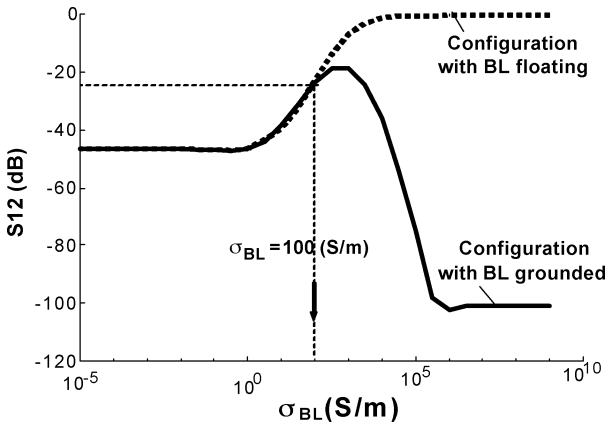

Fig. 5. Effects of the BL conductivity $\sigma_{\rm BL}$ and grounding on substrate coupling at 2 GHz for the test structure in Fig. 3.

pads (S) are connected to plug 1 and plug 2 representing the aggressor (injector) and victim (receiver), respectively, illustrated in Fig. 4.

The test structure is composed of a 500-μm-thick lossy silicon substrate with a resistivity of 20 $\Omega \cdot$ cm and a 2-μm-thick BL of conductivity $\sigma_{\rm BL}$ in siemens per meter, taken as a variable in Fig. 5, covered with an insulating silicon dioxide layer. The ground seal ring on the metal 6 level is connected to the BL by four substrate contacts through via-holes, as shown in Figs. 3 and 4. The evolution of the coupling S_{12} between the p+ plugs against the BL conductivity $\sigma_{\rm BL}$ at 2 GHz for the two different grounding configurations in Fig. 4(a) and (b) is presented in Fig. 5.

The floating configuration of the BL Fig. 4(b) is obtained by introducing a 1.5-μm-thick trench isolation ring to isolate, from the ground contacts, the portion of the BL where the p+ plugs are diffused. This floating configuration poses some difficulties to standard 2.5-D EM design tools. The principal difficulties concern the accurate simulation of the boundary conditions at the limits of the BL domain bounded by the isolation trench ring [see Fig. 4(b) or Fig. 6(b)]. Table I shows the comparisons between different EM approaches [TWF, Sonnet Software, Momentum, High Frequency Structure Simulator (HFSS)] and measurement. The measurements are reported for $\sigma_{\rm BL} = 1000$ S/m. In Table I, the symbol "x" corresponds to situations not being properly simulated using the associate EM tool (according to the current versions). In Sonnet Software, the grounded option can be easily simulated, although the floating option is difficult to analyze because of the presence of the box imposing electric wall boundary conditions at the limits of the stack of layers.

In Momentum software, as the layer stack is assumed to have infinite space extension [$L_o = \infty$ and $W_o = \infty$ in Fig. 6(a)], the grounded option is difficult to simulate; while using HFSS, particular attention has to be paid to the definition of radiating or absorbing boundary conditions matching with surrounding free space. Issues on the convergence of the simulation results against the meshing procedure also have to be considered.

As $\sigma_{\rm BL}$ increases, in Fig. 5, the BL becomes more conductive and the two p+ plugs are more and more sensitive to grounding configuration of the BL. This sensitivity of the BL to the spatial distribution of grounding contacts [16] can give rise to very different isolation performances, in particular for high values of

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TABLE I
COMPARISON BETWEEN DIFFERENT EM TOOLS FOR THE SIMULATION OF THE TEST STRUCTURES IN FIG. 4. AT 1 GHZ

EM Approach	S_{11} and S_{12} at 2 GHz for BL Grounded -Fig. 4(a)- and BL floating -(Fig. 4(b)- with different doping profiles σ_{BL}							
	$\sigma_{BL} = 10^3$ S/m				$\sigma_{BL} = 10^5$ S/m			
	BL Grounded		BL Floating		BL Grounded		BL Floating	
	S_{11} dB	S_{12} dB	S_{11} dB	S_{12} dB	S_{11} dB	S_{12} dB	S_{11} dB	S_{12} dB
TWF Method	-4	-20	-4.9	-9.5	-0.01	-71	-52	-0.5
Mom. Software.	x	x	-5	-10	x	x	-55	-0.4
Sonnet Software.	-3.8	-20	x	x	-0.02	-72	x	x
HFSS Software.	-5	-22	-6	-10	-0.04	-73	-53	-0.7
Measured data	-3.7	-19.5	-5	-10.5				

$\sigma_{\rm BL}$. Since the ground ring and the BL cannot be rigorously assimilated to a single node despite their small dimensions (see Fig. 3), static (electrostatic or magnetostatic) approaches do not lead to accurate results [17] and full-wave attributes of the coupling have to be considered. In Fig. 5, the grounded and floating configurations for the BL exhibit roughly the same behavior against $\sigma_{\rm BL}$ for values less than or equal to 100 S/m [17]. However, for $\sigma_{\rm BL}$ greater than this limit, the two configurations lead to very different results.

The floating configuration shows a saturated, but monotonous variation of the coupling parameter S_{12} against $\sigma_{\rm BL}$: as $\sigma_{\rm BL}$ increases, the impedance between the two p+ plugs decreases and the coupling becomes more and more significant. The grounded configuration leads to very low coupling for very high values of $\sigma_{\rm BL}$ due to the short circuit impressed between the ground and signal contacts in Fig. 4(a). The observed low coupling in this case has to be considered as virtual since the associated insertion losses are dominant. Table I illustrates the virtual coupling observed for high-conductivity values of $\sigma_{\rm BL}$. With $\sigma_{\rm BL} = 10^5$ S/m, in Table I, $S_{12} = -71$ dB and $S_{11} = -0.01$ dB are obtained for the grounded configuration, while for the floating option, $S_{12} = -0.5$ dB and $S_{11} = -52$ dB. Even for moderate values of the BL conductivity ($\sigma_{\rm BL} = 10^3$ S/m in Table I), noticeable differences can be observed between the grounded and floating options.

A normalized coupling parameter C_{12} given in (1), accounting for both the insertion and coupling parameters, has to be considered for optimum power transfer evaluation

$$C_{12} = \frac{|S_{12}|}{\sqrt{1-|S_{11}|^2}}. \qquad (1)$$

High absolute values of $C_{12\rm in}$ in decibels lead to a poor insertion parameter, while lower absolute values result in weak isolation performance. Applying (1) for $\sigma_{\rm BL} = 10^5$ S/m gives $C_{12} = -0.49$ dB and $C_{12} = -44.61$ dB, respectively, for the floating and grounded options.

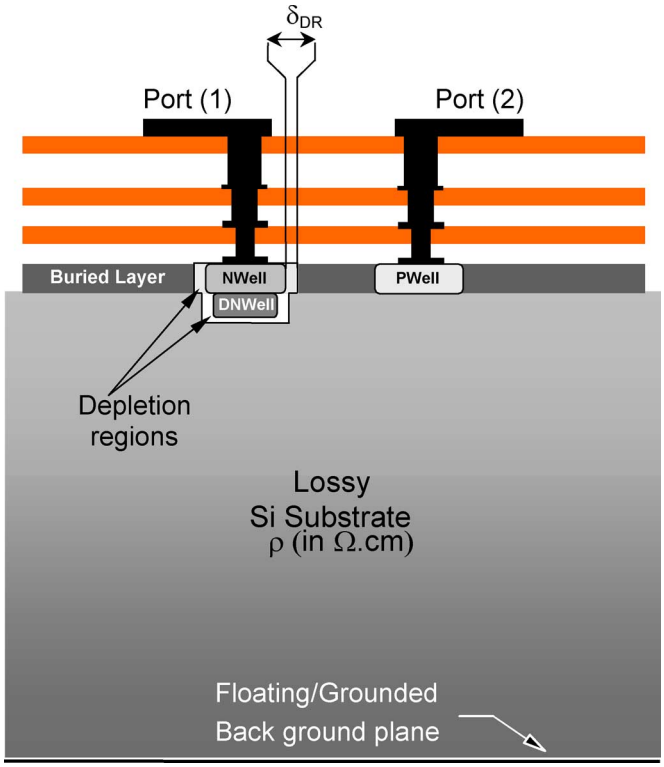

Fig. 7. Cross-sectional view of a typical CMOS structure with depletion regions NWell/p-BL and DNWell/substrate.

B. Influence of Depletion Regions

Depletions layers contribute to the frequency response of the substrate and may have significant influence on the coupling paths. The depletion regions shown in Fig. 7 result from the difference in doping level between the NWell region and the buried p-layer, on the one hand, and the deep NWell (DNWell) and the Si substrate, on the other. NW-BL designates the depletion region between the NWell region and the BL, and DNW-BL represents the depletion region between the DNWell region and Si substrate. The depletion region width is $\delta_{\rm DR}$. The NWell and DNWell thickness and resistivity are taken, respectively, equal to 0.75 μm and 4×10^{-4} $\Omega \cdot$ cm. In Fig. 7, the PWell region has the same conductivity and thickness as the BL. Fig. 8(a) compares the insertion (S_{11}) and coupling (S_{12}) parameters against frequency of the structure in Fig. 7 with ($\delta_{\rm DR} \neq 0$) and without ($\delta_{\rm DR} \equiv 0$: reference structure) including depletion regions. Comparison between EM-simulation results with the TWF method and an equivalent-circuit model built on frequency independent R (resistance), L (inductance), C (capacitance), and G (conductance) elements in Fig. 8(b) shows satisfactory agreement for signal frequencies up to 40 GHz.

The general RLCG equivalent-circuit model of the structure without depletion layers, composed of frequency-independent lumped elements, which constitutes the "intrinsic part" in Fig. 8(b), does not result from any estimation or fitting procedure, but from exact identification between EM simulation and equivalent network responses. $C_{\rm BL}(\sigma_{\rm BL})$, $R_{\rm BL}(\sigma_{\rm BL})$, and $L_{\rm BL}(\sigma_{\rm BL})$, respectively, represent the capacitance, resistance, and inductance values associated to the electrical behavior of the BL. $G_{\rm Sub}(\rho) = 1/R_{\rm Sub}(\rho)$ is the substrate conductance and $C_{\rm Sub}(\rho)$ represents the substrate capacitance. Table II

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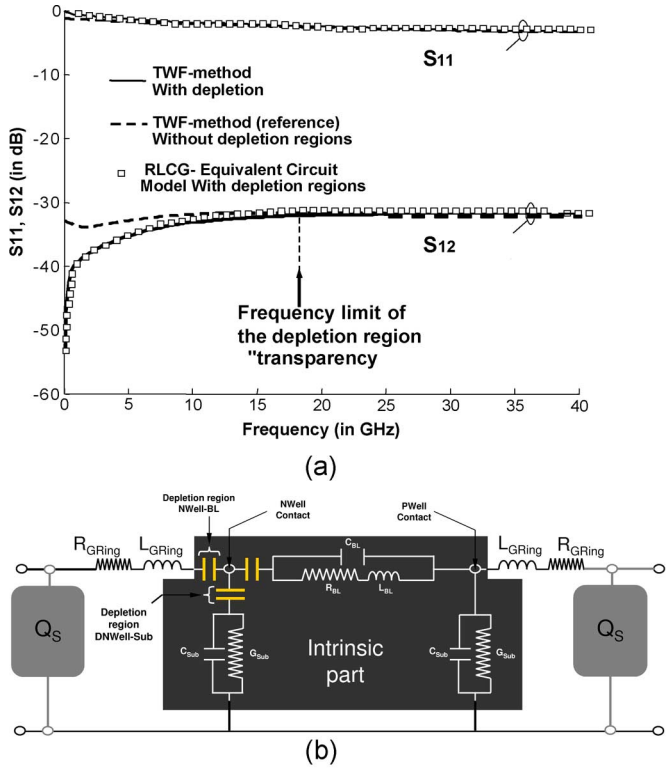

Fig. 8. S_{11}- and S_{12}-parameters against frequency of the structure in Fig. 7: Comparison between: (a) EM simulation results and general RLCG model. (b) Asymmetric RLCG equivalent network including depletion region capacitances.

TABLE II
RLCG EXTRACTED VALUES FOR THE ELECTRICAL EQUIVALENT CIRCUIT IN FIG. 8(b)

RLCG Parameter Elements	R_{Sub} (Ω)	C_{Sub} (fF)	R_{BL} (Ω)	L_{BL} (nH)	C_{BL} (fF)	$C_{NW\text{-}BL}$ (fF)	$C_{DW\text{-}BL}$ (fF)
Extracted Values TWF-simulation	615	18	3300	0.15	0.16	16	112

gives the nominal values extracted from EM simulations for the intrinsic part of the equivalent circuit in Fig. 8(b).

The depletion region NW-BL is represented by the vertical (peripheral) capacitance $C_{\mathrm{NW-BL}}$. The depletion region DNW-BL is approximated by the horizontal capacitance $C_{\mathrm{DNW-BL}}$. Both $C_{\mathrm{NW-BL}}$ and $C_{\mathrm{DNW-BL}}$ are inserted in the equivalent network as lumped elements between parallel and serial coupling branches without modifying the obtained values of the $RLCG$ elements extracted from the EM simulation of the structure without depletion layers. The equivalent network obtained in this way demonstrates in Fig. 9 its capability to predict the results obtained with the EM simulation including the depletion layers. In Fig. 8(b), the two-ports Q_S are related to the parasitics resulting from the numerical EM exciting sources or measurement probing. Fig. 8(a) shows that the effects of the depletion regions become transparency at high frequency, around 20 GHz for the considered nominal values.

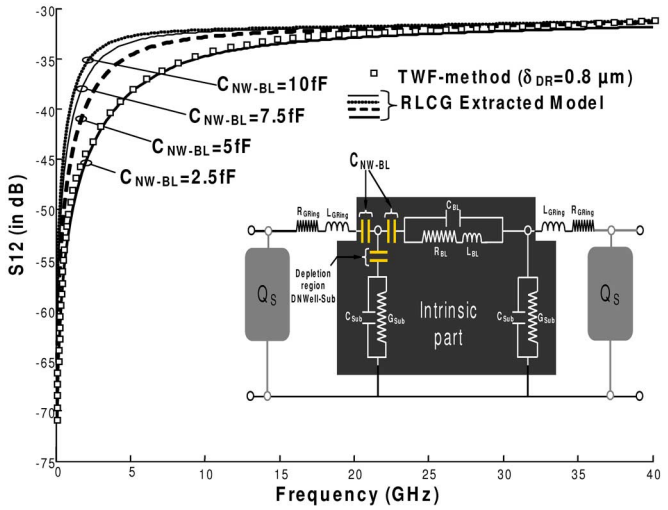

Fig. 9. Effects of the depletion region capacitance CNW-BL on the coupling parameter S_{12} against frequency: comparison between the RLCG model and EM simulation (for $\delta_{\mathrm{DR}} = 0.8\ \mu$m) results.

Fig. 9 presents the evolution against the frequency of coupling parameter S_{12} deduced from the RLCG model for different values of the depletion layer peripheral capacitance ($C_{\mathrm{NWBL}} = 2.5, 5, 7.5,$ and 10 fF). The EM simulation results for a depletion region width $\delta_{\mathrm{DR}} = 0.8\ \mu$m are in good agreement, particularly at low frequency, with the RLCG model results for a peripheral capacitance $C_{\mathrm{NWBL}} = 2.5$ fF.

C. Effects of Local and Global Ground References

The analysis of RF or microwave circuits generally refers to specified input and output ports for the determination of their parameters (scattering, impedance, or admittance parameters). In nodal analysis, a port is reduced to a node (with zero spatial extension) defined as a two-terminal element: one terminal corresponding to the signal and the other representing the common "global" ground reference. However, in EM analysis, a port has a nonzero spatial extension (assumed to be small in regard to the wavelength for an univocal definition of voltages and currents) and cannot always be referred to as a "global" ground. To accurately account, in EM analysis, for real measurement conditions, the probing pattern used in the measurement setup protocol must be included in the simulation. Fig. 10 shows a coplanar waveguide (CPW) pattern used for the analysis of a device-under-test (DUT). The finite extension of the floating lossy ground plane renders the definition of a common ground reference difficult because of the resulting attenuation and delay in the ground return current. Moreover, as EM excitation sources most often assume uniform distribution of EM fields [see Fig. 11(a) and (b)], the port discontinuities are represented in Fig. 10 by the two-port Q_S identified to the Z_{series}, Y_{shunt}, and N elements, which may corrupt the interpretation of the numerical simulation results.

To investigate the impact on EM couplings of "local" and "global" ground references illustrated in Fig. 12(c), the two grounding options shown in Fig. 12(a) and (b) are considered. Fig. 12(a) corresponds to a floating lossy ground seal ring and Fig. 12(b) represents a numerically auto-grounded microstrip (MST)-like configuration. The MST-like configuration could also be considered with a floating ground option (by toggling the auto-ground reference). The seal ring configuration could

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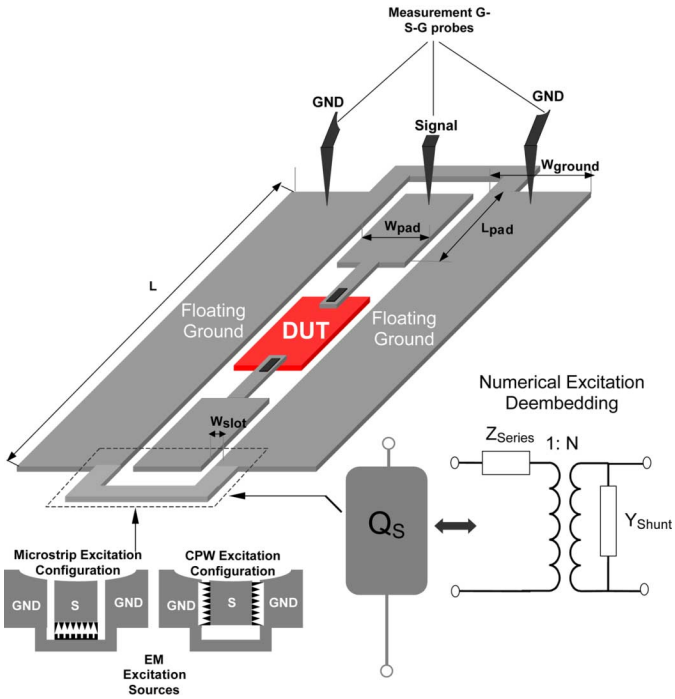

Fig. 10. CPW GSG pattern for the analysis/measurement of a DUT and illustration of current density and electric field, respectively, in MST and CPW numerical EM excitations.

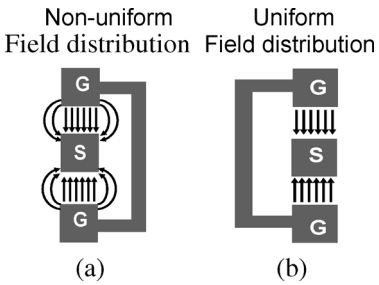

Fig. 11. (a) Nonuniform (real excitations) field distribution and (b) uniform field (numerical excitations) distribution on the exciting port regions.

be associated to the auto-grounded option (by connecting auto-ground reference) as well. These two complementary combinations are not represented in Fig. 12 due to space restrictions.

The wiring inductances (L_{Feed}) and serial resistances (R_{Feed}) of the feeding interconnections contacting the signal pads to the DUT and the seal ring electrical lumped elements L_G and R_G representation are rigorously deduced from EM simulations results of Fig. 13 with an original deembedding procedure for floating ground references.

Fig. 13 shows the simulated S-parameters of the seal ground ring without a DUT or interconnect [see Fig. 12(a)] and with a 400-μm-long transmission line (as shown in the inset) in the floating ground reference option.

In Fig. 14, the floating ground reference configuration in Fig. 12(a) is referred to as CPW configuration and compared to the auto-ground configurations in Fig. 12(b) for the computation of the coupling parameter S_{12} against frequency of the test structures in Fig. 6. Significant differences can be observed between the floating ground reference and the auto-grounded options. The auto-grounded option is investigated for both

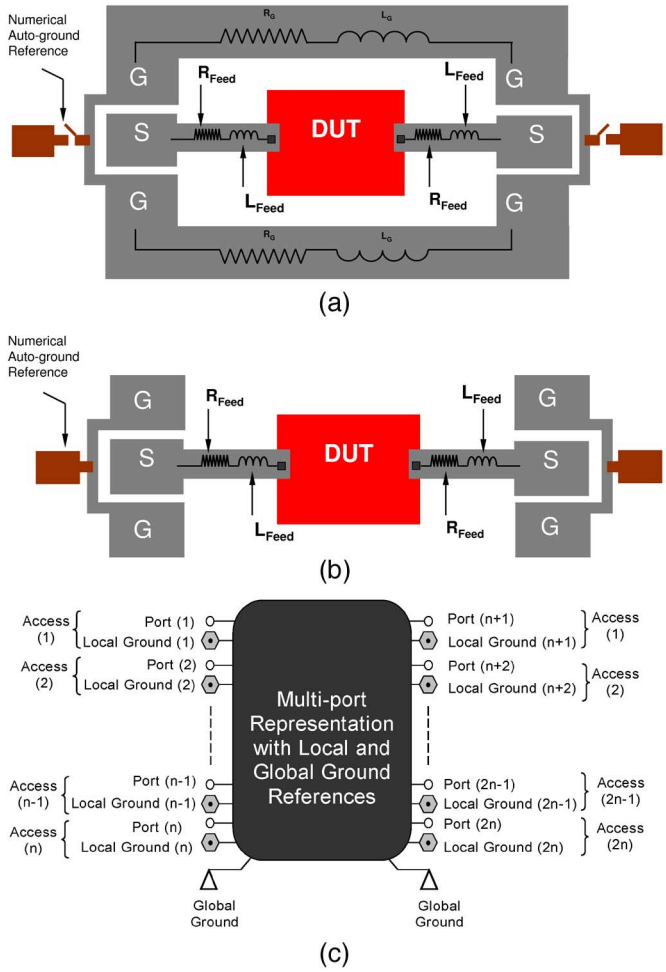

Fig. 12. (a) Two-port with floating ground reference. (b) Two-port with numerically auto-grounded reference. (c) Multiport with local and global ground references.

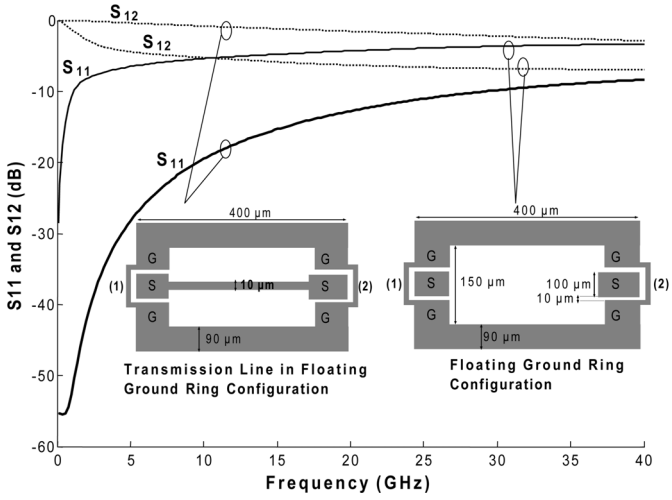

Fig. 13. S_{11} and S_{12} against frequency of a coplanar transmission line with floating seal ground ring: characterization of the seal ground ring.

MST and CPW excitations illustrated in the inset of Fig. 10; noticeably different behavior has to be underlined. It is essential to notice that the S-parameters in Fig. 14 include the effects of the numerical source discontinuities (two-port Q_S) and

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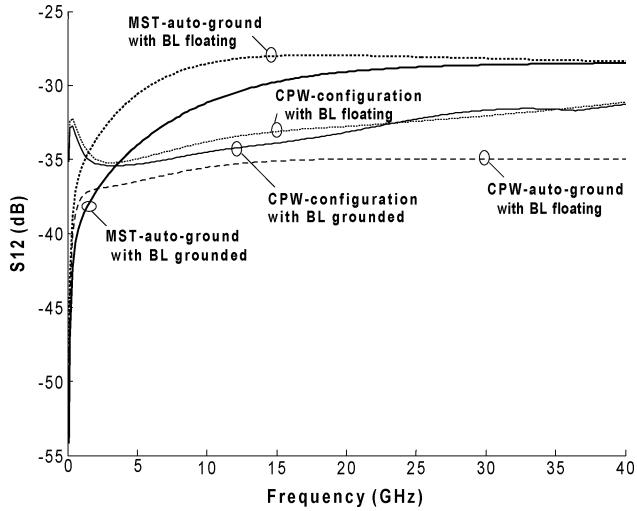

Fig. 14. Comparison between the floating ground reference option and the auto-ground configuration for the computation of the coupling parameter S_{12} against frequency of the structures in Fig. 6.

the parasitics L_{Feed}, R_{Feed}, L_G, and R_G resulting from the inductances and resistances of the feeding interconnects and seal ground ring.

The coupling parameter exhibits a nonmonotonous behavior against frequency for the floating CPW configurations. At low frequency (less than 5 GHz in Fig. 14), a coupling decreasing in magnitude as the frequency increases is observed due to the presence of the floating seal ground ring. However, at high frequency, coupling increasing in magnitude as the frequency increases is observed. Both for the MST option and CPW configuration, floating BLs lead to greater coupling.

III. Interruption of BLs by DTP

A. Effects of DTP on EM Coupling Between Interconnects: Influence of Floating Ring Loops

To investigate the effects of the metal topology on the deep-trench isolation performances to reduce EM coupling, the two test case structures shown in Fig. 15 are simulated using the TWF method. In the first test case structure of Fig. 15(a), the two ground–signal–ground (GSG) probes, with the associated feeding lines, represent the aggressor (noise source or excitation) and the victim separated by concentric floating ring loops. The second test case in Fig. 15(b) represents two coupled interconnect lines separated by the concentric rings, as in Fig. 15(a).

Couplings dependence against the number of ring loops (turns) for the test case structure in Fig. 15(a) is investigated in Fig. 16: as the number of ring loops decreases, isolation performances decreases at low and moderate frequencies.

This is not true at high frequency, above 20 GHz, because of various higher order effects. The influence of different options of deep trench patterning on EM coupling is shown in Fig. 17(a). The options without DTP and without floating ring loops correspond to the reference structures with the BL [assuming the nominal values for the conductivity (1000 S/m) and thickness (2 μm)]. It is observed, but not reported here for conciseness reasons, that floating ring loops can significantly corrupt isolation performances in presence of low-resistivity BLs in both test-

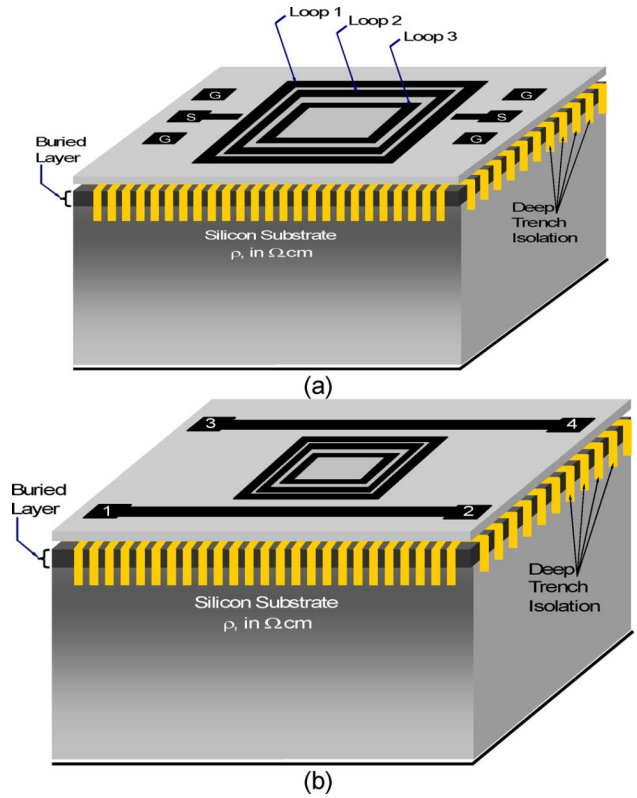

Fig. 15. Reference structures with floating ring loops for: (a) high- and (b) low-impedance configurations for investigation of metal topology effects on the efficiency of deep trench patterning (DTP-X and DTP-Y).

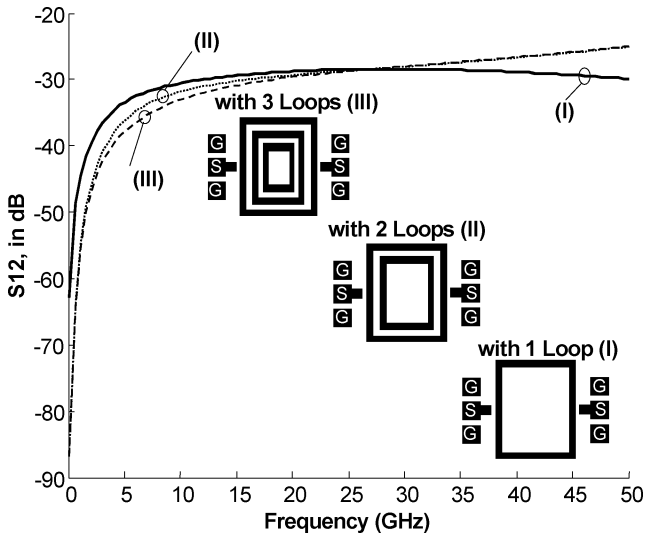

Fig. 16. Coupling against the frequency for different number of ring loops.

case structures. However, introducing DTP leads to important reduction of coupling effects. In the case of the test-case structure with interconnect lines, the existence of privileged directions for the DTP has to be observed [18]. In Fig. 17(a), DTP-X and DTP-Y, respectively, represent deep trench patterning in the x- and y-directions, namely perpendicular or parallel directions to the interconnect lines in Fig. 15(b).

The interruption of the BL and part of the silicon substrate by DPT-X leads, in Fig. 17(a), to better isolation performances

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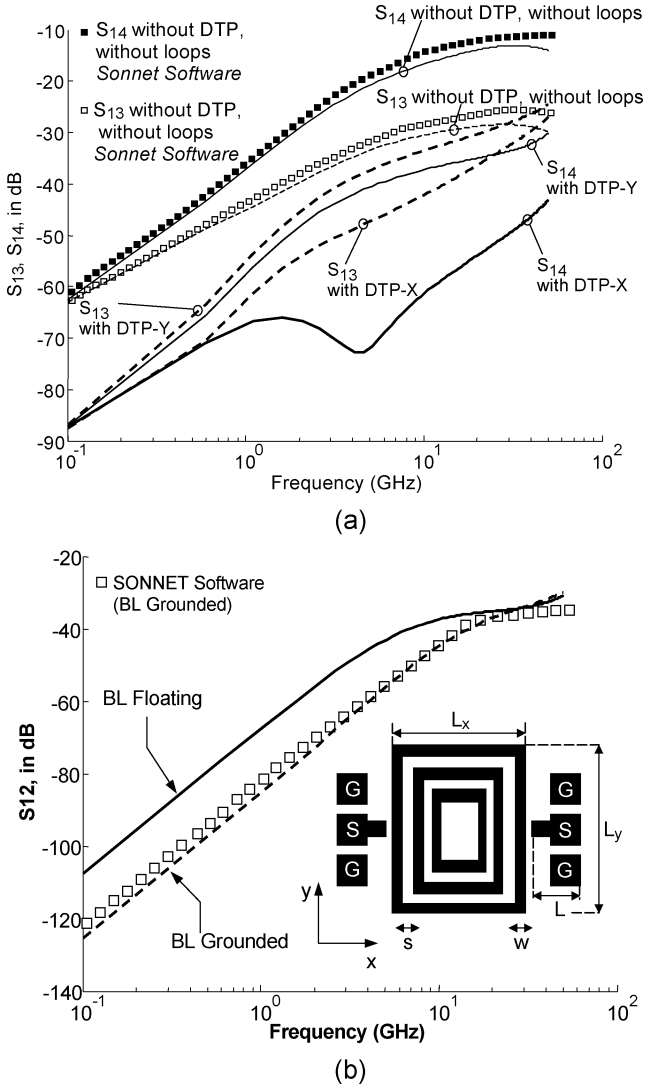

Fig. 17. (a) Isolation and coupling parameters against frequency for various options of deep trench patterning (DTP-X, DTP-Y). (b) Impacts of BL grounding on coupling with floating ring loops. The parameters are $L_x = 300\ \mu$m, $L_y = 430\ \mu$m, the separation distance between ring loops $s = 18.75\ \mu$m, $w = 37.5\ \mu$m, the length of the interconnect lines $L_{lines} = 600\ \mu$m, the spacing between lines is $d = 470\ \mu$m.

(increased absolute value of S_{13}- and S_{14}-parameters) up to 50 GHz. Fig. 17(b) compares isolation performances in the presence of floating ring loops for grounded and floating BL. For the grounded configuration of the BL, comparison of the obtained simulation results with Sonnet Software simulations shows satisfactory agreement (for reference structures without DTP).

B. Effects of DTP on the Q Factor of Spiral Inductors

The penetration of the magnetic field into the substrate stack causes magnetic energy losses that result in low-Q factor and substrate coupling problems. In order to increase the impedance paths of undesirable eddy currents induced by the magnetic field in the substrate stack, DTP is introduced underneath the inductor to interrupt the lossy BL and part of the lossy silicon substrate, as illustrated in Fig. 18. Fig. 19 shows the effect against frequency of low-resistivity BL (BP layer) beneath the inductor on the Q factor.

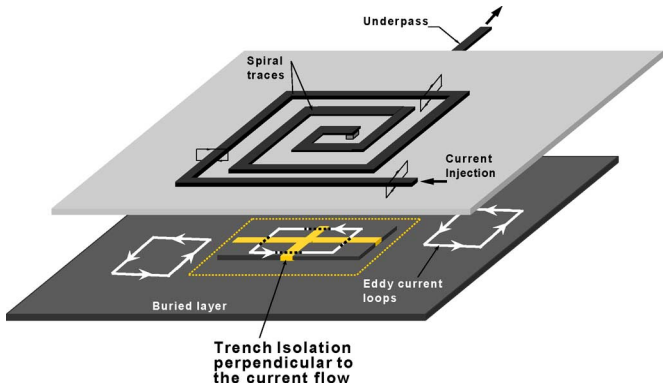

Fig. 18. Eddy current induced by spiral inductor magnetic field on semiconducting layers: insertion of trench isolation to increase impedance path of eddy current.

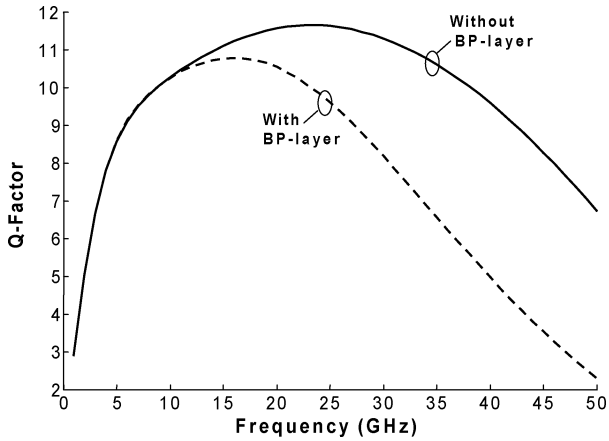

Fig. 19. Influence of a BL (BP-Layer) on the Q factor against frequency.

Removing the BL increases both the Q factor and the vertical electric field penetrating into the substrate. A tradeoff between reduced eddy currents and limited penetration of vertical electric field can be obtained in breaking the underlying BL and Si substrate by the deep trench patterning. In fact, the deep trench patterning acts as blocking p-n-p junctions perpendicularly to the spiral inductor traces. As the blocking deep trench patterning imposes local high-impedance boundary conditions, it must be narrow enough to limit losses resulting from the penetration of vertical electric field into the substrate stack.

The impact of a deep trench patterning on the Q factor against frequency is presented in Fig. 20(a) in reference to deep trench patterning options shown in Fig. 21, and in comparison with a reference structure without deep trench patterning. The option BP designates the case where deep trench patterning is limited to the BP layer. Option BP-Si represents the case where the deep trench patterning penetrates both the BP and Si substrate. Options BP-G and BP-F, respectively, refer to configurations where the BP is grounded and floating.

It is seen that the deep trench patterning leads to a higher Q factor when the BL is floating. In addition to interrupting the BL, penetration of the deep trench patterning inside the Si substrate improves the Q factor in the BP-Si-G case.

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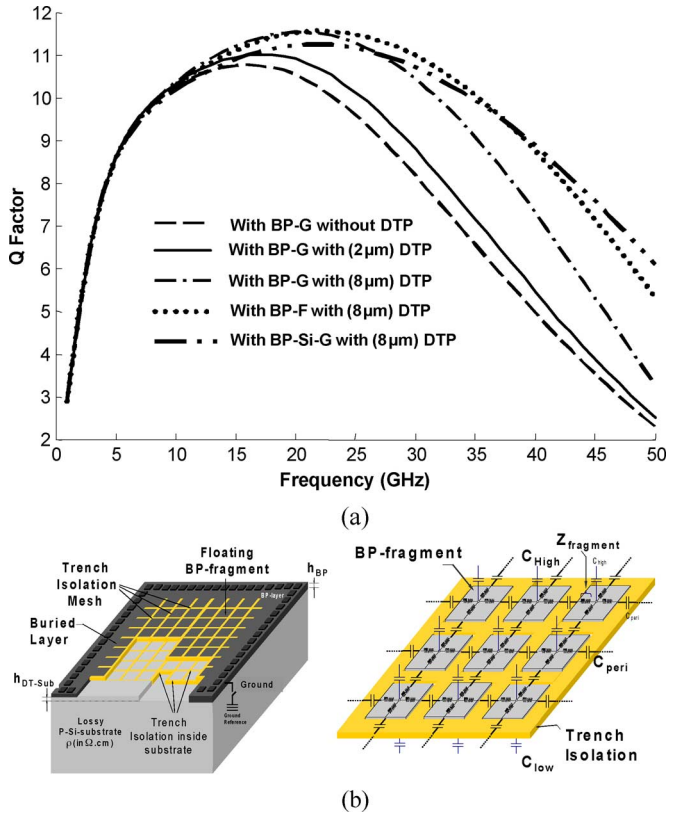

Fig. 20. Effects of the DTP on the Q factor versus frequency: (a) impact of the penetration depth ($h_{\mathrm{DT-Sub}}$) into the substrate and of BL BP grounding. (b) View of deep trench patterning interrupting the BL and part of the substrate, distributed capacitances from [1].

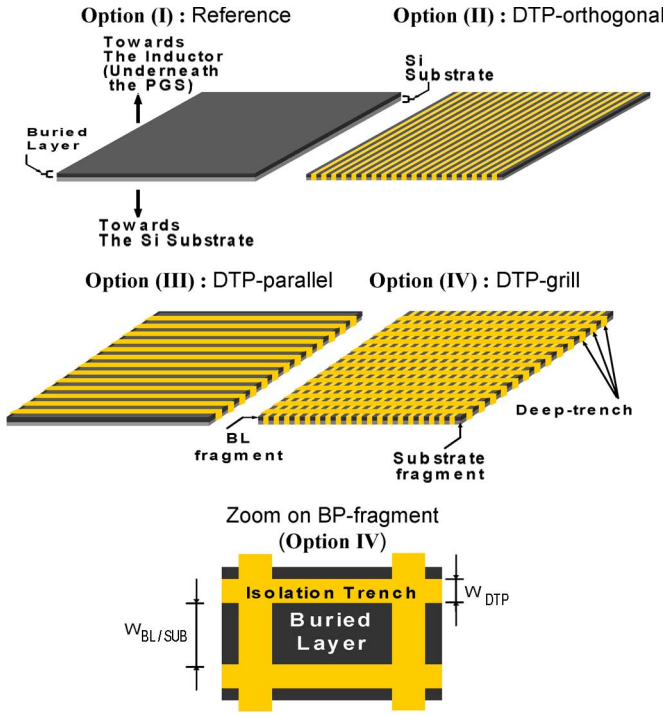

Fig. 21. View of different deep trench patterning options and zoom on the interrupted BL according option IV from [1].

The Q factor is computed using the following conventional definition (2), directly drawn from energy dissipation considerations, where y_{in} designates the short-circuit input admittance of the spiral inductor

$$Q = 2\pi \frac{E_{\mathrm{stored}}}{T \times P_{\mathrm{dissipated}}} \cong 2\omega \frac{|\overline{W}_m| - |\overline{W}_e|}{P_{\mathrm{dissipated}}} = \frac{-\mathrm{Im}(y_{\mathrm{in}})}{\mathrm{Re}(y_{\mathrm{in}})}. \tag{2}$$

In (2), $P_{\mathrm{dissipated}}$ designates the dissipated power, T denotes the period, and ω is the pulsation. The approximation of the total stored energy $|\overline{W}_m| - |\overline{W}_e|$ represents the difference between the average stored magnetic and electric energies. Such approximation in terms of admittance parameters (for a two-port model) is only valid when $|\overline{W}_m|$ is much greater than $|\overline{W}_e|$ as the proposed definition for the Q factor drops to zero at the resonant frequency. Other definitions for the Q factor can be considered and compared [19]. In this study, we restrict ourselves to the conventional definition in (2).

The interruption of the BL and a part of the Si substrate results in floating BL and Si fragments. This introduces distributed capacitances with the traces of the spiral inductor C_{high} with the noninterrupted part of the Si substrate C_{low} and with other surrounding fragments C_{peri}, as illustrated in Fig. 20(b). Average extracted values of 0.30 and 0.13 fF/μm are obtained for C_{high}, respectively, without and with deep trench patterning at 0.1 GHz.

This shows that the deep trench patterning considerably reduces the capacitance to substrate. The per square sheet resistance of the BP fragments [real part of Z_{fragment} in Fig. 20(b)] is $R_{\mathrm{BP}}(R_{\mathrm{BL}}) = 590\ \Omega/\square$ at 0.1 GHz.

Comparative analysis in terms of the maximum Q factor of the four options for the deep trench patterning in Fig. 21 leads to the following design rule where the symbol $\succ\succ$ denotes potentially greater than

$$Q_{\mathrm{option(IV)}} \succ\succ Q_{\mathrm{option(III)}} \succ\succ Q_{\mathrm{option(II)}} \succ\succ Q_{\mathrm{option(I)}}. \tag{3}$$

Such a design rule has to be carefully understood as strongly dependant on the relative values of the substrate and BL resistivities, on one hand, and on the considered frequency range, on the other.

C. Comparison With Measurement Results and With Other Relevant EM Methods

A 4.5-turn on-chip square inductor is considered as a reference structure for comparison with published measurement data [13] and with simulation results from commercial EM tools.

The outermost strip of the inductor (on metals 5 and 4) is 200 μm with a strip width of 14 μm and a turn-to-turn spacing $s = 3$ μm. Metal 5 is separated from the substrate by a 7.1-μm-thick silicon dioxide. The first five rows of Table III present comparisons between our simulation results using the TWF method and measurement data with and without deep trench patterning ($W_{\mathrm{DTP}} = 1.5$ μm). Comparison with simulation results from the method-of-moments-based commercial EM tools without deep trench patterning is also reported in

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TABLE III
COMPARISON WITH MEASUREMENT DATA [13] AND COMMERCIAL EM SOFTWARE FOR THE REFERENCE STRUCTURE IN PART FROM [1]

METHODS	Q_{MAX}	$F_{RES.}$ GHz	L_{ind} nH	C_{ind} fF	R_{ind} Ω	C_{Si} fF	R_{Si} Ω
Method of Moment reference without DTP	6.15	11	4.5	11.2	6.3	110	580
Measurement reference [13] without DTP	6.43	11.3	4.12	10	6.77	100	600
This work TWF-method reference without DTP	6	11	4.25	11	6.20	110	595
Measurement reference [13] with DTP	7.5	11.5	4.12	10	6.77	66.9	748
This work TWF-method reference with DTP	8	11.75	4.25	11	6.20	63	730
This work TWF-method Improved Structure	31.5	12	4.4	9.5	1.66	55	780

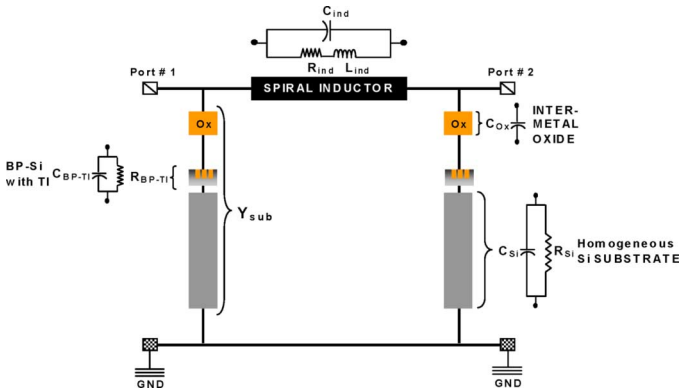

Fig. 22. Simple Pi-equivalent-circuit model of the inductor from [1].

Table III. The columns of Table III, respectively, refer to the Q-factor maximum value $Q_{\max}$, the resonant frequency $F_{\rm res}$—at which the Q factor drops to zero—and, considering the Pi-equivalent circuit model in Fig. 22 for the reference structure, the inductor value $L_{\rm ind}$, the parallel capacitance $C_{\rm ind}$, the serial resistance $R_{\rm ind}$ and the homogenous substrate elements $C_{\rm si}$ and $R_{\rm si}$.

The last row of Table III presents improved performances of the on-chip inductor resulting from a combination of deep trench patterning and topological optimization.

Although the concept of layout optimization for inductors has already been mentioned in previous studies [20], its application in conjunction with DTP is original and has never been proposed, to the authors' best knowledge.

The idea of topological optimization consists of choosing a different strip width for each inductor turn. Wider width for the outer turns reduces ohmic losses, predominant in the external turns, while narrow width is considered for the inner turns, where the magnetic field is maximum.

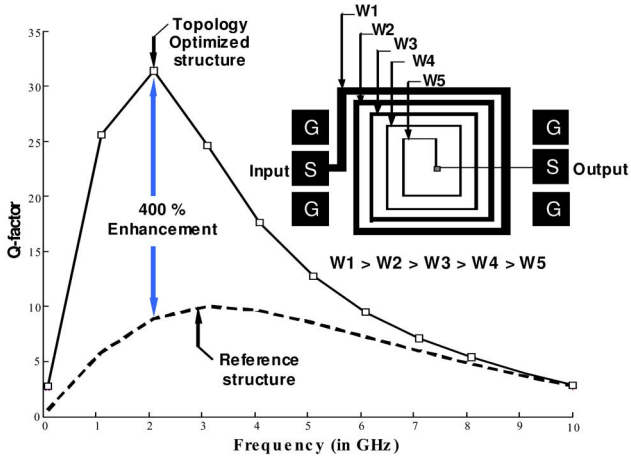

Fig. 23. Q-factor enhancement resulting from DTP isolation in conjunction with topology optimization from [1].

Fig. 23 shows the Q factor of the improved structure against the frequency in comparison with the reference structure, demonstrating a significant enhancement of approximately 400% for the maximum Q factor.

In Fig. 24(b), the influence against frequency of the BL grounding on the coupling between the two square inductors shown in Fig. 24(a) is presented. Each inductor has the geometric properties of the reference structure in Table III. It is observed that a floating BL induces more coupling than a grounded BL, particularly at high frequencies. Fig. 25(a) and (b) shows the distribution of the current density magnitude on the interface between the BL and Si substrate, respectively, with and without deep trench patterning (option IV of Fig. 21). Reduced dissipated power can be observed when deep trench patterning is interrupted by the BL.

D. Extraction of Compact Circuit Model Parameters for Back Annotation of Parasitic Elements

Methodology for Compact Circuit Model Parameters Extraction: Starting from EM analysis results, the methodology for model parameter extraction uses a rational function representation of transfer functions to approximate impedance or admittance parameters as a ratio of polynomials [21]–[23]. Casting impedance or admittance matrix elements in a pole-residue form gives a straightforward way to determine compact equivalent-circuit models composed of frequency-independent elements. This allows for the derivation of a general wideband N-Pi equivalent-circuit representation shown in Fig. 26 that properly accounts for the different behaviors resulting from skin effect, eddy-current losses, and semiconductor doping profiles space variation. Limits of single Pi-network representations are discussed in [24] and [25].

The extraction procedure first determines the unknown complex coefficients of the numerator and denominator polynomials in (4) for a given function $F(\omega)$ representing the series

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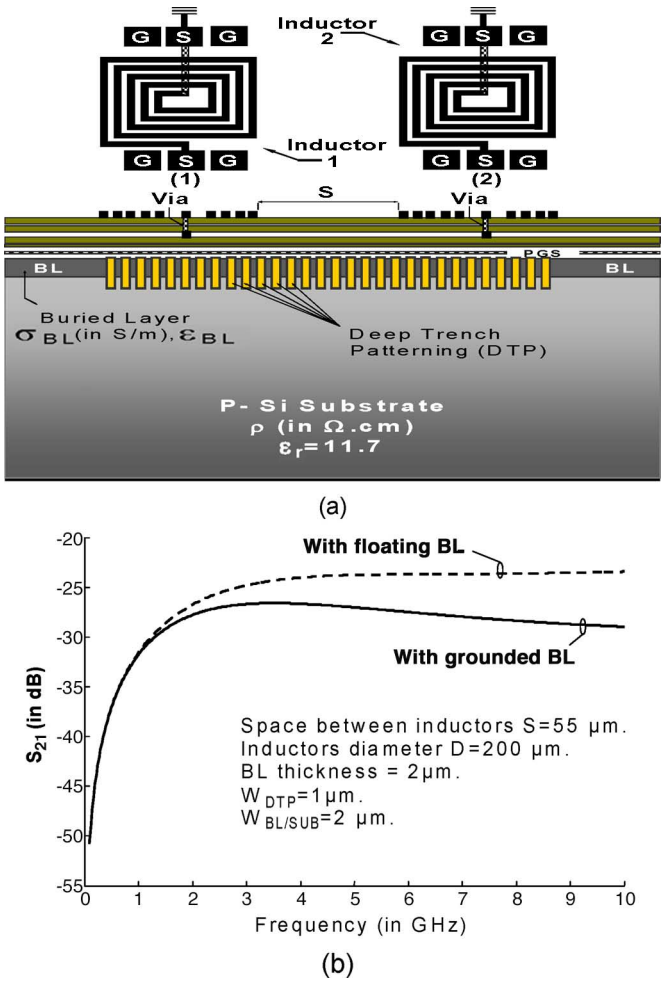

Fig. 24. (a) View of two coupled on-chip inductors. (b) Evolution of the coupling $S21$-parameter against frequency for the reference structure: effects of the BL grounding from [1].

impedance $Z_{Sk}(\omega)$ or the shunt (parallel) admittance $Y_{Pk}(\omega)$ in Fig. 26

$$F(\omega) = F_r(\omega) + jF_i(\omega) = \frac{\sum_{k=0}^{p} \underline{n}_k s^k}{1 + \sum_{k=1}^{p} \underline{d}_k s^k} \tag{4}$$

where $F_r(\omega)$ and $F_i(\omega)$ are, respectively, the real and imaginary parts of the rational function $F(\omega)$ with $s = j\omega$, with ω denoting the pulsation and assuming a normalization $\underline{d_0}$ to unity with $\underline{n_k} = n_k + jn'_k$ and $\underline{d_k} = d_k + jd'_k$.

Taking p an odd integer without loss of generality, the expansion of (4) gives

$$F_r(\omega) - n_0 + \sum_{q=1}^{(p-1)/2} \left(F_r(\omega)d_{2q} - F_i(\omega)d'_{2q} - n_{2q}\right)(-1)^q \omega^{2q} - \sum_{q=0}^{(p-1)/2} \left(F_i(\omega)d_{2q+1} + F_r(\omega)d'_{2q+1} - n'_{2q+1}\right)(-1)^q \omega^{2q+1} = 0 \tag{5}$$

$$F_i(\omega) - n'_0 + \sum_{q=1}^{(p-1)/2} \left(F_i(\omega)d_{2q} + F_r(\omega)d'_{2q} - n'_{2q}\right)(-1)^q \omega^{2q} + \sum_{q=0}^{(p-1)/2} \left(F_r(\omega)d_{2q+1} - F_i(\omega)d'_{2q+1} - n_{2q+1}\right)(-1)^q \omega^{2q+1} = 0 \tag{6}$$

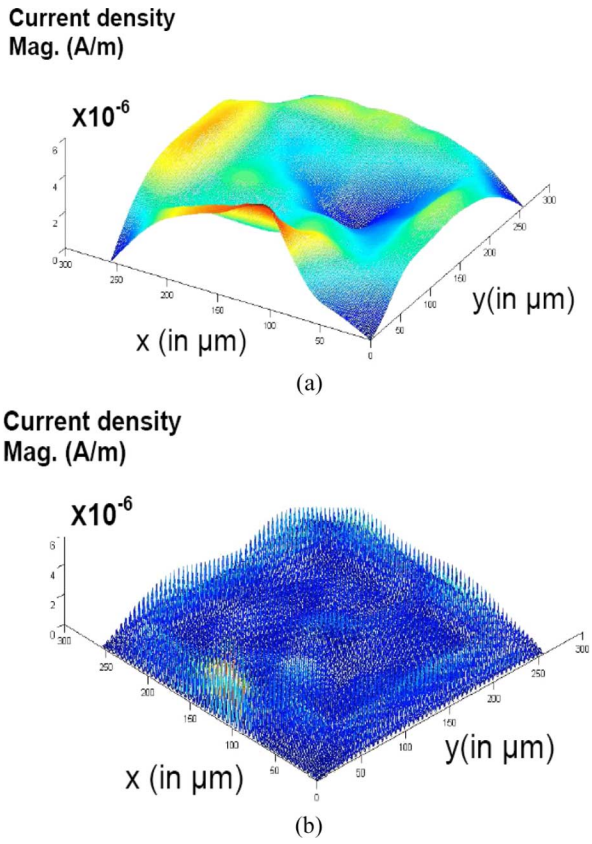

Fig. 25. Current density distribution at 2 GHz on the interface between the BL and the Si substrate: (a) without and (b) with deep trench patterning (option IV of Fig. 21). From [1]. (a) BL level without DTP (Option I). (b) BL level with DTP (Option IV).

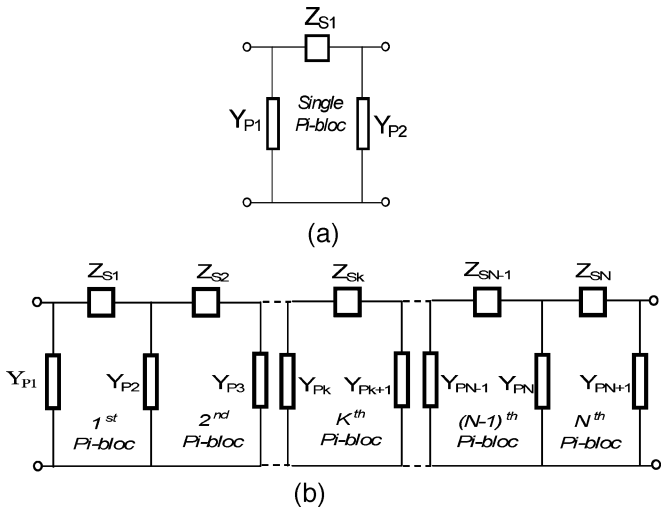

Fig. 26. (a) Single Pi-equivalent circuit. (b) Generalized N-Pi-equivalent-circuit representations.

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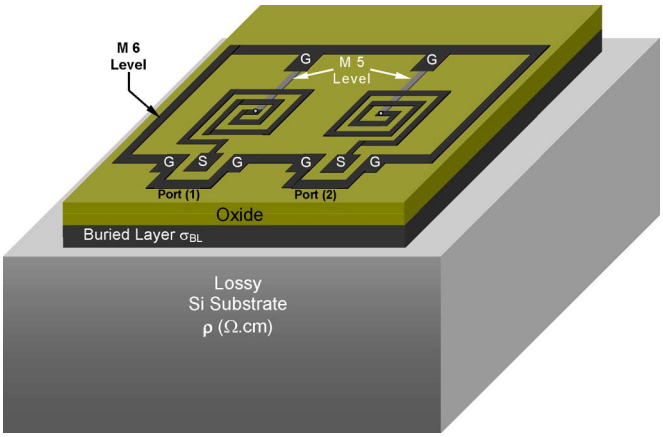

Fig. 27. Electrical equivalent-circuit representation of the two-coupled inductors.

for the real and imaginary parts, respectively. From (5) and (6), a linear set of algebraic equations (7) is built where the vector $X_{n,d}$ collects the unknown coefficients n_k, n'_k, d_k, and d'_k of the polynomials in the numerator and denominator of (4)

$$M(\omega, F_r, F_i) \times X_{n,d} = g(\omega, F_r, F_i). \tag{7}$$

The rectangular matrix M and the vector g both depend on the frequency and on the real and imaginary parts of the rational function $F(\omega)$. Once the vector of the unknown coefficients is determined using an appropriate numerical technique (enhanced QR factorization optimal for ill-conditioned large matrix systems), the denominator of $F(\omega)$ is factored to obtain the stable poles

$$F(\omega) = F_{\text{direct}}(\omega) + \sum_{v=1}^{m} \sum_{r=1}^{R_{\text{Max}}} \frac{r_r}{(s - P_r)^v}. \tag{8}$$

In (8), $F_{\text{direct}}(\omega)$ is the direct term and P_r is the pole of order r with a multiplicity v. r_r designates the residue of order r, with R_{Max} being the total number of poles.

Extraction of Spiral Inductor Models: The extraction of a general and compact model of two coupled on-chip inductors in Fig. 27 uses a symmetric single pi equivalent-circuit representation shown in Fig. 26(a) for each inductor. $L_{\text{ind},j=1,2}$, $R_{\text{ind},j=1,2}$, and $C_{\text{ind},j=1,2}$, respectively, designate the series inductance, series resistance, and series feed-forward capacitance. The BL conductance $G_{\text{BL},j=1,2}$ and parasitic capacitance $C_{\text{BL},j=1,2}$ in series with the substrate conductance $G_{\text{Sub},j=1,2}$ and parasitic capacitance $C_{\text{Sub},j=1,2}$ and the inter-metal capacitance $C_{\text{Ox},j=1,2}$ represent the shunt element of the inductor equivalent circuit.

In Table IV, the nominal values of $G_{\text{BL},j=1,2} = 1/R_{\text{BL},j=1,2}$, $C_{\text{BL},j=1,2}$, $G_{\text{Sub},j=1,2} = 1/R_{\text{Sub},j=1,2}$, $C_{\text{Sub},j=1,2}$, and $C_{\text{Ox},j=1,2}$ extracted from EM simulations for the reference inductor structure of Table I are reported. Since for design reasons the inductance value $L_{\text{ind},j=1,2}$ are not really tunable, only effects of the element parameters $R_{\text{ind},j=1,2}$, $G_{\text{BL},j=1,2}$, $C_{\text{BL},j=1,2}$, $G_{\text{Sub},j=1,2}$, and $C_{\text{Sub},j=1,2}$ on the Q factor will be studied.

TABLE IV
EXTRACTED SUBSTRATE ELEMENTS IN FIG. 3(b)

Substrate Parameter Elements	C_{Ox1} =C_{Ox2} (fF)	R_{Sub1} =R_{Sub2} (Ω)	C_{Sub1} =C_{Sub2} (fF)	R_{BL1} =R_{BL2} (Ω)	C_{BL1} =C_{BL2} (fF)
Extracted Values (TWF-method)	130	650	110	Variable nominal =600	variable

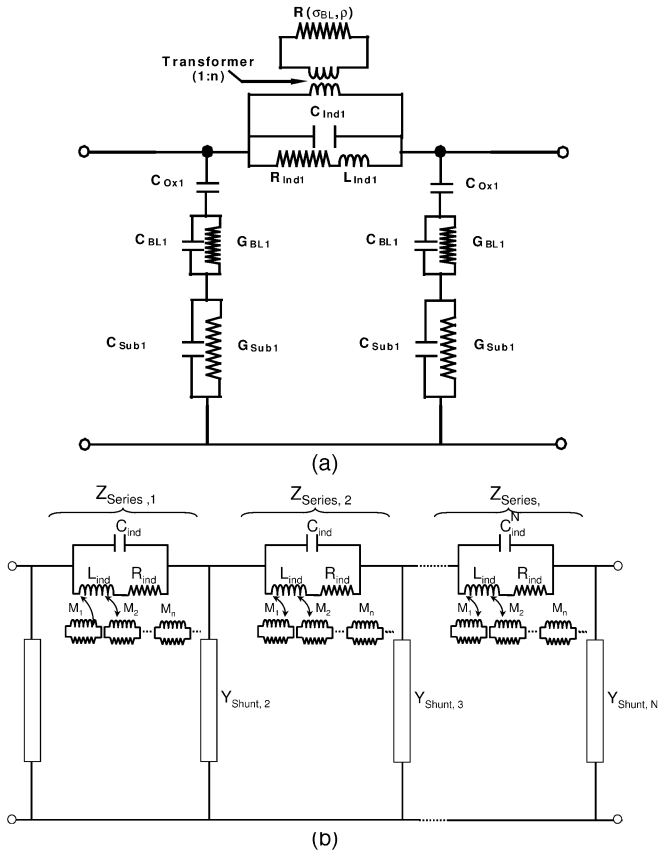

Fig. 28. Insertion of a parasitic transformers in the equivalent-circuit representation of a single inductor to account for magnetic losses: (a) in single π-network and (b) in generalized N-Pi-network.

Closed-form expressions of the real and imaginary parts of the short-circuit input admittance y_{in} for a single spiral inductor in the inset of Fig. 23 are given by (9) and (10)

$$\text{Re}(y_{\text{in}}) = \underbrace{\frac{1}{R_{\text{ind}}} \times \frac{1}{1+Q_{\text{ind}}^2}}_{\substack{\text{Inductor intrinsic} \\ \text{contribution}}} + \underbrace{\frac{\omega^2 R C_{\text{ox}}^2}{1+\omega^2 R^2 (C_{\text{ox}}+C)^2}}_{\substack{\text{Substrate Stack intrinsic} \\ \text{contribution}}} \tag{9}$$

$$\text{Im}(y_{\text{in}}) = \underbrace{\omega C_{\text{ind}} - \frac{1}{R_{\text{ind}}} \times \frac{Q_{\text{ind}}}{1+Q_{\text{ind}}^2}}_{\substack{\text{inductor intrinsic} \\ \text{contribution}}} + \underbrace{\omega C_{\text{ox}} \times \frac{1+\omega^2 R^2 C (C+C_{\text{ox}})}{1+\omega^2 R^2 (C+C_{\text{ox}})^2}}_{\substack{\text{Substrate Stack intrinsic} \\ \text{contribution}}} \tag{10}$$

where $Q_{\text{ind}} = (\omega L_{\text{ind}}/R_{\text{ind}})$, $R = R_{\text{BL}} + R_{\text{Sub}}$, and $C = (C_{\text{BL}} \times C_{\text{Sub}})/(C_{\text{BL}} + C_{\text{Sub}})$

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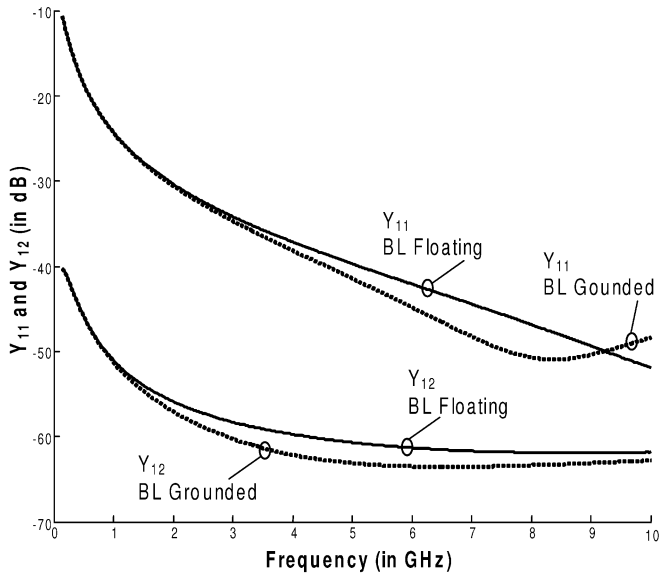

Fig. 29. Effects of BL grounding on the magnitude of Y_{11}- and Y_{12}-parameters against frequency for the two square coupled inductors.

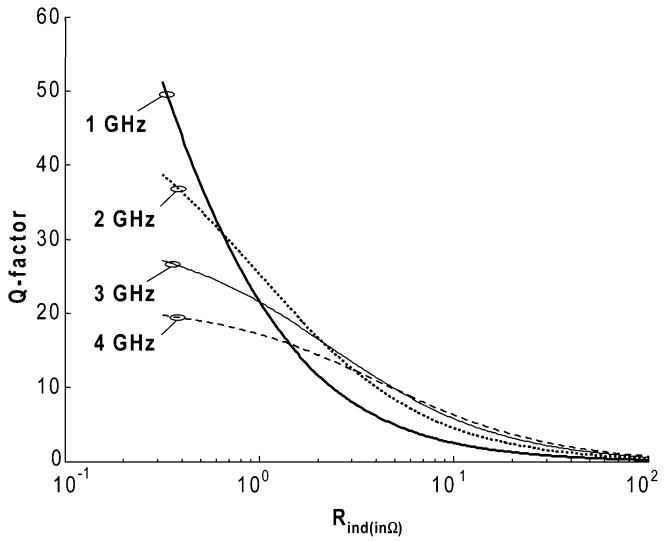

Fig. 30. Evolution of the conventional Q factor against the inductor series resistance at different frequencies.

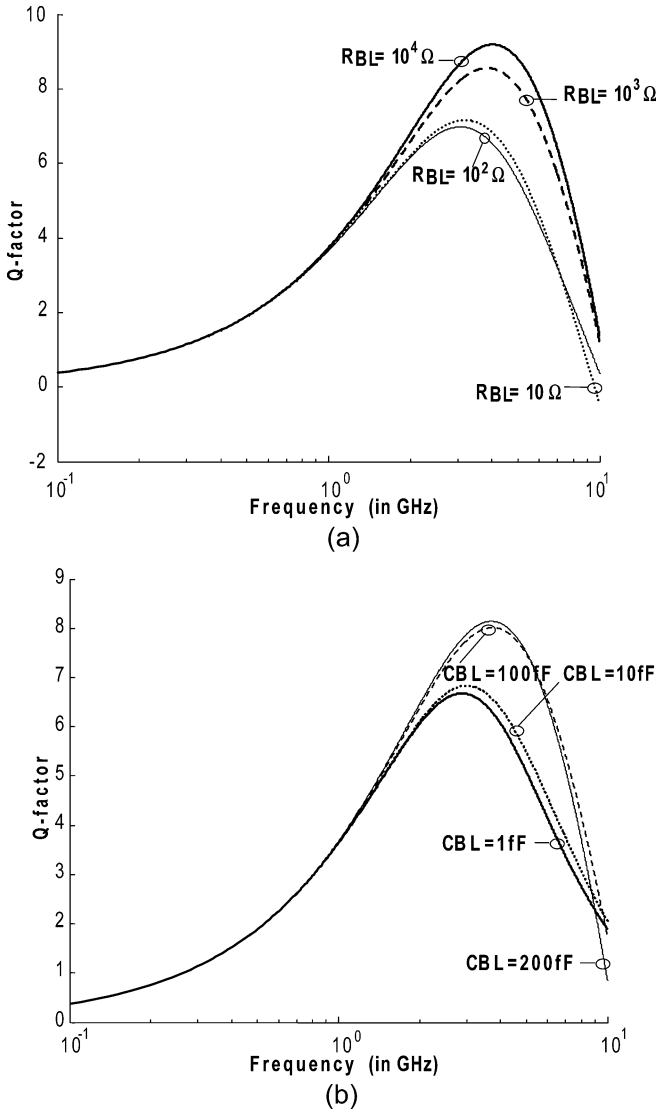

Fig. 31. Evolution of the conventional Q factor against frequency: (a) for different values of $R_{\rm BL}$ and (b) for different values of $C_{\rm BL}$.

The closed-form expressions split the real and imaginary parts of $y_{\rm in}$ into separate contributions of the intrinsic inductor contribution and the intrinsic substrate stack contribution. Thus, (9) and (10) inspired by the equivalent-circuit representation in Fig. 22 do not show coupling through magnetic losses between the intrinsic inductor elements ($L_{\rm ind}$, $R_{\rm ind}$, and $C_{\rm ind}$) and the substrate stack parameters ($C_{\rm Ox}$, $R_{\rm BL}$, $C_{\rm BL}$, $R_{\rm Sub}$, and $C_{\rm Sub}$). Such magnetic coupling can be accounted for by adding to the equivalent circuit a parasitic transformer with a secondary winding connected to R representing the equivalent resistance of the BL and Si substrate, as illustrated in Fig. 28. The parasitic transformer $(1:n)$ adds the terms $n^2 \times (R_{\rm ind}/R(\sigma_{\rm BL},\rho))$ and $n^2 \times (\omega L_{\rm ind}/R(\sigma_{\rm BL},\rho))$, respectively, to the real and imaginary parts of $y_{\rm in}$ in (9) and (10). Theses two terms will account for the coupling between the intrinsic inductor contribution and the intrinsic substrate stack contribution. This coupling is one of the main reasons why general conclusions on deep trench efficiency are closely related to the involved resistivities and frequency ranges.

In the general pole-residue form of (8), the series impedance in the N-pi equivalent-circuit representation can be modeled using the following relation:

$$R_{\rm Ind} + j\omega L_{\rm ind} - Z_{{\rm Series},k}(\omega) = \sum_{n=1}^{N} \frac{K_{M_n}}{R_n + j\omega L_n} \qquad (11)$$

where $R_{\rm Ind}$ and $L_{\rm ind}$, respectively, represent the dc resistance and dc inductance with $M_n = j\omega\sqrt{K_{M_n}}$ denoting a mutual inductance contribution in Fig. 28.

The shunt (or parallel) admittance $Y_{\rm Shunt}$ in Fig. 28(b) is given by the following relation:

$$(Y_{\rm Shunt}(\omega))^{-1} - \frac{1}{j\omega C_{\rm ox}} = Z_{\text{Sub-BL}} \qquad (12)$$

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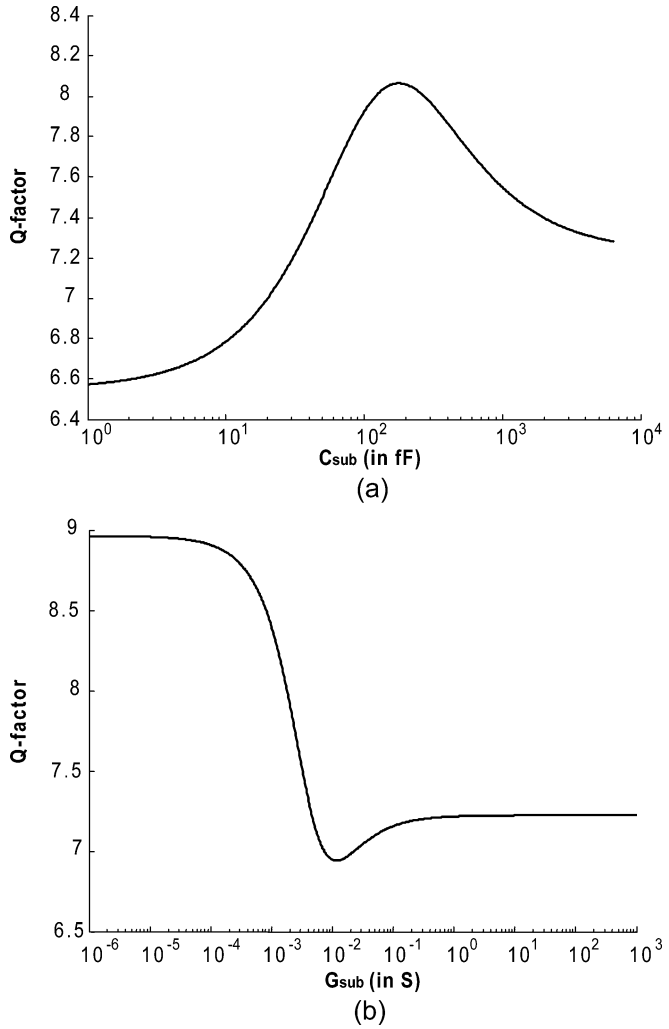

Fig. 32. Evolution of the conventional Q factor: (a) against $C_{\rm Sub}$ and (b) against $G_{\rm Sub}$ at 3 GHz.

where $Z_{\text{Sub-BL}}$ represents the parallel impedance formed by the substrate stack, except oxide layers

$$Z_{\text{Sub-BL}} = \sum_{n=1}^{N} \left(\frac{1}{G_{\text{Sub},n} + j\omega C_{\text{Sub},n}} + \frac{1}{G_{\text{BL},n} + j\omega C_{\text{BL},n}} \right). \tag{13}$$

The quality factor Q of the inductor can be deduced using (2) from (9) and (10).

Although magnetic losses can be accounted for in the electrical equivalent circuit, effects related to the electrical state of the BL (grounded or floating) remain difficult to represent by lumped elements. Fig. 29 shows the effects against the frequency on the admittance parameters Y_{11} and Y_{12} of the two spiral inductors in Fig. 27 of the grounded and floating BL.

In Fig. 30, the variation of the Q factor against the inductor series resistance $R_{\text{ind},j=1,2}$ is presented for different frequencies (1–4 GHz). Lower values of $R_{\text{ind},j=1,2}$ lead to greater Q factors at low frequency. Lower values for $R_{\text{ind},j=1,2}$ are achievable by increasing the inductor metal thickness (use of copper metallization) [2]–[4] or by means of geometry and topology optimization.

Fig. 31(a) and (b) shows the variation against the frequency of the Q factor, respectively, for different values of the BL resistance ($R_{\text{BL},j=1,2} = 10, 10^2, 10^3, 10^4\ \Omega$) and parasitic capacitance ($C_{\text{BL},j=1,2} = 1, 10, 100$ and 200 fF). It is seen that the maximum Q factor increases as the BL resistance and capacitance increase.

The dependence of the Q factor on the substrate parasitic conductance $G_{\text{Sub},j=1,2}$ and capacitance $C_{\text{Sub},j=1,2}$ is presented in Fig. 32(a) and (b), respectively, at 3 GHz. The variation of the Q factor against $G_{\text{Sub},j=1,2}$ presents a minimum value around 0.01 S. Lower substrate conductance $G_{\text{Sub},j=1,2}$ increases the maximum value of the Q factor. Lower $G_{\text{Sub},j=1,2}$ can be achieved by introducing between the BL and substrate a polysilicon patterned ground shield [9], [10], [26] or by inserting a local semi-insulating region in the silicon substrate obtained with proton implants.

IV. Conclusion

EM analysis of patterned deep-trench isolation for substrate coupling reduction and Q-factor enhancement, using the TWF-method, has been presented. Dependence of substrate coupling on the BL doping level and grounding configuration has been discussed. Influences of induced depletion regions on substrate coupling have been investigated. Evaluation, from EM simulations, of depletion regions capacitances has been proposed. Interruption of BLs and part of the silicon substrate by DTP to improve on-chip spiral inductor Q factors have been studied. The effects of the DTP penetration inside the substrate on the quality factor have been investigated. Distributed capacitances resulting from the BL grating have been evaluated. It has been observed that DTP considerably reduces the capacitances to substrate by a factor exceeding 50%. Combination of DTP with layout topological optimization has demonstrated high Q-factor improvement exceeding 4× enhancement. It has been shown that introduction of DTP can be more efficient in term of coupling reduction than completely removing the BL because of Si substrate screening provided by the remaining BL fragment. Limits of electrical lumped-element representation to account for distributed effects and magnetic losses are discussed. A general methodology for systematic extraction of compact equivalent-circuit models including mutual coupling terms has been proposed. The evolutions of the Q factor against extracted compact equivalent-circuit parameters have been presented allowing for direct optimization in common circuit simulators. The simulation results obtained with the TWF approach have been successfully validated by comparison with other relevant EM methods (2.5-D and 3-D approaches) and with published measurement data for reference structures.

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