TSV development, characterization and modeling for 2.5-D interposer applications.

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Abstract

IPDiA presents itself as the 3-D silicon leader providing innovative platforms for customers who want to demonstrate technological concepts based on TSV (Through Silicon Vias). The market segments Medical, Lighting, and Industrial addressed by the IPDiA Technology are adopting 2.5-D and 3-D technologies to increase the performances and density of their devices through the use of silicon interposers and TSV. Such devices can provide smaller form factors and lower power consumption while offering benefits such as allowing manufacturers to combine heterogeneous technologies. The via last approach jointly developed by IPDiA and CEA-Leti allows large possibility of integration combining TSV with active or passive devices.

This paper focuses on the key process steps , the method used for modeling . The electrical performances are described and the models extracted and used to predict performances of the customer products are presented. Preliminary reliability results are also shown. In the last part, 3 applicative cases are studied to understand the TSV electrical behavior on its nearby environment in silicon and the potential impact on devices integrated in the same interposer.

1. Introduction

In the past year IPDiA , and CEA-Leti jointly extended the work on the TSV process optimization to bring it at the right level of maturity and cost for the identified markets where added value is noticeable. Whereas the other companies adopted the via first or via middle process, IPDiA endorsed the via last approach. This choice is mainly driven by co-integrating TSV with PICS (Passive Integrated Connecting Substrate) Technology, the core business at IPDiA. Moreover, this solution brings the potential of making TSV on pre-existing CMOS wafer or on a 2,5-D Integrated Passive Devices interposer developed by IPDiA. After a detailed description of the key process steps : wafer bonding , via etching , isolation deposition, etch back, barrier and seed deposition, via filling , passivation and finishing , the electrical performances will be presented . The electrical behavior around the TSV in different applicative conditions will be deeply explained through 3 cases (Local voltage answer to a steep or frequency signal in a via and electrical interaction between a ground via and a signal via).

2. TSV process flow

IPDiA and CEA-Leti are focusing their developments on vias with 200µm depth and 75µm diameter. A specific design was performed to characterize the vias. This design is based on two metal layers on front side (first metal is aluminum and second metal is copper) and one copper layer on backside. Organic passivation and NiAu Under Bump Metallization were added on front side and backside. A schematic cross section is described on Figure 1.

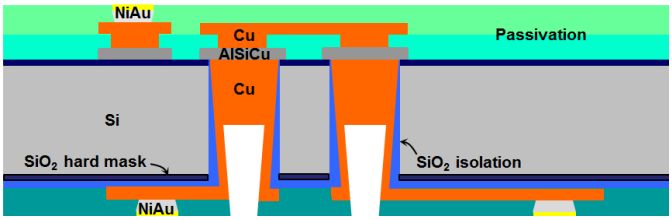


Figure 1. Schematic view of the via last architecture on the test vehicle

In via-last technology, vias are formed after the die have been fabricated, i.e after both the front end of line (FEOL) and BEOL processes have been completed.The key process steps are described in the following chapters.

Bonding process

To prevent wafer breakage, wafer level processing of 200µm thick interposer requires a wafer carrier. The bonded device wafer can be processed on a standard wafer processing equipment for backside processing. The temporary wafer bonding is carried out on a glass substrate for lithography alignment convenience. HT-10.10 glue (supplied by Brewer Science) is spinned on the glass carrier in order to get a 14µm-thick layer for the bonding of the device wafer in an EVG520 tool at 180°C under vacuum (10^{-4}mbar) with a force of 1600N during 3min. With this new stack, backside processing , thinning at 200µm and TSV, can be performed within range of process temperature up to 220°C.

Deep silicon etching

One of the main steps is the deep silicon etching. Due to the via last approach, after the bonding step, the via formation

needs a silicon etching from the backside to the first dielectric on front side. A good profile, a low roughness of the sidewall (scalloping due to isotropic lateral etch that happens during the vertical anisotropic etch) and a behavior without notching at the bottom of the via are essential to obtain conformal deposition on the 3D structures and to enhance functional and efficient vias.

The Bosch process (short cycling steps of isotropic etching with SF_6 and polymer deposition with C_4F_8) is implemented on a SIGMA FXP TRIKON with a low frequency pulsed generator avoiding the notching. A separate pulsed, low frequency power input (380 kHz) is applied to the platen during the etching cycle. This allows ions to escape more readily from structures when the etching cycle is done. From this a decrease in over-etch sensitivity emerges, and the notching of silicon structures is minimized. An over-etch up to 30% without notching was evaluated on 6 inches wafers. This process window absorbs the different Total Thickness Variations appearing during process (process on front side, bonding, grinding …). With these conditions an 8µm/min etch rate is got with photoresist consumption lower than 3µm.

Isolation deposition

The lateral isolation from the substrate is provided by a dielectric film deposited at 200°C in a PECVD reactor. The use of TetraEtOxySilane (TEOS) as a precursor in association with O_2 leads to a conformal SiO_2 layer thanks to the high sticking coefficient of the TEOS molecule compared with silane. The process temperature is adapted due to the presence of bonding glue, leading to a loss of conformity compared with the nominal conditions (350°C). Nevertheless, a thickness ratio of 0.25 is reached between the bottom corner (200µm deep) and the top plan since the thinner part of the dielectric film is 1µm thick when 4µm are deposited on the wafer backside. A relative permittivity (ε_r) of 5 is measured, which is 16% higher than in the nominal conditions. This can be explained by the presence of more SiOH bonds (dipoles that contribute to the polarization) due to a lower hydrogen desorption (see figure 2). These two parameters (minimum thickness and relative permittivity) look suitable for the propagation of RF signals through the TSV with limited attenuation due to the coupling with the substrate.

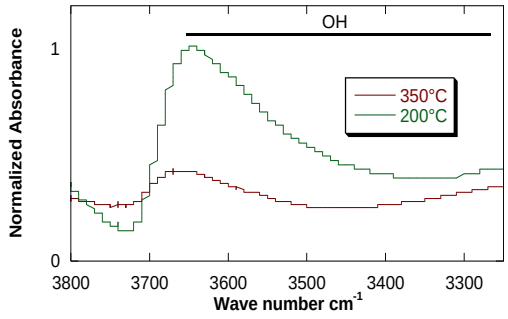


Figure 2. Infrared spectra of oxide layers deposited at 200°C (upper curve) and 350°C (lower curve).

The breakdown voltage of the dielectric material is about 4.8MV/cm, which indicates that our configuration is compatible with working conditions up to 480V.

Etch back

The isolation film is then removed from the bottom of the cavities simultaneously with the front side oxide so that the subsequent metallization comes in contact with the first metal level (1µm-thick AlSiCu). A CF_4/N_2/Ar (80/10/160sccm) gas mixture is used in a RIE (Reactive Ion Etching) plasma reactor in order to get a good anisotropy. Indeed Ar is responsible for the high vertical etch rate by bombarding the surface while saving the sidewalls. The high bias voltage (500W) and the low pressure (45mT) are also favorable for an access to the bottom of the vias. But the consequence is an increase of the wafer temperature which is prohibitive regarding the bonding glue (no temperature regulation from the chuck because of the glass carrier). For this reason, the process is splitted and cooling steps are inserted so that the glue remains below its glass transition temperature (T_g). In these conditions, the etch rate at the bottom is about 130nm/min and it reaches 250nm/min on the top plan. No significant etching is measured laterally. The selectivity to the AlSiCu stop layer is good enough (>100:1) not to worry about over-etch (except regarding the top plan layer thinning). After 3 x 3'30'' of etching (~8% OE) the two oxides are etched at the bottom of the vias and 1.5µm of TEOS remain on the top plan.

Barrier and seed deposition

The metallization of the TSV starts with the deposition of a Ti/TiN/Ti/Cu stack in an IPVD (Ionized Physical Vapor Deposition) reactor. Ti is used as an adherence layer and TiN as a barrier against Cu diffusion. The wafers are transferred from one process chamber (for Ti and TiN) to another (for Cu) under vacuum. As the process causes wafer warming, cooling steps are inserted inside each recipe in order to preserve the bonding glue.

Considering the deposition conformity for a depth of 200µm with an aspect ratio of 2.7, a thickness of 200nm is targeted on the top plan for Ti or TiN and 2.5µm for Cu. Figure 3 shows the stack on the top plan (left picture) and at the bottom corner (right picture), the Ti layers have been etched using diluted HF after sample preparation in order to better distinguish them from TiN. This highlights that there is almost no Ti on the sidewalls.

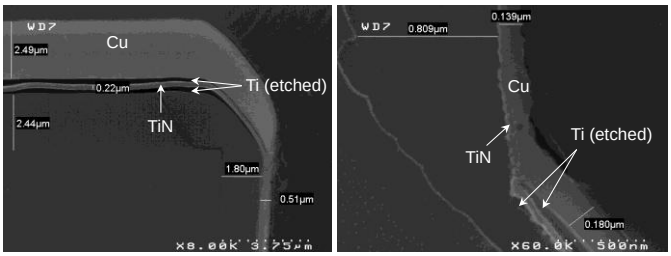
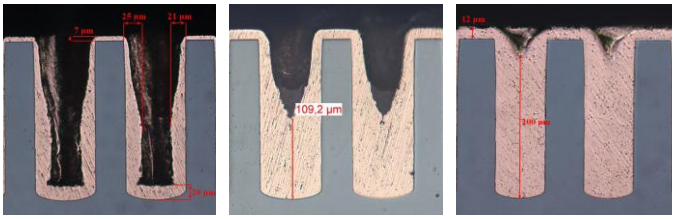


Figure 3. Cross-sectional SEM images of the top (left) and bottom (right) corner of a TSV after IPVD deposition

Copper super-filling

The Copper filling into through holes is obtained by electrochemical deposition. The chemistry has to be adapted to get conformal deposition into confined areas, which is much more difficult than on flat surfaces and to get the required copper thickness layer outside the vias. This adjustment is also driven by the vias density. The copper grows through a negative resist patterning which results in a 8µm-thick copper layer on surface and a 40µm-thick layer deposited inside the via. IPDiA has developed the "super-filling" technology which allows to modulate the copper thickness at the bottom of vias while limiting the thickness at the surface (figure 4).



(a) (b) (c)

Figure 4. Different cases of "super-filling" copper deposition (a) upholstered holes wall (b) half filling and (c) full filling

The copper plating is done on a Technotrans Microform 200. It is a 6-inch semi-automatic tool. The plating bath is a commercial base electrolyte solution added of a set of three-component additives Cabas TM (OM Group). The base solution contains 220 g/l copper sulfate [$CuSO_4{}^{-}5H_2O$], 50 g/l sulfuric acid [H_2SO_4] and 70 ppm chloride [Cl^-]. The three additives were added according to a specific formula providing continuity and high conductivity of Through Silicon Vias.

The supper-filling is obtained with a pulsed current. The advantages of the pulsed current towards the direct current (conformal copper growth) are its periodical breaks (Figure 5) which help the replenishment of reactive chemical compounds inside deep vias. The periodic break of pulsed current could set longer to enhance more the renewal of species.

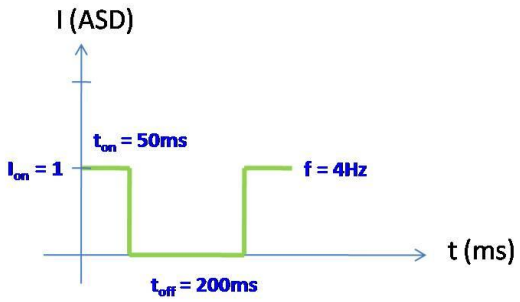


Figure 5. Example of pulsed current parameters used for super-filling at IPDiA

The flexibility of the copper thickness at the bottom of the vias allows a complete filling mandatory for specific applications, assembly constraints and facilitates the process of additional layer on backside. This choice is justified by three ways. The first one is to decrease the resistance of the vias. The second one is the reliability improved versus a simple liner of copper especially at the bottom corners of vias. The third one is the mechanical robustness needed during the full interposer process and mainly during assembly for complex architectures (double sided assembly module for example). Due to the via last approach, a 5 to 20µm-thick membrane (depending on the FE process) is created after deep silicon etching. A simple thin copper layer deposited in standard TSV is a potential root cause of failures during critical steps done without carrier (for example: dam and fill, underfill). Super filling meets with these specific needs.

Seed layer etching

After resist stripping, a wet bench sequence is used to etch the seed layer. First, the Cu is removed by using DSP ($H_2SO_4/H_2O_2/H_2O$: 1/2/50) and the Ti layer is etched with HF 0.25% at room temperature. Then for TiN, special conditions are required because of the presence of the ECD patterns. Indeed, in order to avoid overreaction with Cu, a very diluted SC1 solution ($NH_4OH/H_2O_2/H_2O$: 1/4/16) is used. As compensation the temperature is raised to 60°C. The underlying Ti is removed in the same bench during the TiN overetch.

Passivation and finishing

Copper may be subject to oxidation and must be protected by an organic passivation. Depending on the application and the packaging constraints, 3 main sketches can be elaborated to carry out the passivation step: a cap over the through holes, a conformal thin coating, or a complementary via filling.

A NiAu electroless underbump metallization and Copper-Tin microbumps executed as the last steps are shown on figure 6.

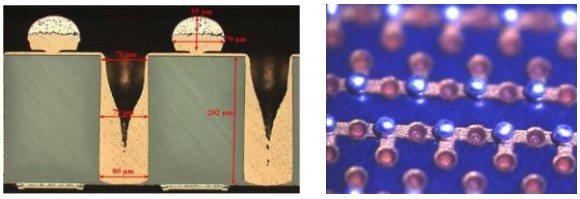


Figure 6. TSV combined with µbump technology on back side

3. Measurement results and discussion

Based on the process described above, wafers have been processed and characterized in HF mode from which a π-shape equivalent model previously proposed and detailed is validated. Then, first reliability tests are shown.

HF Measurements results on HR Silicon

The results of the TSV performance are measured at High Frequency (HF) on a specific test structure called Dual Via Chain (DVC) including CPW (Co-Planar Waveguide) adapted access, 2 TSV and a backside layer, as shown in figure 7.

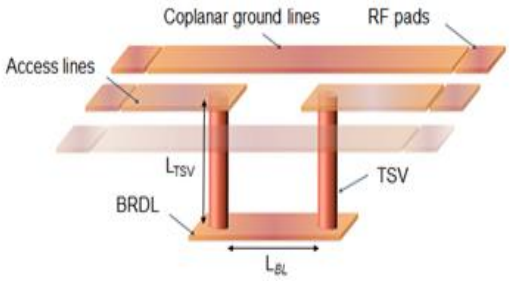


Figure 7. Dual Via Chain schematic view

HF results are presented on figure 8. It represents the transmission and reflection of a 250µm length DVC.

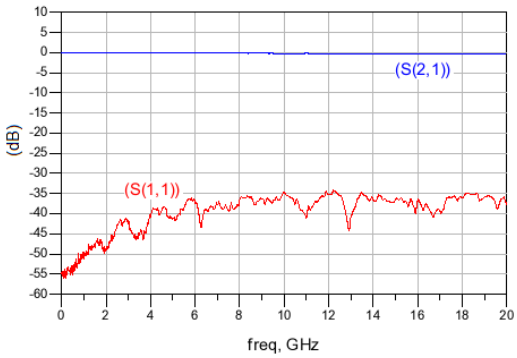


Figure 8. HR measurement result. Transmission (S21 in blue) and reflection (S11 in red)

The good result of this DVC shows a rejection between transmission and reflection higher than 35dB throughout the frequency range (up to 20GHz), and a very low loss in transmission, better than 0,35dB. These performances are obtained thanks to the mastery of the process, particularly with the complete recovering electric contact backside, and the isolation of the TSV even on its critical corner in the bottom.

HF Modeling of DVC on HR Silicon

According to the literature and physical hypothesis we used a generic π-shape model RLCG (see figure 9). Different lengths of backside line, (250, 500 and 1000µm) permitted to decorrelate the impact of pads and access lines from that of the 2 TSV.

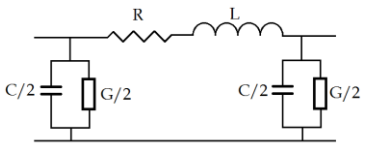


Figure 9. π-shape electrical equivalent model for parameters extraction

The elements of the model were extracted thanks to equations figure 10, in a cylindrical geometry approximation of the TSV, where L_{TSV} is the depth of the TSV (approximately the thickness of the wafer, t_{Si}), r_{TSV} its radius ant t_{Ox} the thickness of the oxide:

$$R_{DC} = \frac{1}{\sigma} \frac{L_{TSV}}{\frac{\pi}{4}\left[4(r_{TSV} - t_{Ox})^2 - 4(r_{TSV} - t_{Ox} - t_{Ti/Cu})^2\right]} \quad (1)$$

$$C_{Ox} = \frac{2\pi\varepsilon_0\varepsilon_{Ox}t_{Si}}{\ln\left(\frac{r_{TSV}}{r_{TSV} - t_{Ox}}\right)} \quad (2)$$

$$L = \frac{\mu_0}{2\pi}\left[t_{Si}\ln\left(\frac{t_{Si} + \sqrt{t_{Si}^2 + r_{TSV}^2}}{r_{TSV}}\right) + r_{TSV} - \sqrt{t_{Si}^2 + r_{TSV}^2} + \frac{t_{Si}}{4}\right] \quad (3)$$

Figure 10. Equations of the π-shape model elements

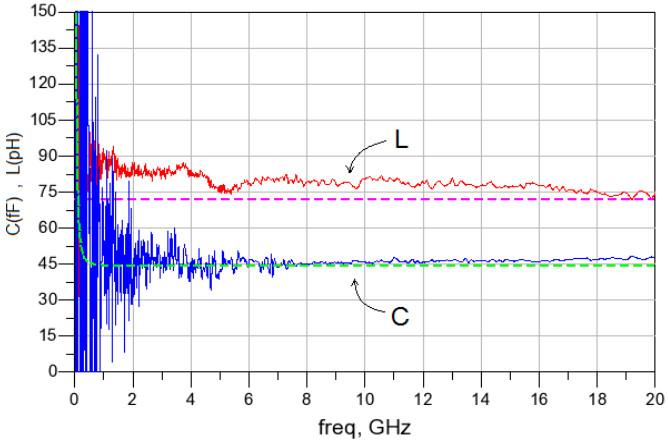
No physical or empirical models are known for conductance, so we have estimated it numerically and thanks to literature [1]. Moreover the aim of using High Resistivity (HR) silicon is to reduce dielectric losses and make conductance a secondary endpoint.

The capacitance of the parasitic branch figure 10 can be splitted into two successive and physical capacitances, deriving respectively from oxide and silicon, depending on the frequency range of the signal propagated. For DC signal, only oxide capacitance is considered, figure 10 (2), which is the asymptotic value of Figure 8 when the frequency tends to 0. However for upper frequency range this capacitance can be seen as a competition between those two capacitances in series. Moreover the theoretical value of Cox is 1,5pF (that confirms, by retro-simulation, the thickness of the dielectric layer of 1,25µm) and with a quick study magnitude gap between these two capacitances we can consider that the asymptote of the capacitance curve when frequency tends to infinite determines silicon capacitance.

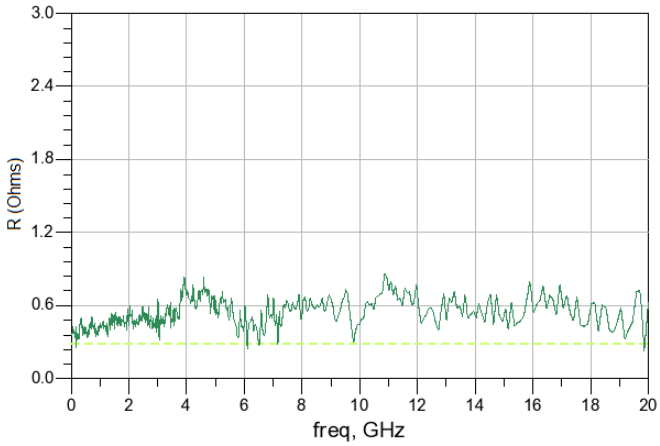
Model validation

According to following figure 11, we can see that the analytical equations can be used to precisely describe TSV performances.

Despite the noise, sensitivity of R is quite stable, mainly at low frequency. The C curve faithfully describes the competition between C_{Si} = 43fF and C_{ox} analytically evaluated to 1,5 pF. Despite we use an analytical approach to miscorrelate the impact of the inductance of the backside line and that of the TSV, we obtain a good coherence between measurement and model. The very low value of the conductance on HR silicon makes it too tricky to be extracted efficiently from noise and was estimated to under 1mS on all the frequency range of measurement.



(a)



(b)

Figure 11. Simulation (dashed line) and measurement (solid line) of extracted TSV π-shape elements. (a) Parallel capacitance and serial inductance, (b) serial resistance.

The use of HR silicon has enabled us to reduce consistently conductive loss in DVC of TSV. The low value of resistance and conductance introduced by the use of HR substrate makes them more sensitive to noise effect but their trend allow us to validate our model throughout all the frequency range of measurement.

TMCL reliability test

In order to test the ability to withstand cyclical exposure and introduce mechanical stress into TSV, they were subjected to thermal cycling (TMCL) as recommended by JEDEC standard [3] (cycling: -40°C to 125°C with a 10°C/mn ramp, during 200, 500 and 1000 cycles)

Figure 12 is the layout of the structure used for this study. The DC resistance of a daisy chain made of 50 TSV is measured by a 4 points probe system.

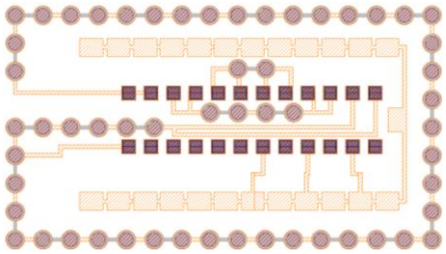
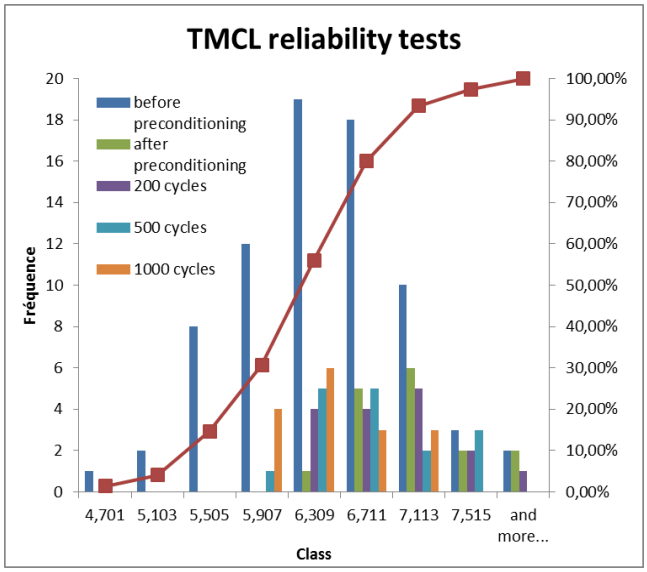


Figure 12. Daisy chain (50 TSV) used for the reliability tests.

Figure 13 shows the electrical results after this mechanical stress. Preconditioning was made on a full wafer (74 DVC structures) and TMCL reliability tests on ¼ wafer (16 DVC structures).



(a)

Statistics	*Before Precond.*	*0 cycles*	*200 cycles*	*500 cycles*	*1000 cycles*
Average	6,193	6,886	6,721	6,516	6,240
error deviation	0,073	0,126	0,119	0,110	0,101
median	6,172	6,869	6,714	6,520	6,236
standard deviation	0,630	0,487	0,459	0,440	0,404
sample variance	0,396	0,237	0,211	0,194	0,163
number of samples	74	16	16	16	16
Confidence interval (95.0%)	0,146	0,270	0,254	0,235	0,215

(b)

Figure 13. Statistic chart (a) and table (b) on DC resistance results after TMCL reliability test

The Normal distribution of DC resistance on full wafer test (blue bar chart) and the cumulative distribution function (red curve) validates a good uniformity on full wafer for TSV chain structure. We can note that we used for TMCL reliability test the ¼ wafer having the structure with the higher resistance. Moreover the low number of structure induces a non-Normal distribution. However the low confidence interval on them reveals good uniformity and so a good maturity of the process.

The small and successive decreases of the DC resistance can be interpreted as a crystalline rearrangement of copper introduced by successive cycling.

This statistical approach allows us to estimate single TSV resistance to 124mΩ with a very high accuracy i.e. an error lower than 2%.

4. Applicative Cases

After describing the via process, the electrical performances and the extracted model, a comprehensive study of TSV induced noise is presented. TSV may cause noise in the substrate or disturb the signals propagated in TSV neighbors. These disturbances must be simulated and validated to meet the requirements of all applications that can be integrated on an interposer with vias. Cohabitation between TSV and integrated devices has to be mastered and tuned. Here below, three important cases are studied.

Case 1 – Local body voltage variation resulting from steep signal propagation in a TSV

This first application case corresponds to the typical case where TSV are processed as via last on a pre-existing CMOS wafer. In that configuration, it is of primary interest to estimate how a voltage transition in the TSV will couple and propagate across the surrounding substrate, thus changing locally the body voltage [4], [5]. In such a case, those adjacent devices might be adversely impacted by the voltage rise, although the exact impact on performance will be extremely dependent upon device architecture (mostly size of transistor) and to a larger scale to the noise margins used in the design of the impacted IP block.

Figure 14 presents the body voltage (1µm² body) variation assuming a typical case for digital circuitry where the TSV is processed into a thinned substrate (200µm) having a uniform resistivity of 10 Ω.cm. The perturbation signal is assumed to be a high drive square 1.2V wave with a typical rising time of 200ps and high signal strength (ideal voltage source). The backside comprises localized GND returns.

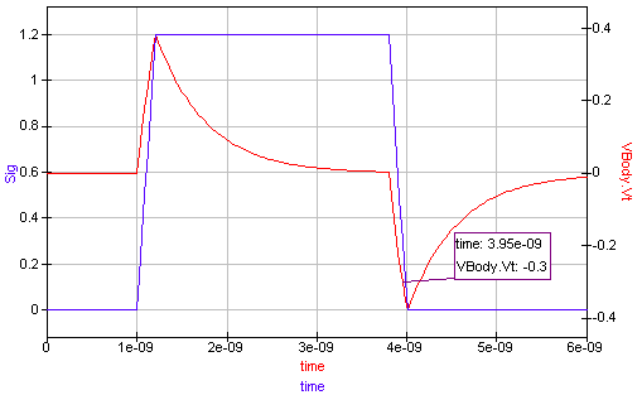


Figure 14. Blue curve – high drive digital signal propagating in a TSV. Red curve – local body voltage swing in silicon resulting from digital propagation of the signal in the TSV at 30µm distance

The figure 15 presents the maximum local body voltage swing as the function of the distance between the body and the TSV. The blue dashed curves represent the keep-out distance around the TSV. From that figure, it can easily be seen that the voltage swing is limited below 60mV outside of TSV the keep-out area. This voltage swing figure is on par with simulation published in the literature on much smaller via geometries [4], [5], [6].

This excellent performance is explained by :

- Low TSV to substrate capacitance. The reduced capacitance value is assumed to be resulting from oxide thickness combined with a relatively low substrate doping that is favorable to TSV capacitance depletion,
- The insertion of large GND return patterns on the wafer backside that are providing favorable attenuation scheme.

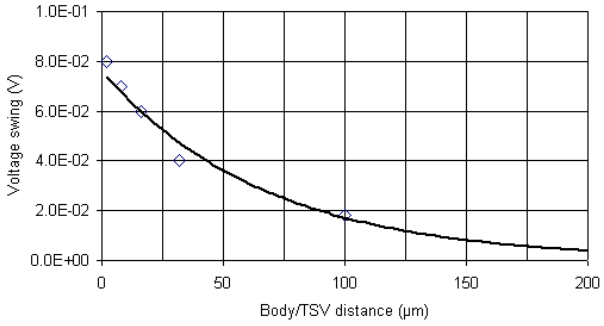


Figure 15. Maximum body voltage swing resulting from a 1.2V voltage raising edge propagated in the TSV (Tr=200Ps) as a function of distance between the body and the TSV. Blue dashed line represents the TSV keep out area.

Case 2 – local body voltage variation as a function of frequency

In this second application case, we consider the same TSV implementation as above and explore the body voltage swing as a function of frequency of the signal propagated in the TSV. This would be a typical application case when the TSV

used to feed through substrate an analogue signal. We consider, variations where the body is localized ranging from:

- Just outside the keep out area (i.e. at 15 µm from the outer sidewall of the TSV)
- Up to 100µm distance.

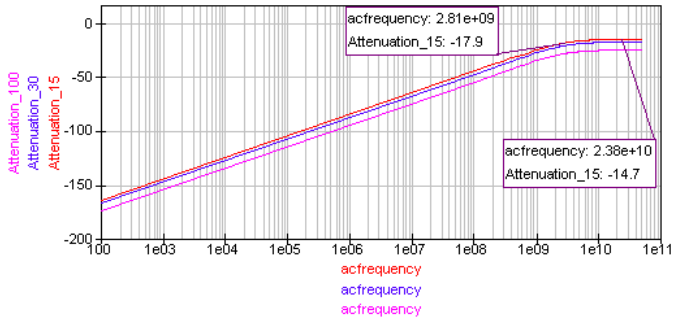


Figure 16. Attenuation (dBv) between voltage propagated in the TSV (high drive signal) and voltage seen by a local body placed on the wafer surface at varying distance from the TSV outer wall : resp. Red/Blue/Pink related to resp. 15µm/30µm/100µm.

From this simulation we observe (as expected) that the TSV behaves as a high-pass filter with a cut-off frequency (-3db), mostly determined by the TSV to substrate capacitance. This cut-off frequency is around 2.9 GHz for the actual TSV geometry.

It can be further seen, that the overall attenuation level, is also governed by the attenuation calculated from the ratio between different resistive paths i.e.:

- Path between the TSV and the local body,
- Path between the TSV and the GND return localized on the backside,

Besides native isolation resulting from TSV structure, isolation can be further enhanced by inserting proper path return to the GND in the design. Again, this attenuation figure with simulation is published in the literature on much smaller via geometries [4], [5], [6].

Case 3 – Signal to ground coupling between neighboring TSV

This third application case aims to describe the electrical influence of the TSV when inserted in transmission in the RF signal path, while neighboring TSVs are connected to the GND. 2 simple cases are considered:

- Where GND is connected to a neighboring TSV located at nominal pitch (i.e. 125µm) – this would correspond to the case where RF signal is propagated through the substrate with its return path to GND.
- Where GND is connected to 4 neighboring TSVs so as to provide lower impedance return to GND (less ESR, less ESL) combined with a better electrostatic shielding of the surrounding substrate (see application case 1 and 2).

A 1kΩ.cm floating substrate is considered, with similar TSV geometry as above (75µm diameter, 125µm nominal pitch and a 200µm thick substrate) which corresponds to a typical case where TSV would be used in an RF interposer in combination with the IPDiA PICS® technology.

Signal transmission and reflection to ground are presented on the figure 17.

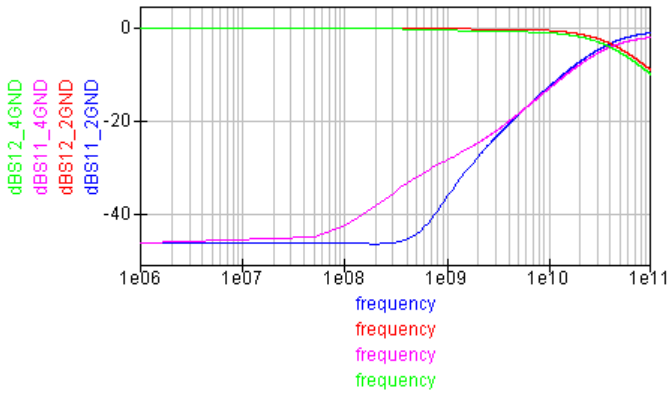


Figure 17. Scattering figure (S parameter) of a TSV used to feed an RF signal through a silicon substrate. dB12 corresponds to the attenuation on the transmitted signal while dB11 corresponds to the attenuation on the reflected signal. The label "_4" corresponds to configurations where signal TSV is surrounded by 4 GND while the label "_2" corresponds to configurations where the TSV propagating the signal is surrounded by 4 GND.

In any of the above configuration, it can be seen that insertion loss are negligible up to frequency above10 Ghz with a cutoff frequency (-3dB) above 20 Ghz. Also reflection to ground shows earlier degradation in frequency in the configuration "_4" as a consequence of reduced impedance to ground compared to "_2" configuration, the overall isolation remains > 20dB to frequency up to 4Ghz.

From this perspective, the proposed TSVs technology has enough performance to frequency margins to comply with most of mobile communication (GSM, WCDMA, LTE) as well as UWB, WLAN (WiFi™) standards.

Conclusion

IPDiA is providing a robust copper based, backside via technology that is fully scalable to volume production. This technology features TSV with a nominal diameter of 75µm and a pitch of 125µm that have been demonstrated in 2.5D passive interposer type application as well as backside vias processed in pre-existing active CMOS wafers.

The optimized copper filling allowed reducing ESL/ESR parasitic in the signal propagation path while the thick dielectric isolation allowed an ultra low capacitance to substrate.

As a result of the above, it has been demonstrated excellent behavior with respect to noise injection into substrate when TSV are used for propagating fast switching

digital signal (i.e. low raising time in the order of ~100ps). Equivalently, it has been shown that the noise injected in the substrate as a result of a sin wave propagating in the TSV was very low up to very high frequencies (>3Ghz). This would exceed requirements for most of the analog application.

Finally, it has been demonstrated that TSV could be satisfactorily used for RF application, even in the case where sensitive RF signal are routed in close vicinity of GND return path [6].

Acknowledgments

The authors would like to thank the members of OSEO for sponsoring this work included in the PRIIM project.

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